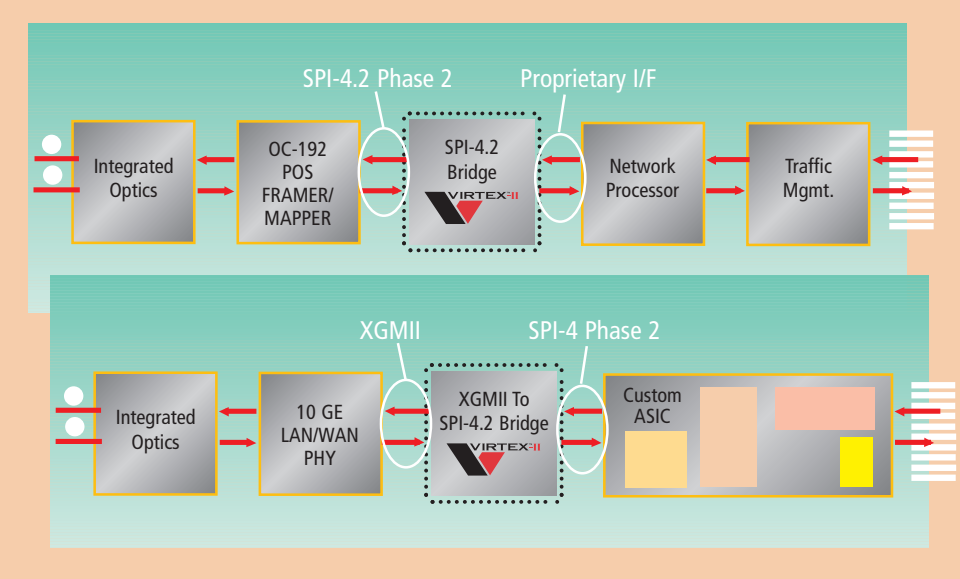
SPI-4.2 (POS-PHY Level 4) Cores

Designing terabit networks can be quite a challenge; the insatiable demand for higher performance and higher bandwidth constantly stretches the boundaries. To satisfy this need, the Optical Internetworking Forum (OIF) adopted the SATURN® Group's POS-PHY™ Level 4 (PL4) technology based on the original Packet-Over SONET/SDH (POS) specifications. POS enables network core routers to send native IP packets directly over SONET/SDH frames, providing lower packet overhead and lower cost per megabit than any other data transport method. Xilinx provides fully compliant System Packet Interface Level 4 Phase 2 (SPI-4.2) cores to address the data path connectivity between POS Physical Layer devices and Link Layer devices in terabit networking and communications systems. Our solutions include SPI-4.2 LogiCORE™ products designed to work with the latest Virtex™-II Series Platform FPGAs.



Xilinx SPI-4 Phase 2 applications

Key Benefits

The Xilinx POS-PHY Level 4 cores provide user-configurable options, excellent flexibility, and seamless operation with industry leading PL4 ASSPs, ensuring maximum bandwidth data transfers. The key benefits include:

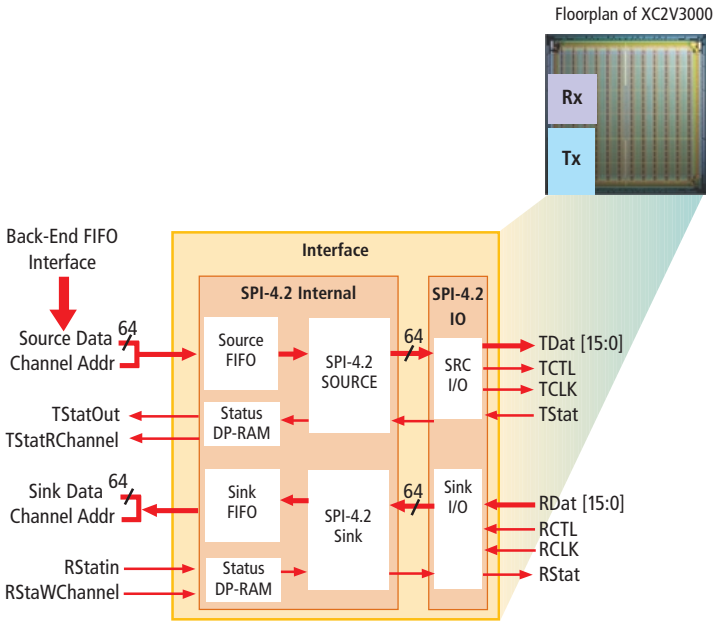
- **Full Compliance –** The Xilinx SPI-4.2 core is fully compliant with the OIF System Packet Interface Level-4 Phase 2 and the SATURN POS-PHY Level 4 Standards.
- **Proven Interoperability –** The Xilinx SPI-4.2 core is proven to operate seamlessly with the leading ASSP devices such as the Mindspeed M29730 OptiPHY,™ the PMC-Sierra XENON™ family, and the Intel IXF1810x family.
- **Single-chip Dynamic Alignment –** the Xilinx SPI-4.2 core centers the data eye and clock edge without additional external devices, reducing overall system design cost and complexity.
- **10 Gbps Performance –** The Xilinx SPI-4.2 core can support OC-192 rates by providing an aggregate bandwidth of 12.8 Gbps in Virtex-II series FPGAs. The performance is achieved using features such as the Digital Clock Manager, Block RAM, and high-speed LVDS I/O buffers with double data rate (DDR) registers.
- **Faster Time to Market –** The Xilinx SPI-4.2 core accelerates the development of emerging OC-192 POS and 10 Gigabit Ethernet systems, by decreasing your development time, and allowing you to focus on adding value to your system.

XILINX®

Key Features

Here are the key features of the Xilinx SPI-4.2 core:

- Fully compliant SPI-4.2 interface with integrated FIFO
- Multi-link operation, scalable from 1-256 links
- Supports static and dynamic alignment
- Split (Source/Sink) configurations allowing for flexible system egress and ingress architectures
- Supports mux/demux and bridging functions
- Automatic transmission of source data based on source FIFO threshold
- DIP-4 and DIP-2 parity generation and checking
- 64-bit internal data path up to 200 MHz to support seamless integration of back-end logic
- Demonstration testbench for quick start-up
- Delivered through CORE Generator



Implementing a SPI-4.2 interface in Virtex-II FPGAs

Applications

Xilinx SPI-4.2 solutions are ideally suited for line cards in gigabit routers, terabit and optical cross connect switches, and a wide range of multi-service Dense Wavelength Division Multiplexing (DWDM) and SONET/SDH-based transmission systems. Due to its extremely high performance, low pin count, and streamlined data transfer protocol, the SPI technology is widely used to connect network processors with OC-192 framers and mappers as well as Gigabit and 10 Gigabit Ethernet data link MACs.

For More Information

We are continually enhancing the SPI-4.2 core, adding more features and capabilities. For the latest details on Xilinx SPI-4.2 solutions, visit Xilinx Connectivity Central at www.xilinx.com/connectivity, or call your local Xilinx representative.

Xilinx SPI-4.2 Solution - LogiCORE Facts

LogiCORE™ Facts		
Core Specifics		
Supported Family	Virtex™-II	
Core Performance: Static Alignment		
Performance (Virtex™-II -5)	800 Mbps on SPI-4.2 Interface 200 MHz on User Interface	
Performance (Virtex™-II -4)	640 Mbps on SPI-4.2 Interface 160 MHz on User Interface	
Core Performance: Dynamic Alignment		
Performance (Virtex-II -5)	700 Mbps (+/-5%) on SPI-4.2 Interface 175 MHz on User Interface	
Core Resources: Static Alignment		
	Rx	**Tx**
Virtex-II Slices	1950	1600
Virtex-II Block RAM	5	6
Global Clock Buffers	2	3
Digital Clock Managers (DCM)	1	2
Core Resources: Dynamic Alignment		
	Rx	**Tx**
Virtex-II Slices	2700	1600
Virtex-II Block RAM	5	6
Global Clock Buffers	2	3
Digital Clock Managers (DCM)	1	2
Provided with Core		
Documentation	Quick Start Guide Design Example Guide	
Design File Formats	EDIF netlist	
Constraints File	.ucf and .ncf	
Design Tool Requirements		
Xilinx Tools	Alliance/Foundation/ISE v4.2i SP3	
Support		
Support provided by Xilinx, Inc.		

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