EDUCATION SERVICES
Xilinx Global Services

EDUCATION SERVICES COURSE LISTING

EFFECTIVE SEPTEMBER 1, 2002

Designing with Rocket I/O Multi-Gigabit Transceiver **Coming Soon!**
Level: Intermediate **Duration: 2 days** **Credits: 10** **Cost: $1000**

Learn how to employ Rocket I/O™ in your Virtex-II Pro™ design. Understand and use the features of the Rocket I/O transceiver blocks such as CRC, 8b/10b encoding, channel bonding, clock correction, and comma detection. Additional highlighted topics include debugging techniques, use of the Architecture Wizard, and synthesis and implementation considerations. This comprehensive course equally balances lecture modules with practical hands-on lab work.

Embedded Systems Development **Coming Soon!**
Level: Intermediate **Duration: 2 days** **Credits: 10** **Cost: $1000**

Looking for a hands on approach to developing embedded systems? If you're an FPGA design engineer or system architect interested in designing with Xilinx embedded processors, this course is for you. Attend this training to gain a better understanding of the main features of the Virtex-II Pro and MicroBlaze™ architectures while using the accompanying development, debug, and simulation environments and tools. Course objectives include designing and building an embedded system using System Generator Pro and developing and integrating hardware and software IP onto the system. This course is based upon the Embedded Development Kit.

Fundamentals of FPGA Design, ISE 5
Level: Introductory **Duration: 1 Day** **Credits: 5** **Cost: $500**

Understand Xilinx FPGA architecture and learn to implement a complete design in one day. This course provides you with an introduction to designing with Xilinx FPGAs using Xilinx ISE 5. New ISE 5 features covered in this course include the Architecture Wizard, assistance in assigning pins, and creating area constraints (PACE). Other topics include design planning, implementation options, and global timing constraints. Reduce your learning curve through several practical labs.

Designing for Performance, ISE 5
Level: Intermediate **Duration: 2 days** **Credits: 10** **Cost: $1000**

Learn design techniques to help improve your design's performance. This course builds on the principles covered in our "Fundamentals of FPGA Design" course with an emphasis on achieving timing closure. Topics include FPGA design techniques, HDL coding techniques, the CORE Generator™ system, power estimation, timing analysis, advanced timing constraints, and advanced implementation options.

Advanced FPGA Implementation, ISE 5
Level: Advanced **Duration: 2 days** **Credits: 10** **Cost: $1000**

Push the limits of your design by learning how to effectively use the advanced-level Xilinx tools. Several new ISE 5 features are covered in this course, which include Data2BRAM enhancements, incremental design, scripting capability in Project Navigator, ability to create an IP core from an RPM, and FPGA Editor Probe enhancements.

Designing for Performance for the ASIC User, ISE 5
Level: Intermediate **Duration: 3 days** **Credits: 15** **Cost: $1500**

Are you an ASIC designer that wants to get the most out of your FPGA design? Then, this course is for you. Learn the FPGA design techniques you need to improve your design's performance. Course highlights include ASIC design and verification techniques compared and contrasted to FPGA design and verification techniques, how to re-target ASIC code for Xilinx with a 10-step Conversion Guide, and HDL inference of FPGA resources with coding examples.

Introduction to Verilog
Level: Introductory **Duration: 3 days** **Credits: 15** **Cost: $1500**

This comprehensive course is an effective introduction to the Verilog language. Course emphasis includes targeting Xilinx and FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design using a top-down synthesis approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

Introduction to VHDL
Level: Introductory **Duration: 3 days** **Credits: 15** **Cost: $1500**

This comprehensive course is an effective introduction to the VHDL language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design using a top-down synthesis design approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

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Advanced VHDL **Coming Soon!**
Level: Advanced **Duration: 2 days** **Credits: 10** **Cost: $1000**

Increase your VHDL proficiency by learning advanced techniques to help you write more robust and reusable code. This comprehensive course is targeted towards designers who already have some experience with VHDL. The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs, as compared to lecture modules.

PCI Core Basics
Level: Introductory **Duration: 1 day** **Credits: 5** **Cost: $500**

This course introduces basic PCI concepts and architectures. It also gives an overview of Xilinx PCI solutions and includes two labs illustrating the general design flow from core configuration to verification and PCI bus transactions.

Designing a PCI System
Level: Intermediate **Duration: 2 days** **Credits: 10** **Cost: $1000**

Using the Xilinx PCI core in your system? This course provides intensive training for designing with Xilinx PCI products. You will learn about specific Xilinx PCI cores, including PCI 64/66 Virtex, PCI 32 Spartan™/Spartan-XL, and PCI 32/33. Design concepts and verification strategies for a PCI system design are covered in detail. The course focuses on hands-on experience via labs where you perform extensive simulation verification using the Xilinx PCI core.

DSP Design Flow
Level: Intermediate **Duration: 3 days** **Credits: 15** **Cost: $1500**

This course covers the Xilinx design flow for implementing DSP functions. The main focus of this course is on the System Generator for DSP. The class also includes information on HDL design flow, the CORE Generator, design implementation tools, and hardware verification. You will gain extensive experience with system-level design, while also becoming familiar with Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware verification.

DSP Implementation Techniques
Level: Advanced **Duration: 3 days** **Credits: 18** **Cost: $1800**

This course bridges the gap between the DSP algorithm/system designer and the hardware engineer. As well as describing how the algorithms can be efficiently implemented, the techniques will also demonstrate which decisions, at the system level, have the greatest impact on the implementation process and product costs.

Free Recorded e-Learning – Learn All About What's New In ISE 5

Learn about the advanced ISE software technologies in our series of free, recorded ISE 5 technical lectures:

- What's New In ISE 5.1i
- PACE
- Architectural Wizard
- Incremental Design
- Simulation Improvements
- Data2BRAM

These recordings are available online 24 hours a day/7 days a week.
View them on the Education Services website at:
http://www.xilinx.com/support/training/ise-whats-new-5.htm

For a complete description of the above courses, including detailed course outlines, lab descriptions, and availability in your region, please reference: **http://www.support.xilinx.com/support/training/training.htm**

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