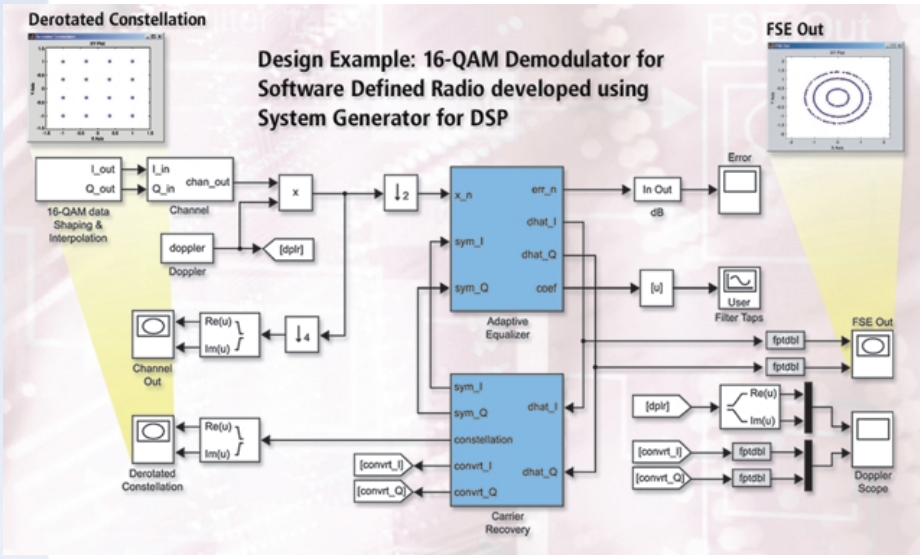
XILINX SYSTEM GENERATOR™ For DSP

System Generator for DSP

A Powerful High-level DSP Modeling Environment

Xilinx FPGAs have become the preferred choice for many high-performance, programmable DSP applications. However, you may not be familiar with our usual FPGA design tools and processes, and you may not have the time to learn DSP design techniques. So, how do you make the best use of our DSP technology, with the least effort?

The System Generator for DSP allows you to easily target your DSP designs to Xilinx FPGAs directly from the MathWorks MATLAB®/Simulink® environment. Your designs will automatically make the most efficient use of the Xilinx device architecture and you don't need to worry about understanding VHDL or Verilog languages to do it. You will achieve optimal DSP designs, automatically, and they will outperform any other solution.



Get the DSP Advantage

The System Generator for DSP uses Simulink to represent a high-level, abstract view of your DSP system; it automatically maps your system to a predictable, highly efficient hardware implementation that allows you to customize the architecture to suit your DSP algorithm. You get:

- **High Performance –** You can easily design and implement very high performance and multi-rate DSP designs (up to 300 MSPS) targeting our Virtex™-II Series FPGAs.
- **A Powerful, high-level modeling environment.** Simulink is widely used for algorithm development and verification. You don't need to understand the device architecture to achieve optimal results.
- **Optimized, predictable, lowest cost implementation.** The Simulink system model and the FPGA hardware implementation are identical, so you are assured of perfect results. And, your implementation will be fast and efficient through the use of intellectual property (IP) designed specifically for the Xilinx device architecture. The IP blocks provide a wide range of functionality from arithmetic operations to complex DSP functions.
- **Unprecedented Productivity.** You can describe an algorithm in mathematical terms, realize it in the design environment using double precision, trim it down to fixed point, and translate into efficient hardware, all in one environment. This drastically reduces development time and misunderstanding between the DSP system architect and the FPGA designer.
- **Access to key device features.** While DSP architects can work at a high level of abstraction, FPGA-literate designers can access the key features of the device to achieve the highest performance and efficiency.

XILINX®

A Powerful, High-level DSP Modeling Environment

The System Generator for DSP is fully integrated with Simulink and conforms to the Simulink sample-time and data type propagation methodology. Modeling and front-end simulation are performed in Simulink using a library of Xilinx blocksets for arithmetic, logic, and DSP functions. It provides the following capabilities:

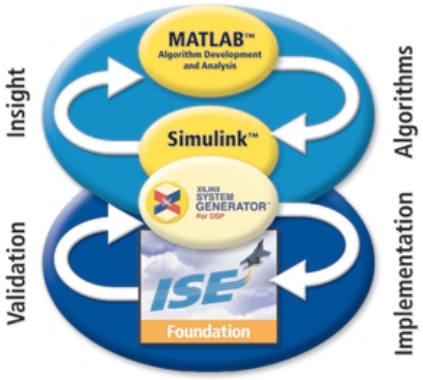
- Block customization uses Simulink Dialog Boxes, allowing interaction with MATLAB, and parameterization via MATLAB functions
- Simulations are bit- and cycle-true to the FPGA. This gives you an exact representation of actual performance including internal resolution and bit precision as well as latency level.
- Arithmetic abstraction automatically provides arbitrary precision fixed-point functions, including quantization and overflow.
- Simulation of double-precision as well as fixed-point operation provides the ability to determine the quantization error at any point of your design.
- Works with the Xilinx ISE 5.1 environment, and the Xilinx CORE Generator,™ to use our latest portfolio of DSP algorithms, implemented as IP cores.
- Supports Virtex-II Pro,™ Virtex™-II, Virtex-E, Spartan™-IIE, and Spartan-II FPGA families.

Industry's Best Productivity

The System Generator for DSP generates highly optimized VHDL code and IP cores,with the hierarchy preserved. It also generates a number of helpful files, including:

- ISE project generation to simplify your design flow
- HDL testbench and test vectors along with .do files for simulation
- A constraints file (.ucf) for timing constraint information and I/O allocation
- ModelSim script files for behavioral simulation
- Provides mixed language support for Verilog, supporting a dual synthesis flow
- Project files for Synplify Pro, Leonardo Spectrum, and Xilinx XST (a part of the ISE Foundation™ software).

  Over a dozen demos/tutorials such as 16 QAM demodulator, discrete wavelet transform and Costas loop are also included.



Access to Key Device Features

System Generator for DSP is part of the Xtreme DSP solution which also includes IP cores, DSP classes, DSP boards and the industry's leading FPGAs, which include features such as:

- Up to 556 embedded 18x18 multipliers, operating at speeds of 300MHz.
- Up to 10 Mbits of on chip block memory
- SRL16 shift-register logic
- Optional control signals such as clock enable and reset.

Take the Next Step

The Xilinx System Generator for DSP is fast, easy to use, and very powerful – and it costs just $1,995 (Part # DS-SYSGEN-4SL-PC). For the full details, and access to a 90 day evaluation, go to: **www.xilinx.com/dsp**. Or, you can place your order at: **www.xilinx.com/store**. Register for our DSP training classes and training bundle (Part # DS-SYSGEN-4SL-T) at: **www.xilinx.com/support/training/training.htm**

VIRTEX-II VIRTEX-II VIRTEX-II PRO SPARTAN-III SPARTAN-IIIE

XtremeDSP

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