DataSourceCD Q1-2003: Xilinx Packaging and Thermal Characteristics
Package Electrical Characteristics

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Introductions

In high-speed systems, the effects of electrical package parasitics become very critical when optimizing for system performance. Such problems as ground bounce and crosstalk can occur due to the inductance, capacitance, and resistance of package interconnects. In digital systems, such phenomena can cause logic error, delay, and reduced system speed. A solid understanding and proper usage of package characterization data during system design simulation can help prevent such problems.

Theoretical Background

There are three major electrical parameters which are used to describe the package performance: resistance, capacitance, and inductance. Also known as interconnect parasitics, they can cause many serious problems in digital systems. For example, a large resistance can cause RC and RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance can cause RC delays, crosstalk, edge-rate degradation, and signal distortion. The lead inductance, perhaps the most damaging parasitic in digital circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge rate degradation, and signal distortion.

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bondwire, lead, or other interconnect inductance.

When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise/fall times, the larger the current spikes are: $I = C * dv/dt$. Current spikes through the IC pin and bondwire induces a voltage drop across the leads and bondwires: $V = L * di/dt$. The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

Analytical Formulas for Lead Inductance

Rectangular Leadframe/Trace (straight)

$$L_{self} = 5l\left[\ln\left(\frac{2l}{w+t}\right)+\frac{1}{2}\right] \quad nH$$

(no ground)

$$L_{self} = 5l\left[\ln\left(\frac{8h}{w+t}\right)+\left(\frac{w+t}{4h}\right)\right] \quad nH$$

(above ground)

l = lead/trace length

w = lead/trace width

t = lead/trace thickness

h = ground height

unit = inches

Bondwire (gold wire)

$$L_{wire} = 5l\left[\ln\left(\frac{2l}{r}\right)-\frac{3}{4}\right] \quad nH$$

L = wire length

r = wire radius

unit = inches

General Measurement Procedure

Xilinx uses the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements. The main components of a TDR setup includes: a digitizing sampling oscilloscope, a fast rise time step generator (<17 ps), a device-under-test (DUT) interface, and an impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

Package and Fixture Preparation Before performing the measurements, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements. The mechanical sample for all inductance (self and mutual) measurements are finished units with all leads shorted to the internal ground. For packages without an internal ground (i.e., QFP, PLCC, etc.) the die-paddle is used instead. The mechanical sample for all capacitance (self and mutual) measurements are finished units with all internal leads floating. The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe/DUT reflection. It also provides small ground loop to minimize ground inductance of the fixture.

Inductance and Capacitance Measurement Procedure For inductance measurements, a minimum of 25% and maximum of 50% of packages leads, including all leads that are adjacent to the lead(s) under test, are insulated from the DUT fixture ground. All other leads, except for the lead(s) under test, are grounded. This insulation forces the current to return through a low impedance path created on the opposite side of the package. It also eliminates mutual coupling from the neighboring leads. Self-inductance is measured by sending a fast risetime step waveform through the lead under test. The inductive reflection waveform through the lead and the bondwire is then obtained. This reflection waveform, which includes the inductance of the die-paddle (for QFP and PLCC-type packages) and parallel combination of leads in the return path, is the self-inductance. The parasitic effects of the return path are small enough to ignore in the context of this method. For mutual-inductance measurement, two adjacent leads are probed. A fast risetime step waveform is sent through one of the leads. The current travels through the lead/bondwire and returns by the path of the low-impedance ground. On the

adjacent "quiet" lead, a waveform is induced due to mutual coupling. This waveform is measured as the mutual inductance.

For capacitance measurements, all external leads except for the lead(s) under test are grounded to the DUT fixture. For QFP, PLCC, and Power Quad-type of packages, the die-paddle and the heat slug are left floating. Self-capacitance is measured by sending a fast risetime step waveform through the lead under test. The reflection waveform from the lead, which includes the sum of all capacitive coupling with respect to the lead under test, is then measured. Appropriately, the self-capacitance can also be called the "bulk" capacitance since the measured value includes the capacitance between the lead under test and all surrounding metal, including the ground plane and the heat slug. For mutual-capacitance measurement, two adjacent leads are probed. An incident waveform is sent through one lead, and the induced waveform on the neighboring lead is measured as the mutual capacitance.

In order to de-embed the electrical parasitics of the DUT fixture and the measuring probes, the short and the open compensation waveforms are also measured after each package measurement. This procedure compensates the DUT fixture to the very tip of the probes.

Inductance and Capacitance Model Extraction All measured reflection waveforms are downloaded to a PC running the analysis software for package parasitic model extraction. The software uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

Data Acquisition and Package Electrical Database

Xilinx acquires electrical parasitic data only on the longest and the shortest lead/traces of the package. This provides the best and the worst case for each package type (defined by package design, lead/ball count, pad size, and vendor). For convenience, the corner interconnects are usually selected as the longest interconnect, while the center interconnects are usually selected as the shortest.

For symmetrical quad packages, all four sides of the package are measured and averaged. Three to five samples are usually measured for accuracy and continuity purposes. The average of these samples is then kept as the official measured parasitic data of that package type in the database.

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