DataSourceCD Q1-2003: Xilinx Packaging and Thermal Characteristics

Component Mass (Weight) by Package Type

Package	Description	JEDEC Outline#	Xilinx #	Mass (g)
BF957	957 Ball-Flip Chip BGA 40x40 Body (1.27mm Pitch)	MS-034-BAU-1 (Depopulated)	OBG0036	18.49
BG225	Molded BGA 27mm Full Matrix	MO-151-CAL	OBG0001	2.2
BG256	Molded BGA 27mm SQ	MO-151-CAL	OBG0011	2.2
BG352	SuperBGA - 35 x 35mm Peripheral	MO-151-BAR	OBG0008	7.1
BG432	SuperBGA - 40 x 405mm Peripheral	MO-151-BAU	OBG0009	9.1
BG492	Molded BGA - 35mm - 1.27mm Pitch	MO-151-BAR	OBG0026	5.0
BG560	SuperBGA - 42.5 x 42.5mm SQ	MO-151-BAV	OBG0010	11.5
BG575	575 BGA 31 x 31mm Body (1.27mm Pitch)	MS-034-BAN-1 (Depopulated)	0BG0039	4.58
BG728	728 BGA 35 X 35mm BodyY (1.27mm Pitch)	MS-034-BAR-1	OBG0030	6.2
CB100	NCTB Top Braze 3K / 4K VER	MO-113-AD(3)	OCQ0008 / OCQ0006	10.8
CB164	NCTB Top Braze 3K / 4K VER	MO-113-AA-AD(3)	OCQ0003 / OCQ0007	11.5
CB196	NCTB Top Braze 4K VER	MO-113-AB-AD(3)	OCQ0005	15.3
CB228	NCTB Top Braze 4K VER	MO-113-AD(3)	OCQ0012	17.6
CG1156	Ceramic HiTCE BGA - 35sq. 1.0mm	MO-151	OBG0031	0.0
CP56	CSP 56 BGA - 6mm (0.5 pitch)	N/A	OBG0029	0.0
CS48	CSP 48 BGA - 7mm (0.8 pitch)	MO-195	OBG0012	0.2
CS144	CSP 144 BGA - 12mm (0.8 pitch)	MO-205-BE	OBG0015	0.3
CS280	CSP 280 BGA - 16mm (0.8 pitch)	MO-205-AH	OBG0024	0.0
DD8	.300 Cerdip Package	MO-03-AA	OPD0005	1.1
FF896	896 BallL - Flip Chip BGA 31 X 31mm Body (1.0mm Pitch)	MS-034-AAN-1	OBG0032	10.7
FF1152	1152 BallL - Flip Chip BGA 35 X 35mm Body (1.0mm Pitch)	MS-034-AAR-1 (depopulated)	OBG0033	14.24
FF1517	1517 BallL - Flip Chip BGA 40 X 40mm Body (1.0mm Pitch)	MS-034-AAU-1 (depopulated)	OBG0034	18.53
FG256	Fine Pitch BGA 17 x 17 mm, 1.0 mm ball pitch	MO-151-AAF-1	OBG0021	0.8
FG324	Molded BGA 23 mm - 1.0 mm Pitch	MO-151-AAJ	OBG0013	2.2
FG456	Fine Pitch BGA 23 x 23 mm, 1.0 mm ball pitch	MO-151-AAJ-1	OBG0019	2.1
FG556	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0020	3.92
FG676	Fine Pitch BGA 27 x 27 mm, 1.0 mm ball pitch	MO-151-AAL-1	OBG0018	3.3
FG680	Fine Pitch BGA 40 x 70 mm, 1.0 mm ball pitch	MO-151-AAU-1	OBG0022	10.3
FG860	Fine Pitch BGA 42.5 x 42.57 mm, 1.0 mm ball pitch	MS-034-AAV	OBG0025	13.8
FG900	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0027	4.0

© 2003 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and further disclaimers are as listed at http://www.xilinx.com/legal.htm. All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.

NOTICE OF DISCLAIMER: Xilinx is providing this design, code, or information "as is." By providing the design, code, or information as one possible implementation of this feature, application, or standard, Xilinx makes no representation that this implementation is free from any claims of infringement. You are responsible for obtaining any rights you may require for your implementation. Xilinx expressly disclaims any warranty whatsoever with respect to the adequacy of the implementation, including but not limited to any warranties or representations that this implementation is free from claims of infringement and any implied warranties of merchantability or fitness for a particular purpose.

Package	Description	JEDEC Outline#	Xilinx #	Mass (g)
FG1156	Fine Pitch BGA 35 x 35 mm, 1.0 mm ball pitch	MO-151-AAR-1	OBG0028	5.5
FT256	256 Thin PBGA 17 X 17mm Body (1.0mm Pitch)	MO-151	OBG0040	0.9
HQ160	Metric 28 x 28 - 0.65mm 1.6H/S Die Up	MO-108-DDI	OPQ0021	10.8
HQ208	Metric 28 x 28 - H/S Die Up	MO-143-FA1	OPQ0020	10.8
HQ240	Metric QFP 32 x 32 H/S Die Up	MO-143-GA	OPQ0019	15.0
HQ304	Metric QFP 40 x 40 - H/S Die Down	MO-143-JA	OPQ0014	26.2
MQ208	28 x 28 metal Quad EIAJ Outline	N/A	OPQ0006	6.1
MQ240	32 x 32 metal Quad EIAJ Outline	N/A	OPQ0011	8.0
PC20	PLCC Jedec MO-047	MO-047-AA	OPC0006	0.8
PC28	PLCC Jedec MO-047	MO-047-AB	OPC0001	1.1
PC44	PLCC Jedec MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC Jedec MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC Jedec MO-047	MO-047-AF	OPC0001	6.8
PD8	DIP .300 Standard	MO-001-AA	OPD0002	0.5
PD48	DIP .600 Standard	N/A	OPD0001	7.9
PG68	Ceramic PGA cavity Up 11 x 11	MO-067-AC	OPG0002	7.0
PG84	Ceramic PGA cavity Up 11 x 11	MO-067-AC	OPG0003	7.2
PG84	Windowed CPGA cavity Up 11 x 11	MO-067-AC	OPG0013	7.5
PG120	Ceramic PGA 13 x 13 Matrix	MO-067-AE	OPG0012	11.5
PG132	Ceramic PGA 14 x 14 Matrix	MO-067-AF	OPG0004	11.8
PG156	Ceramic PGA 16 x 16 Matrix	MO-067-AH	OPG0007	17.1
PG175	Ceramic PGA 16 x 16 Standard Version	MO-067-AH	OPG0009	17.7
PG191	Ceramic PGA 18 x 18 Standard - All	MO-067-AK	OPG0008	21.8
PG223	Ceramic PGA 18 x 18 Type	MO-067-AK	OPG0016	26.0
PG299	Ceramic PGA 20 x 20 Heatsink	MO-067-AK	OPG0022	37.5
PG299	Ceramic PGA 20 x 20 Type	MO-067-AK	OPG0015	29.8
PG411	Ceramic PGA 39 x 39 Stagger	MO-128-AM	OPG0019	36.7
PG475	Ceramic PGA 41 x 41 Stagger	MO-128-AM	OPG0023	39.5
PG559	Ceramic PGA 43 x 43	MO-128	OPG0025	44.5
PP132	Plastic PGA 14 x 14 Matrix	MO-83-AF	OPG0001	8.1
PP175	Plastic PGA 16 x 16 Buried	MO-83-AH	OPG0006	11.1
PQ44	EIAJ 10 x 10 x 2.0 QFP	MS-022-AB	OPQ0015	0.5
PQ100	EIAJ 14 x 20 QFP - 1.60 (default)	MO-108-CG1	OPQ0013	1.6
PQ100	EIAJ 14 x 20 QFP - 1.80 (not used)	EIAJ-Old	OPQ0016	1.6
PQ100	EIAJ 14 x 20 QFP - 1.95 (old version)	MO-108-CC2	OPQ0013	1.6
PQ160	EIAJ 28 x 28 0.65mm 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28 x 28 0.5mm 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 x 32 0.5mm	MO-143-GA	OPQ0010	7.1
PQ304	Metric QFP 40 x 40 - H/S Die Down	MO-143-JA	OPQ0014	26.2
SO8	Version 1 - 0.150/50 mil	Mo-150	OPD0006	0.1
SO20	300 mil SOIC	MS-1-3	OPD0009	0.5
SO24	300 mil SOIC	MS-113	OPD0010	0.6
TQ100	Thin QFP 1.4mm thick	MS-026-BDE	OPQ0004	0.7

Package	Description	JEDEC Outline#	Xilinx #	Mass (g)
TQ128	Thin QFP 1.4mm thick - RECT	MS-026-BHB	OPQ0028	0.8
TQ144	Thin QFP 1.4mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	Thin QFP 1.4mm thick	MS-026-BGA	OPQ0008	1.9
VO8	Thin SOIC - II	N/A	OPQ0007	0.1
VQ44	Thin QFP 1.0 thick	MS-026-AED	OPQ0017	0.4
VQ64	THIN QFP 1.0 thick	MS-026-ACD	OPQ0009	0.5
VQ100	Thin QFP 1.0 thick	MS-026-AED	OPQ0012	0.6
WC44	Jedec Windowed Cerquad	MO-087	QCQ0004	2.9
WC84	Windowed Cerquad	MO-087	QCQ0010	11

Notes:

1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.
2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.
3. Tie-bar details are specific to Xilinx package. Lead width minimum is 0.056".

-- START HERE page --