DataSourceCD Q1-2003: Xilinx Packaging and Thermal Characteristics
Package Information

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Introduction to Xilinx Packaging

Electronic packages are interconnect housing for semiconductor devices. The major functions of the electronic packages are to provide electrical interconnections between the IC and the board and to efficiently remove heat generated by the device.

Feature sizes are constantly shrinking, resulting in increased number of transistors being packed into the device. Today's submicron technology is also enabling large scale functional integration and moving toward system on a chip solution. In order to keep pace with these new advancements in silicon technologies, semiconductor packages have also evolved to provide improved device functionality and performance.

Feature sizes at the device level is driving package feature sizes down to the design rules of the early transistors. To meet these demands, electronic packages must be flexible to address high pin counts, reduced pitch and form factor requirements. At the same time, packages must be reliable and cost effective.

Packaging Technology at Xilinx

At Xilinx, a wide range of leaded as well as array packages have been developed to meet the design/performance requirements of today's advanced IC devices. Array package families such as standard overmolded PBGAs, thermally enhanced Cavity down BGAs, and small form factor CSPs(Chip Scale Packages) are offered to address the issues of pin counts/density requirements while offering superior electrical performance as compared to their leaded counterparts.

Package Technology Briefs

Cavity Up BGAs
CSPs
Cavity-Down BGAs
Flip Chip BGAs

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These packages have a lead spacing of 0.5 mm, 0.65 mm, or 0.8 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters. (See Table 1 for package dimensions.)

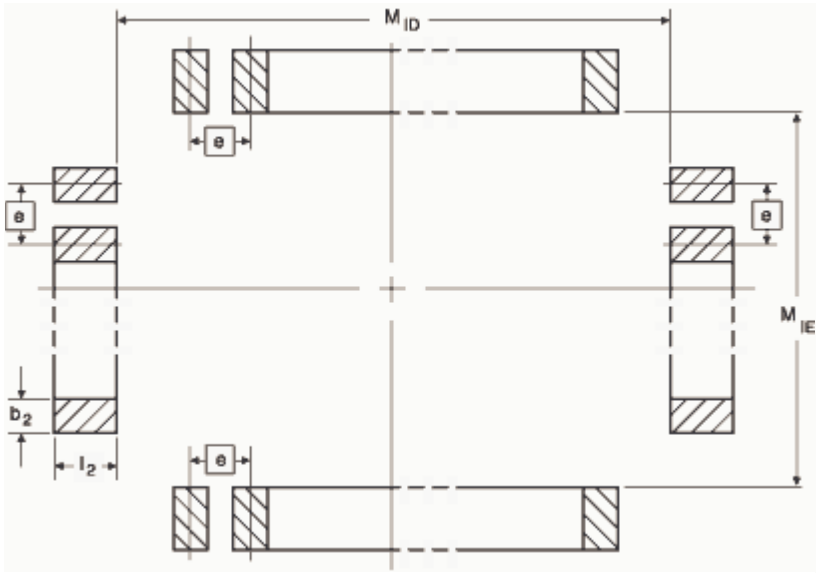

Figure 1: EIA Standard Board Layout of Soldered Pads for QFP Devices

Table 1: **Dimensions for Xilinx Quad Flat Packs(1)**

Dim.	VQ44	VQ64	PQ100	HQ160 PQ160	HQ208 PQ208	VQ100 TQ100	TQ144	TQ176	HQ240 PQ240	HQ304
MID	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
MIE	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
E	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
B2	0.4-0.6	0.3-0.4	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4
I2	1.60	1.60	1.80(2)	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes:
1. Dimensions in millimeters.
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

Suggested Board Layout of Soldered Pads for BGA Packages

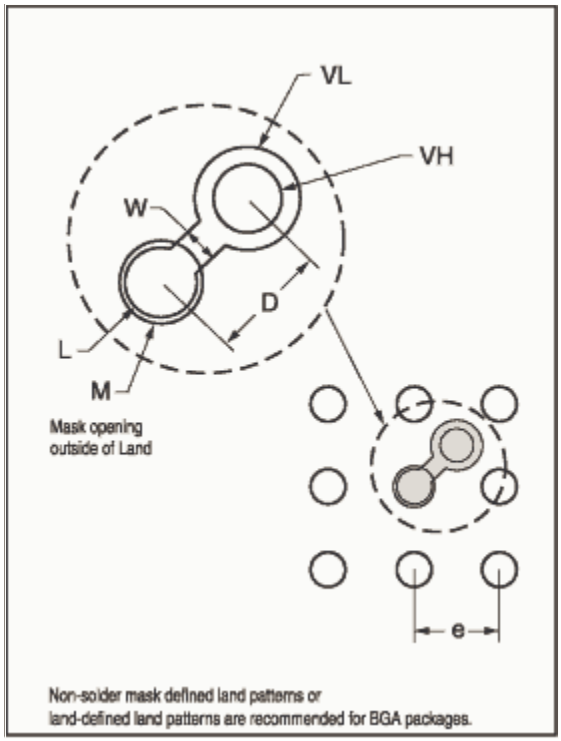

Figure 2: **Suggested Board Layout of Soldered Pads for BGA Packages(1)**

Table 2: **Recommended PCB Design Rules**

	FG256 / FT256	FG456	FG676	FG680	FG860	FG900	FG1156	FF896	FF1152	FF1517
Component land Pad Diameter (SMD)(2)	0.45 / 0.40	0.45	0.45	0.50	0.50	0.45	0.45	0.48	0.48	0.48
Solder Land (L) Diameter	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.45	0.45	0.45
Opening in Solder Mask (M) Diameter 0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.55	0.55	0.55	0.55
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land (VL) Diameter	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
Through Hole (VH) Diameter	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300

Table 2: **Recommended PCB Design Rules *(Continued)***

	FG256 / FT256	FG456	FG676	FG680	FG860	FG900	FG1156	FF896	FF1152	FF1517
Pad Array	Full	Full	Full	Full	Full	Full	Full	Full	Full	
Matrix or External Row	16 x 16	22 x 22	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34	30 x 30	34 x 34	39 x 39
Periphery Rows -	-	7(3)	-	5	6	-	-	-	-	-

Table 3: **Recommended PCB Design Rules (continued)**

	BG225	BG256	BG352	BG432	BG560	BG575	BG728	BF957	CS144	CP56
Component land Pad Diameter (SMD)(2)	0.63	0.63	0.63	0.63	0.63	0.61	0.61	0.61	0.35	0.30
Solder Land (L) Diameter	0.58	0.58	0.58	0.58	0.58	0.56	0.56	0.56	0.33	0.27
Opening in Solder Mask (M) Diameter 0.50	0.68	0.68	0.68	0.68	0.68	0.66	0.66	0.66	0.44	0.35
Solder (Ball) Land Pitch (e)	1.50	1.27	1.27	1.27	1.27	1.27	1.27	1.27	0.80	0.50
Line Width Between Via and Land (w)	0.300	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.13	0.13
Distance Between Via and Land (D)	1.06	0.90	0.90	0.90	0.90	0.90	0.90	0.90	0.56	-
Via Land (VL) Diameter	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.51	0.51
Through Hole (VH) Diameter	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.250	0.250
Pad Array	Full	-	-	-	-	Full	Full	Full	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	24 x 24	27 x 27	31 x 31	13 x 13	10 x 10
Periphery Rows -	-	4	4	4	5	-	-	-	4	1

Notes:

1. 3x3 matrix for illustration only, one land pad shown with via connection.
2. Component land pad diameter refers to the pad opening on the component side (solder mask defined).
3. FG456 package has solder balls in the center in addition to periphery rows of balls.

Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins), copper based BGA packages, and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air. More information on Xilinx's "Cavity Up" packages and "Cavity Down" packages can be found in the Packaging Technology Briefs.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP)

packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Pressure Handling Capacity

For the Flipchip BGA that has been surface mounted, a direct compressive (non varying) force applied NORMALLY to the lid with a tool head that coincides with the lid or is slightly bigger will not cause any damage to the flipchip balls or or external balls provided the force does not exceed 3.0 grams per external ball and the device and board are supported to prevent any flexing or bowing. Forces greater than this may work, however if the forces will exceed this limit, a careful finite element analysis will be in order.

The PC board needs to be properly supported to prevent any flexing resulting from such a force. Any bowing resulting from such a force can likely damage the package to board connections. It is suggested that any complicated mounting arrangement needs to be modeled with respect to the thermal stresses that can result from the heating of the device.

Clockwise or Counter-clockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

Table 4: **Summary of Thermal Resistance for Packages**

Package Code	$Theta_{JA}$ Still Air (Max) °C/Watt	$Theta_{JA}$ Still Air (Typ) °C/Watt	$Theta_{JA}$ Still Air (Min) °C/Watt	$Theta_{JA}$ 250 LFM (Typ) °C/Watt	$Theta_{JA}$ 500 LFM (Typ) °C/Watt	$Theta_{JA}$ 750 LFM (Typ) °C/Watt	$Theta_{JC}$ (Typ) °C/Watt	Comments
BF957	11.2	10.9	10.6	6.8	5.4	4.6	1.1	JESD: 4L/2P-SMT Simulation
BG225	37.2	30 .3	23.9	21.9	19.3	18.5	3.6	SEMI: 4L/2P-SMT
BG256	38.8	27.0	21.2	19.5	17.2	16.5	3.9	SEMI: 4L/2P-SMT
BG352	13.3	12.6	11.8	8.8	7.2	6.5	1.0	SEMI: 4L/2P-SMT
BG432	11.8	11.2	10.7	7.9	6.5	5.9	0.9	SEMI: 4L/2P-SMT
BG492	17.2	17.2	17.2	12.2	11.9	11.9	0.8	SEMI: 4L/2P-SMT
BG560	11.2	10.6	10.	7.4	6.1	5.6	0.8	SEMI: 4L/2P-SMT
BG575	16.9	15.8	14.7	12.1	11.4	11.0	2.8	JESD: 4L/2P-SMT Simulation
BG728	13.7	13.6	13.2	10.2	9.3	8.7	1.9	JESD: 4L/2P-SMT Simulation
CB100	48.8	41.9	38.5	25.4	19.7	17.8	5.8	SEMI: Socketed
CB164	29.8	2.7	25.0	16.6	12.4	10.6	3.7	SEMI: Socketed
CB196	26.2	25.0	23.8	15 .6	11.6	10.0	2.5	SEMI: Socketed
CB228	21.3	18.5	16.3	11.5	8.6	7.4	1.9	SEMI: Socketed
CC20	105.0	105.0	105.0	72.8	57.7	35.0	7.0	SEMI: Socketed

Table 4: **Summary of Thermal Resistance for Packages *(Continued)***

Package Code	$Theta_{JA}$ Still Air (Max) °C/Watt	$Theta_{JA}$ Still Air (Typ) °C/Watt	$Theta_{JA}$ Still Air (Min) °C/Watt	$Theta_{JA}$ 250 LFM (Typ) °C/Watt	$Theta_{JA}$ 500 LFM (Typ) °C/Watt	$Theta_{JA}$ 750 LFM (Typ) °C/Watt	$Theta_{JC}$ (Typ) °C/Watt	Comments
CC44	48.6	45.8	44.5	37.6	30.8	25.2	8.3	SEMI: Socketed
CD8	121.0	112.9	103.9	80.0	7.6	6.8	1.0	SEMI: Socketed
CD48	40.0	40.0	40.0	-	-	-	5.0	SEMI: Socketed
CG560	14.3	14.3	14.3	9.2	7.2	6.8	1.0	SEMI: Socketed
CG1156	10.7	10.7	10.7	8.0	7.6	6.8	1.0	JESD: 4L/2P-SMT Simulation
CP56	65 .0	65.0	65.0	-	-	-	15 .0	Estimated
CP132	62.3	67.4	72.4	62.8	60.4	58.5	13.4	JESD: 4L/2P-SMT Simulation
CS48	45.0	45.0	45.0	-	-	-	5.0	Estimated
CS144	65.0	35.7	34.0	25.9	23.9	23.2	2.5	Estimated
CS280	30.5	30.5	30.5	25.0	23.1	22.2	0.8	Estimated
DD8	115.9	109.3	94.0	89.8	73.5	60.2	8.3	Socketed
FF896	11.8	11.8	11.8	8.2	6.7	5.9	1.1	JESD: 4L/2P-SMT Simulation
FF1152	11.9	11.7	11.4	7.6	6.1	5.2	1.1	JESD: 4L/2P-SMT Simulation
FF1517	10.5	10.5	10.5	6.5	5.1	4.4	1.1	JESD: 4L/2P-SMT Simulation
FG256	33.6	25.1	18.4	21.2	19.7	19.1	3.9	SEMI: 4L/2P-SMT
FG324	29.4	26.0	21.1	19.3	17.2	16.5	3.4	SEMI: 4L/2P-SMT
FG456	23.5	19.6	16.5	15.5	14.1	13.6	2.2	SEMI: 4L/2P-SMT
FG556	13.7	13.6	13.5	9.7	9.4	9.4	2.1	SEMI: 4L/2P-SMT
FG676	16.7	16.6	16.6	13.2	12.0	11.5	2.0	SEMI: 4L/2P-SMT
FG680	11.1	10.8	10.4	7.5	6.2	5.6	0.9	SEMI: 4L/2P-SMT
FG860	10.5	10.2	10.0	7.2	5.6	5.4	0.8	SEMI: 4L/2P-SMT
FG900	14.1	13.7	13.5	9.8	9.5	9.5	2.0	Estimated
FG1156	13.7	13.4	13.2	9.7	9.2	9.0	2.0	JESD: 4L/2P-SMT Simulation
FT256	34.6	30.9	27.5	26.2	24.4	23.7	4.3	SEMI: 4L/2P-SMT
HQ160	16.5	15.6	14.7	10.8	8.6	7.7	2.0	SEMI: 4L/2P-SMT
HQ208	16.7	15.8	14.4	10.9	8.7	7.8	2.1	SEMI: 4L/2P-SMT
HQ240	14.5	13.2	11.8	9.1	.37	6.5	1.5	SEMI: 4L/2P-SMT
HQ304	11.3	10.6	10.0	7.1	5.6	4.9	1.1	SEMI: 4L/2P-SMT
HT144	19.1	18.5	18.2	12.6	10.7	10.1	2.1	SEMI: 4L/2P-SMT
HT176	15.6	15.3	15.2	10.4	8.9	8.4	2.0	SEMI: 4L/2P-SMT
HT208	13.6	13.4	13.3	9.0	7.6	7.2	1.9	SEMI: 4L/2P-SMT
MQ208	18.4	17.9	17.4	14.0	12.6	11.9	1.3	SEMI: 4L/2P-SMT
MQ240	16.8	16.7	16.4	12.0	10.8	10.5	1.2	SEMI: 4L/2P-SMT
PC20	87.3	82.3	72.0	62.1	55.5	51.8	24.2	SEMI: 4L/2P-SMT
PC28	67.6	66.1	63.0	49.8	44.6	41.6	17.8	SEMI: Socketed
PC44	53.7	46.5	42.3	35.1	31.4	29.3	14.9	SEMI: Socketed

Table 4: **Summary of Thermal Resistance for Packages *(Continued)***

Package Code	$Theta_{JA}$ Still Air (Max) °C/Watt	$Theta_{JA}$ Still Air (Typ) °C/Watt	$Theta_{JA}$ Still Air (Min) °C/Watt	$Theta_{JA}$ 250 LFM (Typ) °C/Watt	$Theta_{JA}$ 500 LFM (Typ) °C/Watt	$Theta_{JA}$ 750 LFM (Typ) °C/Watt	$Theta_{JC}$ (Typ) °C/Watt	Comments
PC68	46.2	41.9	38.4	31.6	28.2	2.46	9.5	SEMI: Socketed
PC84	41.7	33.3	27.9	25.8	20.8	16.8	5.6	SEMI: Socketed
PD8	83.0	78.9	71.3	59.4	53.2	49.6	21.5	SEMI: Socketed
PD48	43.2	43.2	43.2	32.6	29.1	27.2	11.6	SEMI: Socketed
PG68	38.8	37.0	34.1	25.6	19.9	17.3	7.8	SEMI: Socketed
PG84	38.5	34.4	31.3	23.8	18.5	16.1	6.0	SEMI: Socketed
PG120	37.8	27.8	24.6	19.3	15.2	13.3	4.0	SEMI: Socketed
PG132	32.0	28.7	23.9	20.3	16.7	14.8	2.9	SEMI: Socketed
PG144	25.8	24.5	23.3	17.4	14.3	12.6	3.7	SEMI: Socketed
PG156	25.6	23.9	20.7	14.9	11.6	10.3	2.7	SEMI: Socketed
PG175	25.2	23.3	19.9	14.5	11.3	10.0	2.6	SEMI: Socketed
PG191	25.7	21.8	18.5	15.5	12.7	11.2	1.5	SEMI: Socketed
PG223	25.3	21.1	17.7	15.0	12.3	10.8	1.5	SEMI: Socketed
PG299	21.0	17.3	15.1	10.4	8.7	8.3	2.0	SEMI: Socketed
PG411	16.1	14.7	14.3	9.5	7.4	6.5	1.4	SEMI: Socketed
PG475	15.1	14.6	14.3	9.4	7.3	6.4	1.4	SEMI: Socketed
PG559	13.7	13.4	13.2	8.6	6.7	5.9	1.3	Estimated
PP132	35.4	34.4	32.8	23.5	17.9	17.1	6.1	SEMI: Socketed
PP175	29.5	28.9	28.0	19.0	15.0	13.0	2.5	SEMI: Socketed
PQ44	52.2	51.3	50.1	39.8	36.4	35.4	12.4	SEMI: 4L/2P-SMT
PQ100	35.0	33.5	32.0	29.5	27.6	26.6	5.6	SEMI: 4L/2P-SMT
PQ160	38.1	31.8	20.6	23.5	20.8	19.2	5.0	SEMI: 4L/2P-SMT
PQ208	36.9	30.4	18.9	22.4	19.8	18.4	4.8	SEMI: 4L/2P-SMT
PQ240	28.5	19.9	14.0	14.7	13.0	12.0	3.8	SEMI: 4L/2P-SMT
SO8	14.17	147.1	147.1	112.2	104.6	98.6	48.3	IEEE-(Ref)
SO16	106.0	106.0	106.0	-	-	-	47.0	Vendor data
SO20	86.0	86.0	86.0	65.4	61.1	57.6	36.0	Vendor data
SO24	80.0	80.0	80.0	60.8	56.8	53.6	28.0	Vendor data
TQ44	76.5	76.2	75.8	59.2	50.0	45.1	8.2	SEMI: 4L/2P-SMT
TQ100	39.5	31.8	30.6	25.9	24.0	23.5	7.5	SEMI: 4L/2P-SMT
TQ128	31.5	30.6	30.0	26.9	25.2	24.3	5.3	SEMI: 4L/2P-SMT
TQ144	57.6	33.5	29.8	26.1	22.3	20.9	5.5	SEMI: 4L/2P-SMT
TQ160	28.9	28.9	28.9	21.8	18.5	17.0	5.6	SEMI: 4L/2P-SMT
TQ176	29.7	28.1	26.7	21.3	18.0	16.5	5.3	SEMI: 4L/2P-SMT
VO8	160.0	160.0	160.0	137.6	129.6	123.2	60.0	Estimated
VQ24	76.0	76.0	76.0	57.8	54.0	50.9	28.0	Estimated
VQ44	46.9	42.2	38.9	35.2	32.8	32.1	8.2	SEMI: 4L/2P-SMT
VQ64	46.9	42.3	39.3	35.2	32.9	32.1	8.2	SEMI: 4L/2P-SMT
VQ100	53.2	38.8	32.4	32.3	30.1	29.3	9.3	SEMI:4L/2P-SMT

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