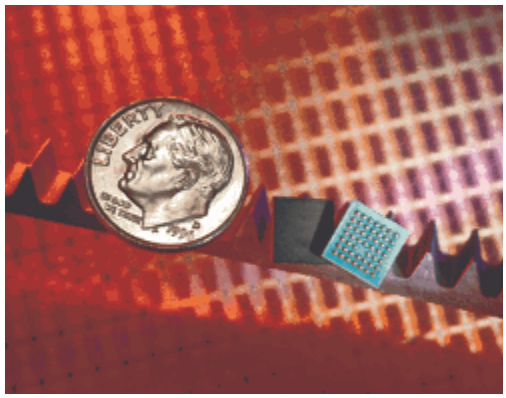
DataSourceCD Q1-2003: Xilinx Packaging and Thermal Characteristics
Chip Scale Packages

Introduction

Over the past years, Chip Scale Packages have emerged as a dominant packaging option for meeting the demands of miniturization while offering improved performance. Applications for Chip Scale Packages are targeted to portable and consumer products where real estate is of utmost importance, miniaturization is key, and power consumption/dissipation must be low. A Chip Scale Package is defined as any packages that fit the definition of being between 1 to 1.2 times the area of the die that the package contains while having a pitch of less than 1 mm.



According to Electronic Trend Publications in San Jose, the use of CSP packages is expected to grow by 108% per year over the next few years, reaching more than 6.1 billion units shipped worldwide by 2002. This dramatic growth is occurring because CSP packages bring you the benefits of:

- An extremely small form factor which significantly reduces board real estate for such applications as PMCMCIA cards, portable and wireless designs, and PC add-in cards
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other packages
- A very thin, light weight package
- Leveraging existing assembly and board level infrastructure

Package Construction

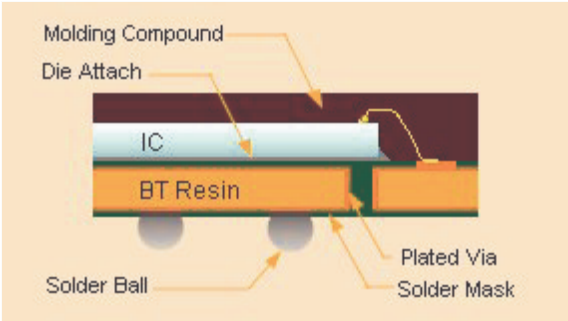


Figure 1: **Rigid BT-based Substrate**

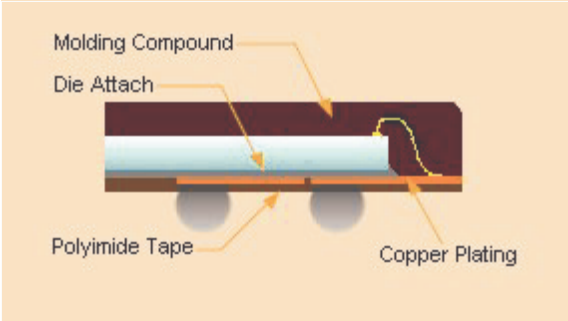


Figure 2: **Flex Based Tape Substrate**

Xilinx Chip Scale Packages

Although there are currently more than 50 different types of CSPs available in the market, Xilinx's CSP packages fall into two categories: (1) Flex-based substrates shown in Figure 1 and (2) Rigid BT-based substrates. Although, both types of meet the reliability requirement at the component and board level, BT-based substrate was chosen for the newer devices because of the large vendor base producing/supporting the BT-based substrates.

Xilinx is the first programmable logic company to offer Chip Scale Packages with a 0.8 mm pitch. This packaging solution is currently used for Xilinx's XC9500 series CPLD products that contain up to 100,000 system gates and for Virtex Series FPGAs with up to 200,000 system gates. By employing Xilinx's CSP packages, system designers could dramatically reduce board real estate and increase the I/O counts.

Table 1: **Xilinx CSP Offerings**

Package Code	Ball Count	Body Size (mm)	Ball Pitch (mm)	Substrate Type	Ball Pattern
CS48	48	7 x 7	0.80	2 Metal BT	7 x 7 matrix
CS144	144	12 x 12	0.80	Single metal layer tape	4 perimeter rows
CS280	280	16 x 16	0.80	Single metal layer tape	5 perimeter rows
CP56	56	6 x 6	0.50	2 Metal BT	2 perimeter rows
CP132	132	8 x 8	0.50	Single metal layer tape	3 perimeter rows

Package Drawings

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