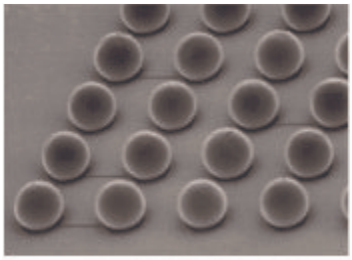
DataSourceCD Q1-2003: Xilinx Packaging and Thermal Characteristics
Flip Chip Packages

Introduction

Flip chip is a packaging interconnect technology that replaces peripheral bond pads of traditional wirebond interconnect technology with area array interconnect technology at the die/substrate interface. The bond pads are either redistributed on the surface of the die or in some very limited cases, they are directly dropped from the core of the die to the surface. Because of this inherent distribution of bond pads on the surface of the device, more bond pads and I/Os can be packed into the device.



Eutectic Bumps

Unlike traditional packaging technology in which the interconnection between the die and the substrate is made possible using wire, flip chip utilizes conductive bumps that are placed directly on the area array pads of the die surface. The area array pads contain wettable metallization for solders (either eutectic or high lead) where a controlled amount of solder is deposited either by plating or screen-printing. These parts are then reflowed to yield bumped dies with relatively uniform solder bumps over the surface of the device. The device is then flipped over and reflowed on a ceramic or organic laminate substrate. The solder material at molten stage is self-aligning and produces good joints even if the chips are placed offset to the substrates. After the die is soldered to the substrate, the gap (standoff) formed between the chip and the substrate is filled with an organic compound called underfill. The underfill is a type of epoxy that helps distribute stresses from these solder joints to the surface of the whole die and hence improve the reliability and fatigue performance of these solder joints.

This interconnect technology has emerged in applications related to high performance communications, networking and computer applications as well as in consumer applications where miniaturization, high I/Os, and good thermal performance are key attributes.

Cross-Section/Package Construction

Flip Chip Packages for high performance applications are built on high-density multi-layers organic laminate substrates. Since the flip chip bump pads are in area array configuration, it requires very fine lines and geometry on the substrates to be able to successfully route the signals from the die to the periphery of the substrates. Multilayer build up structures offers this layout flexibility on flip chip packages. The cross section of a Xilinx flip chip package with all essential elements is shown in Figure 1.

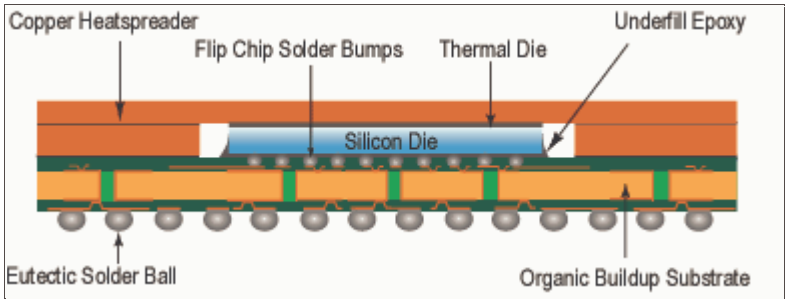


Figure 1: **Flip Chip Package**

Reliability

Temperature Cycles (0 - 100°C) >=1000 Cycles
Temp Cycle (-40 to 125°C) >=500 Cycles
THB 85°C/ 85 RH, Biased, 1000 hrs
Unbiased 85/85 85°C/85 RH, 1000 hrs
Moisture Sensitivity JEDEC Level 4

Benefits

If well implemented, Flip Chip Interconnect Technology offers the following benefits:

- Easy access to core power/ground, resulting in better electrical performance
- Excellent Thermal Performance (Direct heatsinking to backside of the die)
- Higher I/O density since bond pads are in area array format
- Higher frequency switching with better noise control

Table 1: **Xilinx Package Offering**

Package Code	Ball Count	Body Size (mm)	Ball Pitch (mm)	I/Os	Package Mass
BF957	957	40 x 40	1.27	684	18.49 grams
FF896	896	31 x 31	1.0	624	10.70 grams
FF672	672	27 x 27	1.0	416	4.4 grams
FF1152	1152	35 x 35	1.0	824	14.24 grams
FF1517	1517	40 x 40	1.0	1108	18.53 grams

For Application Notes on implementing Flip Chip BGA in the design and assembly processes, contact your local Xilinx Sales Representative

Package Drawings

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