Virtex-II Pro™ System Wake-Up Solutions

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The following table shows the revision history for this document.

	Version	Revision
03/08/02	1.0	Initial Xilinx release.

Contents

Chapter 1

Managing Hardware and Software Data with Virtex-II Pro Devices

Summary

The Virtex-II Pro Platform FPGA solution is a powerful system solution with numerous advanced features, including IBM PowerPC™ processors and Rocket I/O™ multi-gigabit transceiver blocks. The advanced features introduce new options that need to be considered when selecting a customized system wake-up solution. The system wake-up is the process necessary to bring the Virtex-II Pro devices to an operational stage for the system application and typically consists of two steps, configuring the FPGA logic and booting up the PowerPC processor for successful system operation.

The Virtex-II Pro PowerPC (PPC) microprocessor can be initialized as part of the system wake-up. This document briefly describes the various options available for system wake-up and highlights the two most efficient solutions for basic and advanced systems.

Overview

The following section gives an overview of the different methods available to configure the Virtex-II Pro device and to allow the PowerPC (PPC) to boot up and access memory for code storage and software execution.

The four system wake-up solutions for Virtex-II Pro Platform FPGAs are:

1. System ACE CF - CompactFlash-based configuration management
2. System ACE MPM - Parallel Flash-based Multi-Package Module
3. XILINX PROM - Serial Programmable Read Only Memory
4. External Non-volatile Memory - Flash, Read Only Memory, and other equivalent solutions.

Table 1-1 provides the available solutions for the Virtex-II Pro system wake-up.

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Table 1-1: **Solutions Available for Virtex-II Pro (XC2VP4, XC2VP7, XC2V20, XC2V50) System Wake-Up**

Solution	Density	Mode Support	Configuration Speed	Technology	I/O Voltage Tolerance	Feature Support
XC18Vxx PROM	Up to 4 Mb	Slave-Serial, SelectMAP	Up to 264 Mb/s	Flash	Down to 2.5V	Devices are reprogrammable (IEEE 1149.1 and IEEE 1532)
XC17Vxx PROM	Up to 16 Mb	Slave-Serial, SelectMAP (available for 17V08/17V16)	Up to 120 Mb/s	EPROM	3.3V	One Time Programmable (OTP)
System ACE MPM (Multi-Package Module) or System ACE SC (Soft Controller)	16 Mb to 64 Mb	Slave-Serial, SelectMAP	Select Map-152 Mb/s Slave Serial - 66 Mb/s	Parallel Flash-based solution	Down to 2.5V	• Native Flash Interface • Configuration management – multiple Design set support • Network Reconfigurable
System ACE CF CompactFlash	64 Mb up to 8 Gb	JTAG (IEEE 1149.1, IEEE 1532)	Up to 30 Mb/s	CompactFlash-based solution	Down to 2.5V	• MPU Interface (PPC405 compatible) • Configuration management – multiple Design set support • Network reconfigurable

Notes:

1. The XC2VP2 device which does not contain a CPU can be configured in the same manner as a Virtex-II device with a similar density.

System ACE CF (CompactFlash) Solution

The System ACE CF is a pre-engineered interface solution between a CompactFlash or one-inch Microdrive disk drive and a Virtex-II Pro FPGA. It features a built-in microprocessor interface and can support the configuration of multiple devices, boards, and bitstreams (multiple designs), as well as processor core initialization and software storage. This drop-in configuration solution delivers a dense, flexible, pre-engineered solution that reduces design time while supporting the complex needs of a microprocessor-based solution. For more information, see:
http://www.xilinx.com/isp/systemace/systemacecf.htm

When the System ACE CF solution is used with the Virtex-II Pro Platform FPGA, the wake-up sequence is as follows:

1. Configure the Virtex-II Pro FPGA logic from the CompactFlash (CF) via JTAG.
2. Transfer boot code from CompactFlash to Block SelectRAM™ (BRAM) or external RAM (DRAM or SRAM) via JTAG.
3. The PPC405 boots up from BRAM or RAM.
4. PPC405 can access the CompactFlash memory via the MPU port of the System ACE CF Controller for code storage and software execution. The PPC405 can also transfer software from the CompactFlash to BRAM, RAM, or a combination of both for faster execution.

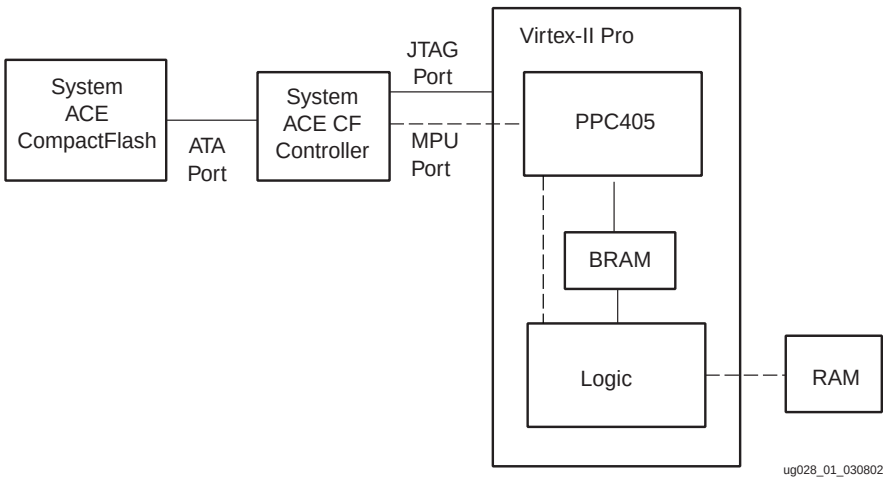


Figure 1-1: **System ACE CF Solution for Virtex-II Pro Wake-Up**

System ACE MPM/SC Solution

The System ACE MPM is a pre-engineered multi-package module and the System ACE SC is a functionally identical solution provided as a soft controller and not pre-packaged in a single module. Both solutions interface between an on-board industry standard Flash and a Virtex-II Pro FPGA. Both solutions feature a native flash (EPROM) and boundary scan interface and can support the configuration of multiple devices, board, and bitstreams (multiple designs), as well as processor core initialization. These drop-in configuration solutions provide high-performance bitstream delivery (Slave Serial and SelectMAP modes), while reducing design time for supporting the complex needs of a microprocessor-based solution. For more information, see:
http://www.xilinx.com/isp/systemace/systemacempm.htm

When the System ACE MPM is used with a Virtex-II Pro device (Figure 1-2), the wake up sequence is:

1. Configure the Virtex-II Pro FPGA logic and transfer boot code from MPM via SelectMap or Serial to BRAM.
2. The BRAM boots up the PPC405.
3. The PPC405 can access unused portions of ACE MPM via the MPM Flash Interface for code storage and software execution. The PPC405 can transfer software from ACE MPM to BRAM, RAM, or a combination of both for faster execution.

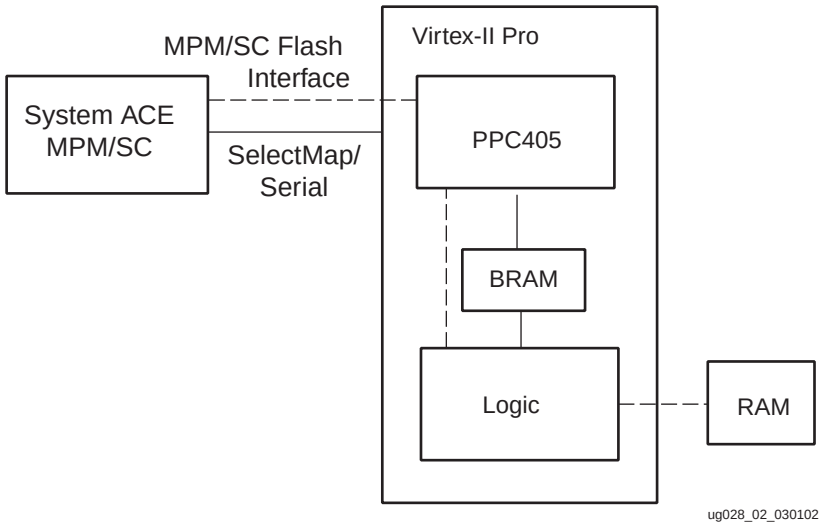


Figure 1-2: **Xilinx System ACE MPM/SC Solution for Virtex-II Pro Wake-Up**

Xilinx PROMs

Xilinx has developed a wide variety of configuration PROMs to provide an easy-to-use, high-performance programming solution. PROM products include In-System Programmable (ISP) as well as One-time Programmable (OTP) families in industry leading densities and packages.

When a Xilinx Configuration PROM is used with a Virtex-II Pro device (Figure 1-3), the wake up sequence is as follows:

1. Configure the FPGA portion of Virtex-II Pro device and transfer boot code from PROM via SelectMap or Serial to BRAM.
2. The BRAM boots up the PPC405.
3. The PPC405 can access the external non-volatile memory, like standard Flash, for code storage and software execution. The PPC405 can transfer software from the external non-volatile memory to BRAM, RAM, or a combination of both for faster execution.

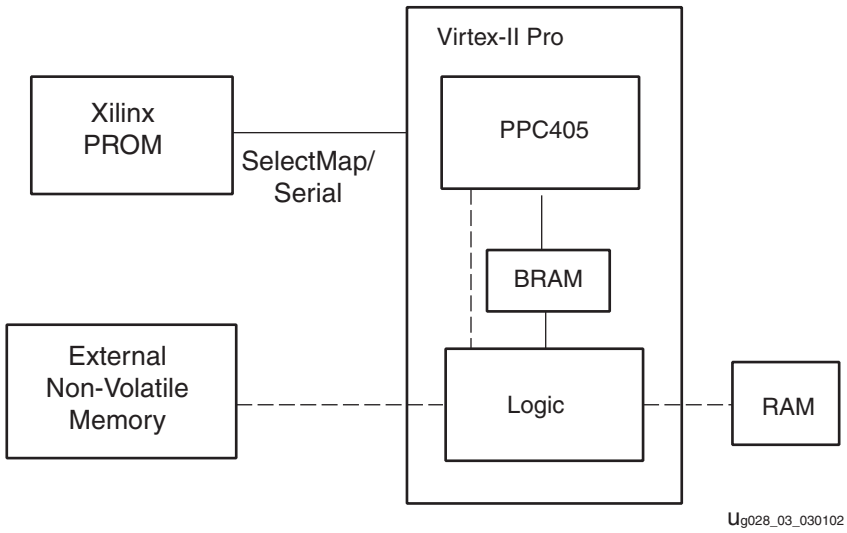


Figure 1-3: **Xilinx PROM Solution for Virtex-II Pro System Wake-Up**

External Non-Volatile Memory

External non-volatile memory can be used to configure a Virtex-II Pro device including Flash-based memory (such as standard Flash, CF cards, SD cards, etc.), as well as and hard disk drives. Using an external non-volatile memory requires a controller to configure the Virtex-II Pro device on wake-up. For the controller design, refer to the following application notes:

- **XAPP058** ("Xilinx In-System Programming Using an Embedded Microcontroller") or
- **XAPP079** ("Configuring Xilinx FPGAs Using an XC9500 CPLD and Parallel PROM")

The sequence of wake-up for a Virtex-II Pro device using an external non-volatile memory is as follows:

1. Configure the FPGA portion of the Virtex-II Pro device and transfer the boot code from external non-volatile memory to either BRAM or RAM.
2. Either BRAM or RAM boots up the PPC405.

The PPC405 can access external non-volatile memory, via the non-volatile memory interface, for code storage and software execution. The PPC405 can transfer software from the external non-volatile memory to BRAM, RAM, or a combination of both for faster execution.

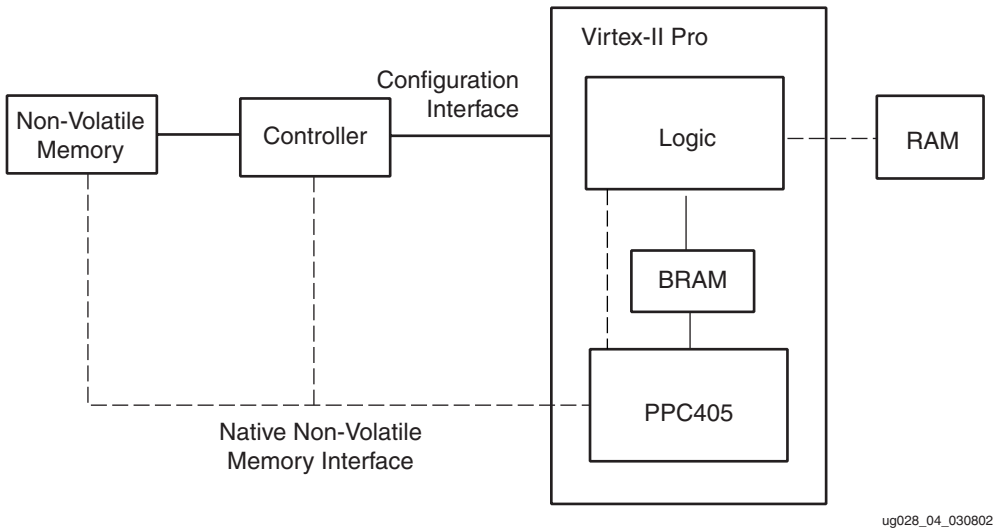


Figure 1-4: **Non-Volatile Memory Solution for Virtex-II Pro Wake-Up**

Chapter 2

Basic and Advanced Virtex-II Pro Wake-Up Solutions

Basic Virtex-II Pro Wake-Up Solution

Overview

The first method to be described is a well-known setup used with other Xilinx FPGA families. The setup requires very little external hardware and minimal connections. The only external device required for this setup is a Serial PROM storage device. The PROM is used to store the traditional configuration data for the Virtex-II Pro device.

The new level of complexity that must be addressed is the storage location of the Virtex-II Pro PowerPC™ boot-code. In this basic setup, the Virtex-II Pro FPGA Block SelectRAM (also referred to as BRAM) is utilized for the PPC boot code storage. The BRAM contents are loaded in the configuration data that is stored in the PROM, thereby, eliminating the need for an additional external RAM device to store the PPC contents.

Basic System Architecture

Figure 2-1 shows the connections to the Xilinx PROM required for the Master Serial configuration mode. Figure 2-1 also shows a simplified block diagram of the Virtex-II Pro device before configuration. In this setup, both the FPGA logic and BRAM load on configuration from the PROM and the PPC boot-ups from the BRAM.

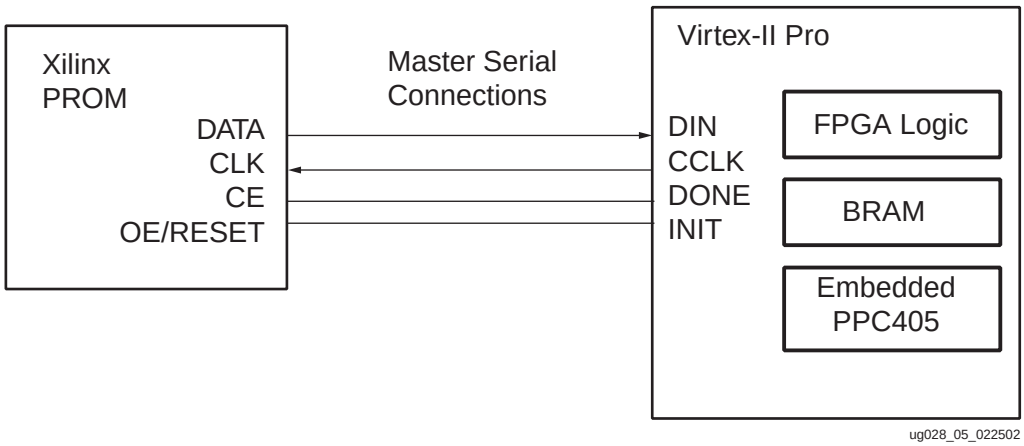


Figure 2-1: **Virtex-II Pro Basic System Wake-Up Solution**

Notes:

1. Other modes can also be used in a similar manner with additional hardware connections. Refer to the appropriate Xilinx PROM data sheet for guidelines and the required VCC / GND pullup / pulldown and optional connections.

This basic setup requires less hardware and external connections, but the trade-off is that the maximum storage space available for the boot-code and software is limited by the BRAM. Each available BRAM contains 18 Kbits. Table 2-1 displays the total amount of BRAM memory available for each member of the Virtex-II Pro family.

Table 2-1: **Available Virtex-II Pro Platform FPGA family BRAM and Microprocessor Cores**

Device	Columns	No. of PPC Cores	Total SelectRAM[1, 2] Memory		
			Blocks	In Kbits	In Bits
XC2VP4	4	1	28	504	516,096
XC2VP7	6	1	44	792	811,008
XC2VP20	8	2	88	1,584	1,622,016
XC2VP50	12	4	216	3,888	3,981,312

Notes:

1. The XC2VP2 does not contain PPC cores, so standard Virtex-II configuration solutions can be utilized.
2. 16 Kbits of the BRAM are available for direct interfacing with the Virtex-II Pro PPC.

Basic Solution Wake-Up Flow

Step 1

The Configuration stage is similar to other Virtex FPGA families. During this stage, the Virtex-II Pro device is powered on and completes three major phases:

- Clearing configuration memory
- Initialization
- Loading the bitstream.

Phase 1 and 2 simply prepare the device to receive the configuration data from the PROM. The FPGA's memory is cleared and the mode pin settings are sampled to determine the correct download mode. The appropriate pins become active to signify the loading of the configuration data. The loading of the bitstream defines the functional operation of the internal blocks, such as function look-up tables (LUTs), flip-flops (FFs), multiplexers, buffers, pullup / pulldown, slew rate, etc., and their interconnections.

Step 2

Device startup is a transition stage from the configuration mode to the normal programmed device operation. The startup sequence performs the following tasks:

- Release the DONE pin,
- Negate Global Tristate Signal (GTS) which activates all I / Os,

- Assert Global Write Enable (GWE) which allows all RAMS and flip-flops to change state, and finally,
- Assert End-Of-Startup (EOS) internal flag.

Step 3

At this stage, the FPGA has completed configuration and the PPC starts to execute code from the reset vector.

Basic Software Flow

This section describes the software flows necessary to generate a valid programming bitstream with the Virtex-II Pro PPC boot code. It also explains how to convert this bitstream into a PROM file required for this solution.

The flow through the Xilinx software tools to create a valid bitstream for the Virtex-II Pro device in general is the same as it is for any other Xilinx FPGA. The standard flow takes a design originating from HDL or schematic source code through the design front-end tools to create a standard netlist. This netlist is taken through the Xilinx implementation tool suite to physically map, then place and route the design into the desired Virtex-II Pro architecture. For further details on these software tools, refer to the on-line software manual, the *Development Systems Reference Guide*.

The deviation from the most standard flow for Xilinx FPGA families to a flow targeting the Virtex-II Pro device is in the setup required to allow the PPC to execute code from the BRAM. Two additional files are utilized to enable this functionality, the Block SelectRAM Memory Map file (.bmm) and the software code file (.elf). For additional information on the creation and usage of these two files, refer to the *Virtex-II Pro Developer's Kit* (Vols. 4 and 6.

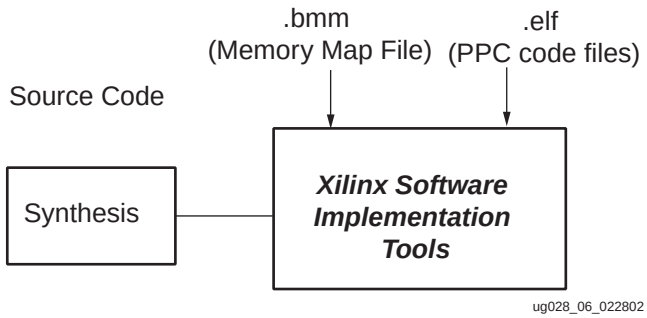


Figure 2-2: **Xilinx Tool Software Flow for Bitstream Generation with BRAM Initialization**

The last step in this software flow is the creation of the PROM file for programming the PROM. The PROM File is created in iMPACT software. The merged bitstream created from the Data2BRAM flow is used as the input file for iMPACT. The user targets the appropriate PROM density and .mcs format to create a serial formatted PROM file for the target solution. For a detailed flow, refer to the on-line software manual **iMPACT User Guide**.

Advanced Virtex-II Pro Wake-Up Solution

Overview

The second method discussed is for advanced users who want to take advantage of the configuration management and auxiliary storage capabilities of the System ACE CompactFlash (CF) solution.

The System ACE CF can manage up to eight separate designs for the Virtex-II Pro device. By default, one design is delivered at power-up to configure the Virtex-II Pro device and boot the PPC. On command, the System ACE CF can reconfigure the Virtex-II Pro with any of the eight possible designs stored in the CF.

The System ACE CF controller has a microprocessor (MPU) port that provides access to the CompactFlash. The Virtex-II Pro PPC can be connected to the System ACE CF MPU port to access data in the standard file structure within the CF.

The System ACE CF provides a centralized solution for system wake-up and the storage of auxiliary application code and data.

Advanced System Architecture

The advanced system contains the CompactFlash storage device, the System ACE CompactFlash controller, the Virtex-II Pro device, and external RAM. The System ACE CF controller acts as the master controller for the CompactFlash device. At power-up or on command, the System ACE CF controller extracts a selected configuration file from the CompactFlash and delivers the configuration data to the Virtex-II Pro device via the JTAG Test Access Port (TAP). The System ACE CF configuration process includes the delivery of both the FPGA fabric configuration bits and the initialization of the external RAM with the code and data. See below for details on the configuration delivery scheme.

The optional MPU port connection between the Virtex-II Pro device and the System ACE CF controller gives the PPC access to the CompactFlash file structure for reading and writing additional application code and data.

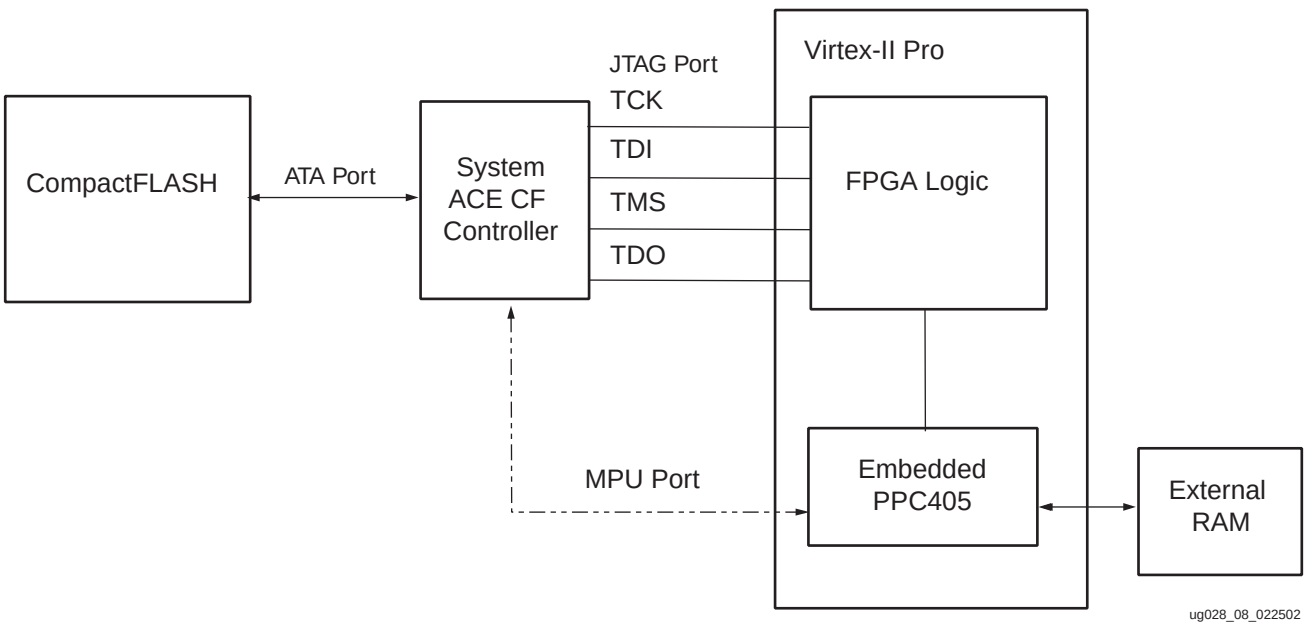
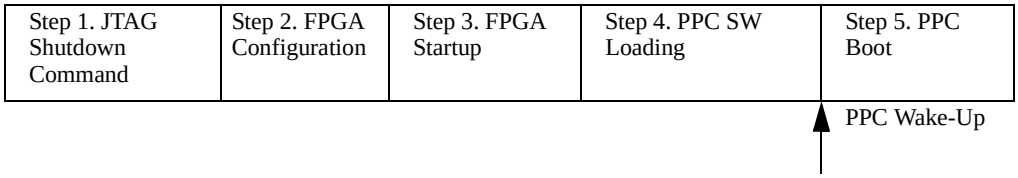


Figure 2-3: **Advanced System Wake-Up Solution**

Advanced Solution Wake-Up Flow

The Virtex-II Pro JTAG configuration flow is designed to support reconfiguration as well as initial configuration. Thus, the Virtex-II Pro wake-up flow begins with a JTAG shutdown command sequence that disables the active logic in the FPGA. The FPGA configuration and startup stages are the same as in the Basic setup. However, two extra stages are required to load the PPC code and wake up the PPC.



The five stages of the wake-up flow are accomplished through JTAG command sequences from the System ACE CF.

Step 1

The shutdown stage halts the PPC and disables the active logic in the FPGA. This stage prepares the FPGA to receive new configuration data. In the case of a reconfiguration, this stage eliminates the danger of contention between the new configuration and the previously loaded configuration.

Step 2

The configuration stage is similar to the other Virtex FPGA families' configuration stages. During this stage, the new bitstream is downloaded to the Virtex-II Pro device. The bitstream defines the functional operation of the internal logic blocks, the I/O pins, and the PPC interconnects to internal and peripheral devices, such as the external RAM.

Step 3

Startup is a transition stage from the configuration mode to the normal programmed device operation. The startup sequence performs the following tasks:

- Releases the DONE pin,
- Negates Global Tristate Signal (GTS) which activates all I/Os,
- Asserts Global Write Enable (GWE) which allows all RAMS and flip-flops to change state, and finally
- Assert End-Of-Startup (EOS) internal flag.

At the completion of this stage, the FPGA fabric is active including the PPC interconnects.

Step 4

The PPC software loading stage fills the external RAM with the PPC boot code and data through the PPC control logic.

Step 5

The PPC boot stage consists of the setting of the PPC program counter to the starting location of the boot code and releasing the PPC into its normal run mode.

Virtex-II Pro JTAG Test Access Port (TAP)

The JTAG TAP in the Virtex-II Pro device is tightly integrated with the FPGA configuration logic as well as the PPC control logic. The JTAG TAP and FPGA configuration logic integration allows the FPGA to be configured through the JTAG TAP. The JTAG TAP and PPC control logic integration allows the PPC to be controlled through the JTAG TAP.

JTAG control of the PPC is the key to the memory initialization and PPC wake-up scheme. The System ACE CF can instruct the PPC through the JTAG TAP to write the initial memory image. The System ACE CF can also instruct the PPC to start from a specific code location through the JTAG TAP.

Advanced Software Flow

A single System ACE CF configuration (.ace) file contains all the JTAG commands that are necessary to configure the Virtex-II Pro device and wake the PPC in the advanced system. The System ACE CF configuration file is created from two sources: the FPGA configuration bitstream (.bit) file and the PPC code and data (.elf) file. See the *Virtex-II Pro Developer's Kit* for descriptions of the flows that create the .bit and .elf files.

Because the target Virtex-II Pro device can be in a JTAG scan chain with an arbitrary number of JTAG devices, the System ACE CF configuration file preparation process must understand the JTAG scan chain layout. The System ACE CF solution delivers the configuration and code through serial JTAG vectors. These serial JTAG vectors are saved in an intermediate *de facto* standard Serial Vector Format (SVF) file.

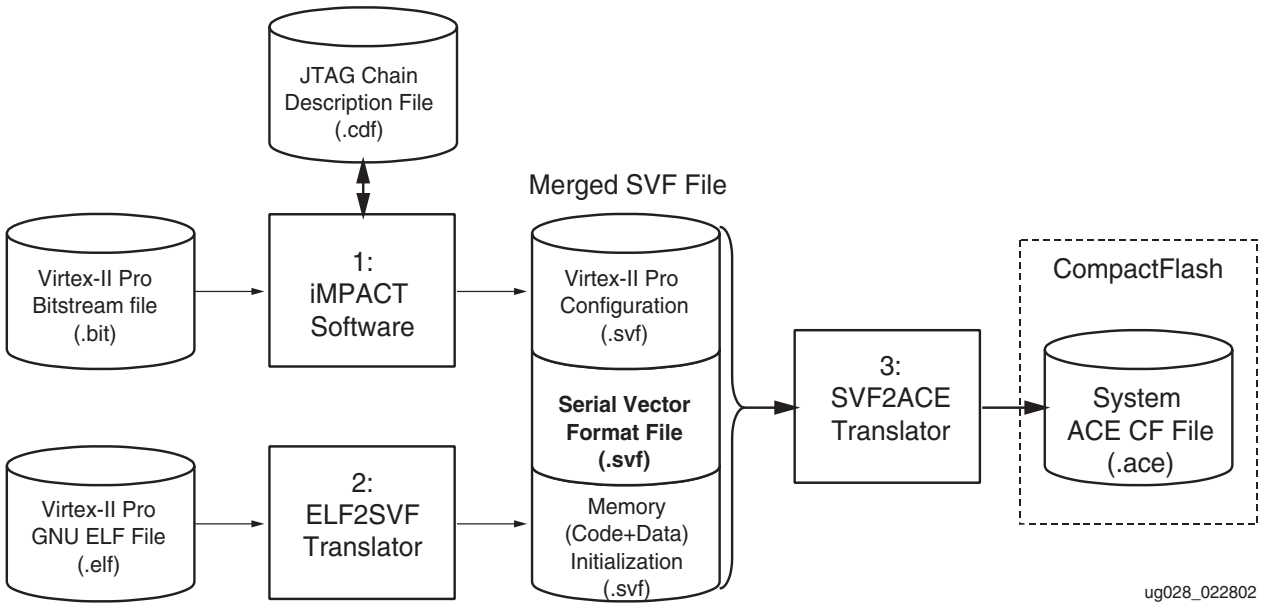


Figure 2-4: **Advanced Virtex-II Pro Software Flow**

Transformation of the .bit and .elf files into the unified .ace file requires three software steps:

Step 1

The iMPACT software generates the JTAG vectors for delivering the bitstream to the target Virtex-II Pro within the JTAG scan chain. The result is an SVF file with vectors to shut down, configure, and start up the FPGA logic. (See the *iMPACT User Guide* for detailed instructions on defining the JTAG scan chain and creating an SVF file to program the Virtex-II Pro device.)

Step 2

The ELF2SVF translates the PPC code and data (.elf) file into JTAG instructions for the PPC to fill the appropriate memory locations. In addition, the ELF2SVF translator appends JTAG instructions to preset the PPC program counter to the starting location of the boot code and to put the PPC into its run state with the preset program counter value. The resulting SVF is appended to the bitstream configuration SVF file.

Step 3

Convert the combined SVF file into the corresponding System ACE CompactFlash (ACE) file.

The ACE file is copied to the CompactFlash unit for system deployment. (See the *System ACE CompactFlash User Guide* for detailed instructions on the System ACE CompactFlash operation and file structure.)

In the target system, the System ACE CF controller executes the ACE file from the CompactFlash to configure and wake up the PPC.