Timing Analyzer Guide

Timing Analyzer Guide — 3.1i *Printed in U.S.A.*

About This Manual

This manual describes Xilinx's Timing Analyzer program, a graphical user interface tool that performs static timing analysis of an FPGA or CPLD design.

The illustrations and examples in this user guide are based on the UNIX workstation version of the Timing Analyzer software. In most cases there are only minor differences in the appearance of the Timing Analyzer on all supported platforms. Any significant differences between platforms are described in this user guide.

Before using this manual, you should be familiar with the operations that are common to all Xilinx software tools: how to bring up the system, select a tool for use, specify operations, and manage design data. These topics are covered in the *Development System Reference Guide*.

Manual Contents

This manual covers the following topics.

- Chapter 1, "Introduction," describes the Timing Analyzer's function, place in the Xilinx design flow, key features, inputs and outputs, and the architectures with which it works. It also outlines the basic procedure for using the tool.
- Chapter 2, "Getting Started,"describes how to access and exit the Timing Analyzer; how to use its menus, icons, Console window, dialog boxes, and filters; and how to use its online help facility.

- Chapter 3, “Timing Analysis,” describes the basic path types and explains how the Timing Analyzer solves some basic design analysis problems.
- Chapter 4, “Using the Timing Analyzer,” explains how to perform most of the Timing Analyzer’s major functions.
- “Glossary” defines all the terms that you should understand to use the Timing Analyzer effectively.

Additional Resources

For additional information, go to `http://support.xilinx.com`. The following table lists some of the resources you can access from this Web site. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging `http://support.xilinx.com/support/techsup/tutorials/index.htm`
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at `http://support.xilinx.com/support/searchtd.htm`
Application Notes	Descriptions of device-specific design techniques and approaches `http://support.xilinx.com/apps/appsweb.htm`
Data Book	Pages from *The Programmable Logic Data Book*, which contain device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging `http://support.xilinx.com/partinfo/databook.htm`
Xcell Journals	Quarterly journals for Xilinx programmable logic users `http://support.xilinx.com/xcell/xcell.htm`
Technical Tips	Latest news, design tips, and patch information for the Xilinx design environment `http://support.xilinx.com/support/techsup/journals/index.htm`

Conventions

This manual uses the following conventions. An example illustrates each convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: - 100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  ```
  rpt_del_net=
  ```

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *`design_name`*

  - References to other manuals

See the *Development System Reference Guide* for more information.

- Emphasis in text

  If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  edif2ngd *[option_name] design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  lowpwr ={**on**|**off**}

- A vertical bar " | " separates items in a list of choices.

  lowpwr ={**on**|**off**}

- A vertical ellipsis indicates repetitive material that has been omitted.

  ```
  IOB #1: Name = QOUT'
  IOB #2: Name = CLKIN'
  .
  .
  .
  ```

- A horizontal ellipsis "...." indicates that an item can be repeated one or more times.

  `allow block` *block_name loc1 loc2locn;*

Online Document

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.

- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

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Chapter 1

Introduction

The Timing Analyzer performs static timing analysis of an FPGA or CPLD design. The FPGA design must be mapped and can be partially or completely placed, routed or both. The CPLD design must be completely placed and routed. A static timing analysis is a point-to-point analysis of a design network. It does not include insertion of stimulus vectors.

The Timing Analyzer verifies that the delay along a given path or paths meets your specified timing requirements. It organizes and displays data that allows you to analyze the critical paths in your circuit, the cycle time of the circuit, the delay along any specified paths, and the paths with the greatest delay. It also provides a quick analysis of the effect of different speed grades on the same design.

The Timing Analyzer works with synchronous systems composed of flip-flops and combinatorial logic. In synchronous design, the Timing Analyzer takes into account all path delays, including clock-to-Q and setup requirements, while calculating the worst-case timing of the design. However, the Timing Analyzer does not perform setup and hold checks; you must use a simulation tool to perform these checks.

This chapter briefly describes the Timing Analyzer's function, place in the design flow, major features, inputs and outputs, and the architectures with which it works. It also outlines the basic procedure for using the tool. This chapter contains these sections.

- "Design Flow"
- "Inputs and Outputs"
- "Architectures"
- "Features"
- "Online Help"

Design Flow

You use the Timing Analyzer after mapping, placing, and routing, as shown in the following figure.

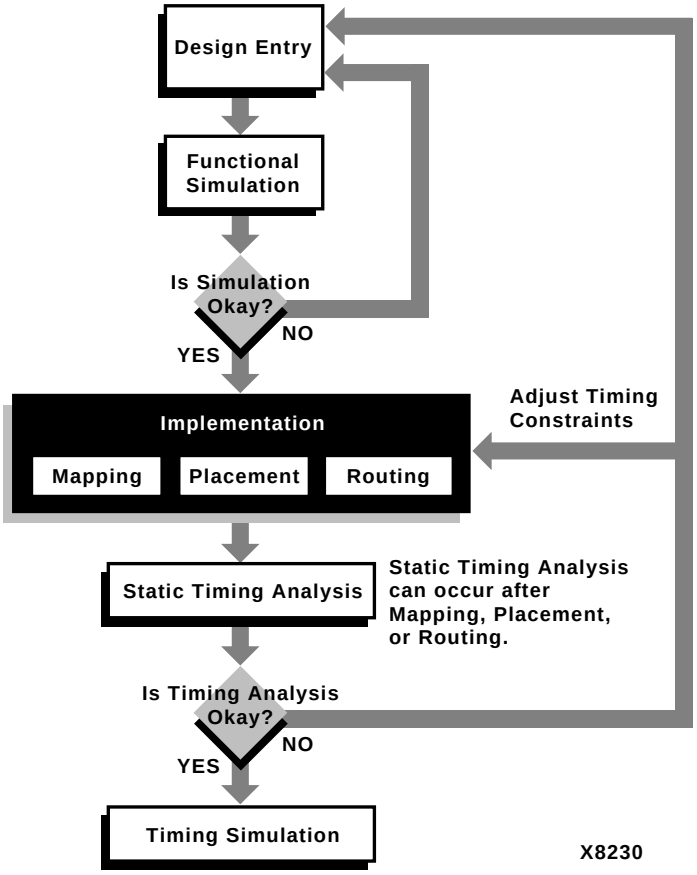


Figure 1-1 Timing Analyzer in the Design Flow

Inputs and Outputs

The Timing Analyzer has the following input and output capabilities:

- Accepts NCD design files and physical constraints files (PCF) output by the mapper for FPGAs
- Accepts VM6 (CPLD) design files output by the fitting software
- Loads macro files (XTM) as input
- Creates timing report (TWR) files as output
- Creates macro (XTM) files

Note Load PCF files from the Mapper only. When you load a design, the Timing Analyzer also loads the default PCF file if it is present. The default PCF file is the physical constraints file with the same name and located in the same directory as the NCD file. You can load a different PCF file after the design is loaded. The order of the timing constraints in the PCF file is reflected in the Timing Analyzer reports. CPLD physical constraints information is contained in the VM6 file itself.

Architectures

You can use the Timing Analyzer with the following Xilinx devices:

- Spartan™ / XL / -II
- Virtex™ / -E / -II
- XC9500™ / XL / XV
- XC4000™E / L / EX / XL / XV / XLA
- XC3000™A / L
- XC3100™A / L
- XC5200™

Features

The Timing Analyzer offers the following interface, report, filters, macro, and analysis interrupt features.

Interface

You can issue Timing Analyzer commands from the menus, toolbar, or Console window. You can also activate commands by running macros. The instructions in this user guide use only the menu commands or toolbar buttons. The equivalent command-line syntax is provided in the Timing Analyzer Online Help.

Reports

The Timing Analyzer can create the following reports.

- Timing Constraints Analysis report compares design performance to the timing constraints.
- Analyze Against Auto Generated Design Constraints Analysis report displays the results of analyzing the constraints specified in the constraints file for FPGAs. If no constraints are specified, this report displays the maximum clock frequencies for all clocks in the design and the worst-case timing for all clock paths. For CPLDs, it displays all external synchronous path delays which include: pad-to-pad (tPD), clock pad-to-output pad (tCO), setup-to-clock-at-the-pad (tSU), and internal clock-to-setup (tCYC) paths.
- Analyze Against User Specified Paths by Defining Endpoint Analysis report contains a detailed analysis of all specified paths and includes the worst-case path delays for all paths in the design. You can filter this report.

  Analyze Against User Specified Paths by Defining Clock and IO report generates the analysis report, for user specified Period, Timegroups of Pads, Offset in before constraints, and Offset out after constraints.
- Clocks report lists the names of all clocks in the design.
- Settings report lists the current settings set with commands in the Path Filters and Options menus.
- Query Nets report displays net delay information. (FPGA only)
- Query TimeGroups displays time group information. (FPGA only)

Path Filtering Commands

You can customize Timing Analyzer reports by specifying filters in the Filter Paths by Net tab accessed through the commands in the Analyze menu. The Reset Path Filters command resets the path filters to default settings. The Filter Paths by Net tab is included in all Analyze Against dialog boxes which have the following functionality:

- Analyze Against Timing Constraint Filters commands affect only the Timing Constraints Analysis and Analyze Against Auto Generated Design Constraints reports.
- Analyze Against User Specified Paths by Defining Endpoint Filters commands deal with specific paths whose starting points and ending points you can define. These commands apply to the Analyze Against User Specified Paths by Defining Endpoint reports.
- Common Filters commands exclude or include paths with specific nets and control path tracing. These commands apply to the Analyze Against Timing Constraints Analysis, Analyze Against Auto Generated Design Constraints Analysis, Analyze Gaussian User Specified Paths by Defining Endpoint Analysis and Gaussian User Specified Paths by Defining Clock and IO Timing Analysis reports.

Macros

You can create macros that execute multiple Timing Analyzer commands in one step. Macros are script files for running Timing Analyzer commands and options. The Console window records all the commands that you execute in any Timing Analyzer session. After entering the desired series of commands in this window, you can copy and paste the sequence into a macro document, save the macro document, and run it.

Analysis Interrupt

The commands in the Analyze menu have an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears. Clicking the button, the Esc key, or the Enter / Return key stops analysis. A report is not generated or displayed.

Online Help

The Timing Analyzer offers both context-sensitive help and a Help menu. See the “Obtaining Help” section of the “Getting Started” chapter for more information on the online help and instructions for accessing it.

Chapter 2

Getting Started

This chapter describes starting and exiting the Timing Analyzer, using menus, buttons, Console windows, dialog boxes, and online help. It contains these sections.

- "Starting the Timing Analyzer"
- "Timing Analyzer Window"
- "Console Window"
- "Dialog Boxes"
- "Basic Timing Analysis Procedure"
- "Obtaining Help"
- "Exiting the Timing Analyzer"

Starting the Timing Analyzer

The Timing Analyzer runs on PCs and workstations. On the PC, the graphical user interface is based on Microsoft Windows. On the workstation, the interface is based on OSF Motif.

You can start the Timing Analyzer from the Windows Program Manager, the Xilinx Design Manager, or the command line.

From the Design Manager

To start the Timing Analyzer from the Design Manager window (PC or workstation), click on the Timing Analyzer icon (shown in the following figure) or select **`Tools`** → **`Timing Analyzer`**.

Stand-Alone Tool

If you installed the Timing Analyzer as a stand-alone tool on a PC, click on the Timing Analyzer icon (shown in the previous figure) on the Windows desktop or select timingan.exe from the Windows 95 or Windows NT Start button.

From the Command Line

To start the Timing Analyzer from a UNIX command line, type the following command.

```
timingan
```

These are a number of variations for starting the Timing Analyzer from the command line.

- To run the tool as a background process, end the command with an ampersand (&).

  ```
  timingan &
  ```

- To start the Timing Analyzer and open an existing FPGA or CPLD design, type the following.

  ```
  timingan {design_name.ncd|design_name.vm6}
  ```

  For FPGA designs, if a physical constraints file (PCF) exists in the same directory as the design and has the same name, except for the extension, that design_name.pcf file is automatically opened.

- To start the tool, open an existing FPGA design and the corresponding physical constraints file, type the following. Physical constraints files only apply to FPGAs.

  ```
  timingan design_name.ncd -pcfpcf_file_name.pcf
  ```

- Use the –run option followed by a macro file name to run a macro. If a design and PCF file are specified on the command line also, the macro is run after the design and PCF file are loaded. The macro may contain an Exit command.

```
timingan design_name.ncd -pcfpcf_file_name.pcf
-run macro_name
```

- To start the tool and open a Timing Analyzer report in a Hierarchical Report viewing window, type the following.

  ```
  timingan filname.twr
  ```

- To start the tool and open a Timing Analyzer report in a text editor window, type the following.

  ```
  timingan filname
  ```

- To unload a default PCF file, use the -nopcf option.

Timing Analyzer Window

This section describes the Timing Analyzer's main window, menus, toolbar, and status bar. You can execute Timing Analyzer commands from the menus, toolbar, or the Console Window.

When you start the application, the Timing Analyzer window appears. The window contains pull-down menus, a toolbar at the top of the window, and a status bar at the bottom of the window. The menus are described in the "Menus" section.

Note The Edit menu is only enabled when a design, report, or macro file is open and is the active window. Also, most of the toolbar buttons are not enabled unless a file is open and active.

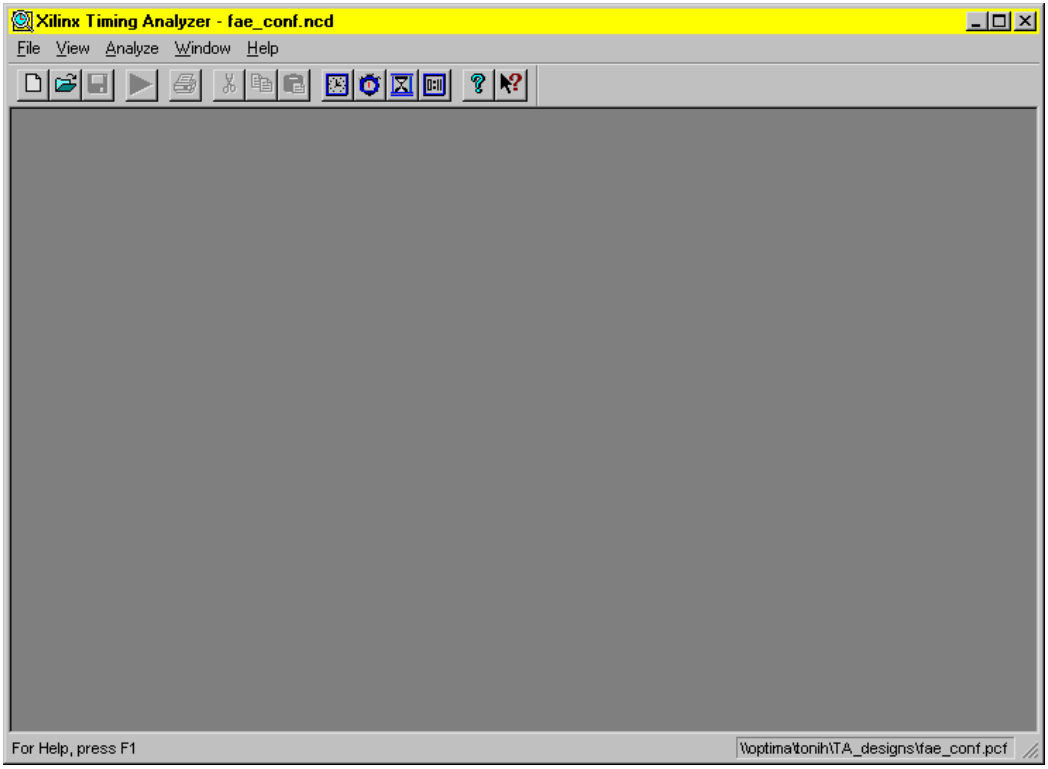


Figure 2-1 Timing Analyzer Window

The toolbar and status bar appear by default when you start the Timing Analyzer. You can hide them from view by selecting the Toolbar or the Status Bar commands, respectively, from the View menu.

Menus

Most of the Timing Analyzer commands are available in the pull-down menus. However, unless a design is loaded, most of the commands are disabled and not available. Certain commands and some command options are disabled and not available, depending whether the open design is an FPGA or a CPLD design.

You can select menu commands with the mouse or the keyboard. With the mouse, click the left mouse button on the desired command.

With the keyboard, press the Alt key and type in the letter underlined in the menu for that command. When you select a menu command with either method, a brief description of the command's function appears in the Status Bar at the bottom of the Timing Analyzer window.

For complete command descriptions, select **Help** → **Help** Topics or see the Timing Analyzer on-line help for more information.

Toolbar

The toolbar appears at the top of the window, just below the menu bar. The toolbar provides button access to frequently used commands in the menus. Textual labels for the buttons appear when you move the cursor arrow over a button. This feature is called a tool tip. A longer description also appears in the status bar. See the Timing Analyzer OnlineHelp for more information.

Status Bar

By default, the status bar appears at the bottom of the window. When you select a menu command, a brief description of the command's function appears in the status bar. As the Timing Analyzer processes, status messages are dynamically updated and displayed.

To hide or show the status bar, select **View** → **Status Bar**

Console Window

The Console window displays the sequence of commands that you have used in a Timing Analyzer session. It is primarily used for creating macros, but it has a command line field, in which you can type and execute keyboard commands. The Console window also contains a Show Command Status box that you can click on to display or hide status messages. For information on creating and using macros, see the "Using Macros" section of the "Using the Timing Analyzer" chapter.

Commands that you can enter in the Console window are described in the Timing Analyzer Online Help.

You can open the Console window by selecting **View** → **Console**.

Dialog Boxes

Many Timing Analyzer menu commands display dialog boxes in which you can enter information and set options. This section describes dialog box common fields, tabs within the Analysis dialog boxes, and how to use filters.

Common Fields

The fields shown in the following table are common to most dialog boxes.

Table 2-1 Common Dialog Box Fields

Dialog Box Field	Function
OK	Closes the dialog box and implements the intended action according to the settings in the dialog box
Cancel	Closes the dialog box without effecting any action
Help	Displays information on that particular dialog box

Analysis Dialog Tabs

Many of the dialog boxes in the Timing Analyzer feature menu tabs with grid based selection items, such as Analyze Against Timing Constraints in the next figure. You can select the various tabs that include all the filter settings and options that apply to that type of analysis.

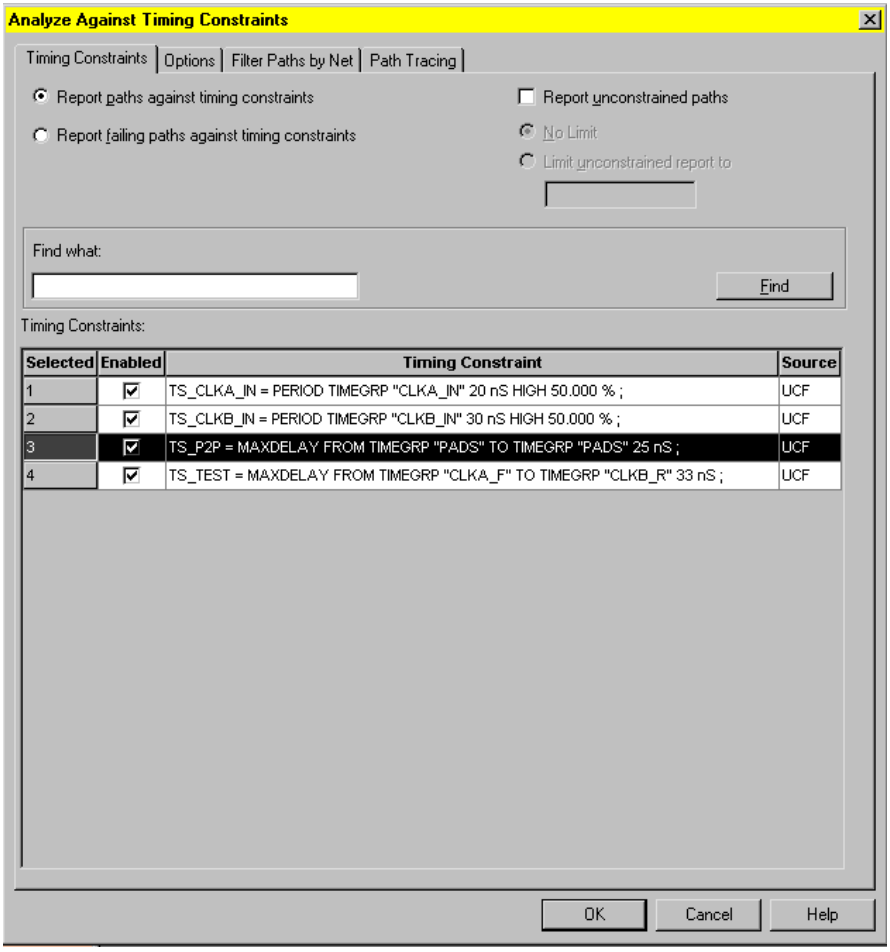


Figure 2-2 Tabs Within the Analyze Against Timing Constraints Dialog Box

Using Filters with Commands

To use filters with commands select **`File` →`Preferences`**, the Preference dialog appears. The following figure displays an example of the Preferences dialog box. User can select the Allow Wildcards (8,?) or the Exact string matches radio buttons to set the Find What search strings in all tab dialogs.

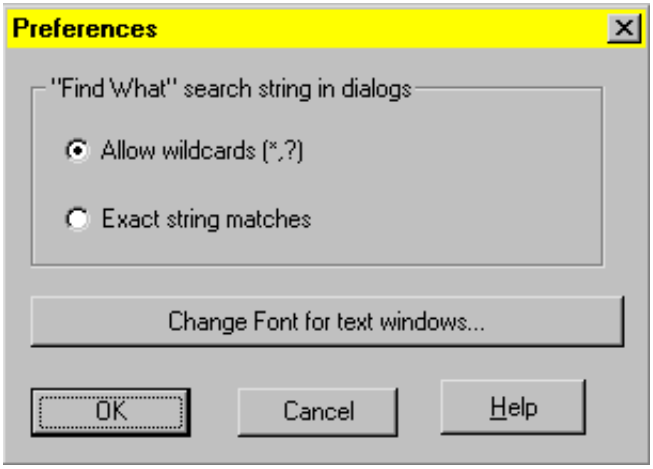


Figure 2-3 Preferences Dialog Box

Valid Inputs and Wildcards

In the find what (filter fields), you can enter a text string consisting of characters and wildcards.

- Characters can be any alphanumeric characters, text spaces, and the characters that appear on the top of the number keys on a keyboard. Alphabetic characters are case-sensitive. No control characters are permitted.
- A wildcard can be an asterisk (*), which can represent any number of characters, or a question mark (?), which represents a single character.

You cannot enter a range of characters in filter fields.

Matching Text Strings

The Timing Analyzer does not strictly match patterns; it matches entire text strings. It does not find a string if it is embedded in a larger string, unless you use wildcards. For example, it does not find $1N36 if it is embedded in ABC$1N36XYZ. However, if you searched for *$1N36*, it would find that string in ABC$1N36XYZ.

Basic Timing Analysis Procedure

The typical procedure for using the Timing Analyzer is as follows.

1. Open the Timing Analyzer and load your design.

   For FPGAs, if a physical constraints file (PCF) with the same name as your design exists in the directory, the Timing Analyzer also loads that file, by default. (The PCF file is generated when a design is mapped.)

2. If you are unfamiliar with the Timing Analyzer, explore its features. You can use the online help facility to help you with this process. To run the online help, select **`Help`** → **`Help Topics`**

3. You can optionally generate a report to obtain a basic overview of the design's timing before you begin to analyze it in detail. The Analyze Against Auto Generated Design Constraints Report provides that information. Choose the Analyze Against Auto Generated Design Constraints command from the Analyze menu to generate and display an Analyze Against Auto Generated Design Constraints Analysis report.

4. Select commands from the Analyze menu tabbed dialogs that include all the filter setting and options that apply to specify the kinds of reports you want to generate. These settings always appear when Analyze menus are chosen.

5. Select commands from the Edit menu to search or edit reports.

6. Select commands from the File menu to save or print reports.

7. Optionally, you can create macros comprising the commands just issued.

   These steps are described in more detail in the "Using the Timing Analyzer" chapter.

Obtaining Help

You can obtain help on the Timing Analyzer's commands and procedures by selecting commands in the Help menu, by selecting the Help button in the toolbar, by clicking the Help button in dialog boxes, or by pressing the F1 key. The Help button in the toolbar, the ones contained in some menu command dialog boxes, and the F1 key

provide context-sensitive help for what you click on or that dialog box, respectively.

Help Menu

The Help menu contains the following commands.

- Help Topics lists the online help topics available for the **Timing Analyzer**. From the opening screen, you can jump to command information or step-by-step instructions for using the **Timing Analyzer**. After you start the help, you can click the Contents button (first button in the top-left corner) in the Help window whenever you want to return to the help topics list.
- **About Timing Analyzer** displays a pop-up window that displays the version number of the **Timing Analyzer** software.

Context-Sensitive Help

You can obtain context-sensitive help on the **Timing Analyzer** by using the Help button in the toolbar or the **Help** button contained in many of the menu command dialog boxes. This section describes both methods of how to access the context-sensitive help.

Toolbar Button

To access context-sensitive help from the toolbar, follow this procedure.

1. Click on the Help button from the toolbar, shown in the following figure.

   The cursor changes to an arrow and question mark, like the button.

2. For help on menu commands, click (with the left mouse button) on the menu, then click the command in that menu or submenu. For help on toolbar buttons, click once on the particular button.

The Timing Analyzer displays information about the selected command or button.

Help Button in Dialog Boxes

Many of the dialog boxes associated with Timing Analyzer menu commands have a Help button. You can click on the button to obtain help on that dialog box. A window opens with the information.

F1 Key

Pressing the F1 key when the cursor is placed on a dialog box displays help for that dialog box.

Exiting the Timing Analyzer

To exit the **`Timing Analyzer`**, click **`File`** → **`Exit`** or type exit at the prompt in the Console window.

If you have unsaved reports open, a prompt box similar to that in the next figure appears.

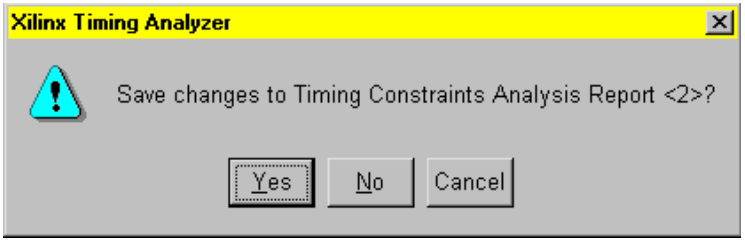


Figure 2-4 Exit Prompt Box

Click Yes to save the report, then follow the procedure described in the “Saving a Report” section of the “Using the Timing Analyzer” chapter.

You are prompted for confirmation before exiting, even if there is no unsaved data. However, if SetForce is on, an Exit command in a macro causes the Timing Analyzer to exit without asking for confirmation.

Chapter 3

Timing Analysis

This chapter explains some of the concepts involved in static timing analysis and how to use the Timing Analyzer to resolve key analysis issues.

Xilinx software tools support two different methodologies of implementing timing analysis. For FPGAs, timing is analyzed through user-defined constraints specified with Timing Analyzer commands and filters. The commands in the **`Analyze` → `Against Timing Constraints`** Filter Tab help you customize your analysis. See the Commands section of the Timing Analyzer Online Help and the *XILINX Software Conversion Guide from XACTstep v5.x.x to XACTstep vM1.x.x* for more information. CPLDs use system-defined paths for timing analysis. These paths are selected with commands in the Analysis dialog tabs found in the Analyze menu. See the Commands section of the Timing Analyzer Online Help for more information on these commands.

This chapter contains these main sections.

- "Basic Path Types"
- "Design Analysis Issues"

Basic Path Types

After you implement your design, you can use the Timing Analyzer to calculate your design's system performance, which is limited by seven basic types of timing paths. Each of these paths goes through a sequence of routing and logic. Because these path delays are affected by the results of the placement and routing that implement the design connectivity, these sequences can vary.

Before you read the Timing Analyzer reports, read the following sections for a description of the basic path types.

Clock to Setup

A clock-to-setup path starts at flip-flop clock inputs and ends at non-clock flip-flop register inputs, D or T, or the receiving flip-flop's tSU, where that pin has a setup requirement before a clocking signal. Along the way, it propagates through the flip-flop Q output and any number of levels of combinatorial logic. It includes the clock-to-Q delay of a flip-flop, the path delay from that flip-flop to the next flip-flop, and the setup requirement of the next flip-flop.

The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs. When these flip-flops are clocked by the same clock, the delay on this path is equivalent to the cycle time of the clock. The following figures show a clock-to-setup path which uses the same clock. Figure 3-2 also shows a timing diagram describing the path.

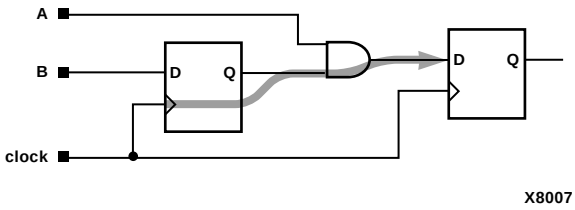


Figure 3-1 Clock-to-Setup Path

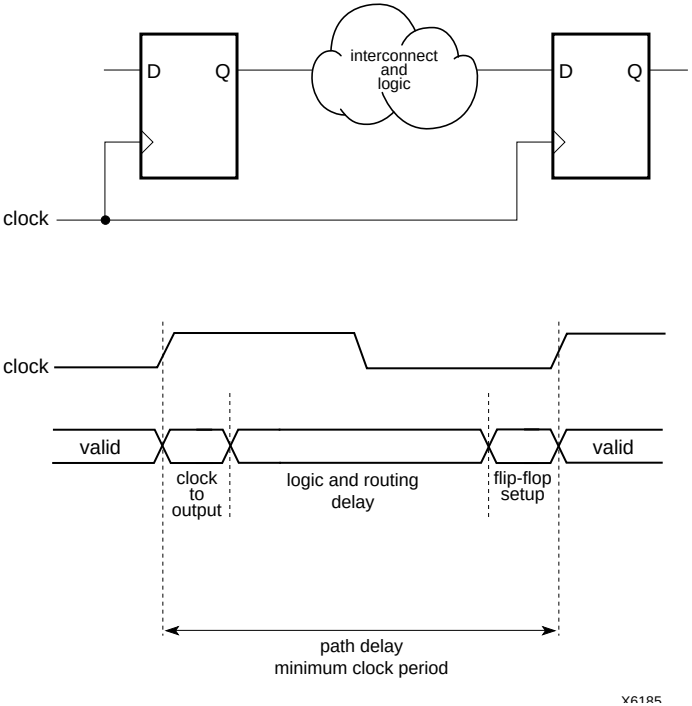


Figure 3-2 Clock-to-Setup Path (Same Clock) with Timing Diagram

Source and destination flip-flops can be clocked by the same clock on different clock edges. In these cases, the path delay limits the minimum clock high or clock low time as shown in the following two figures.

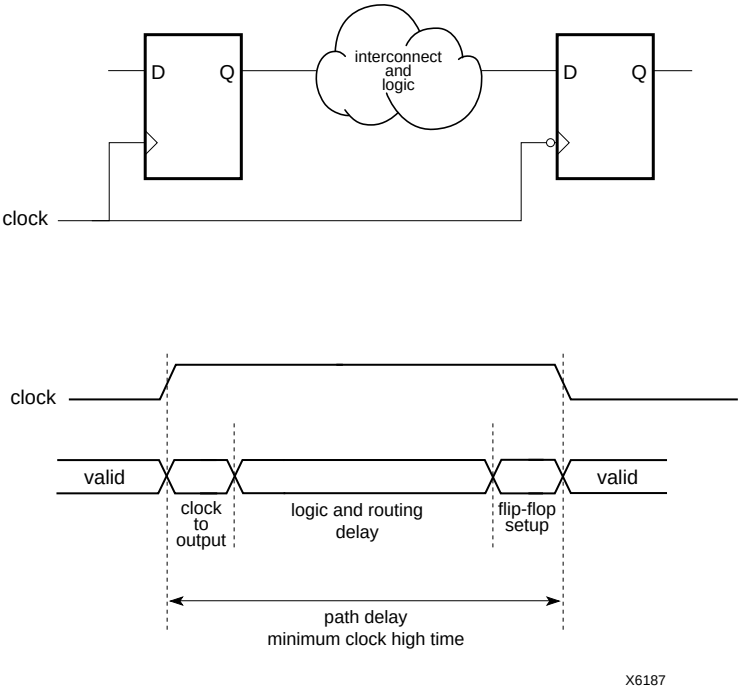


Figure 3-3 Clock-to-Setup Path (Rising to Falling Edge)

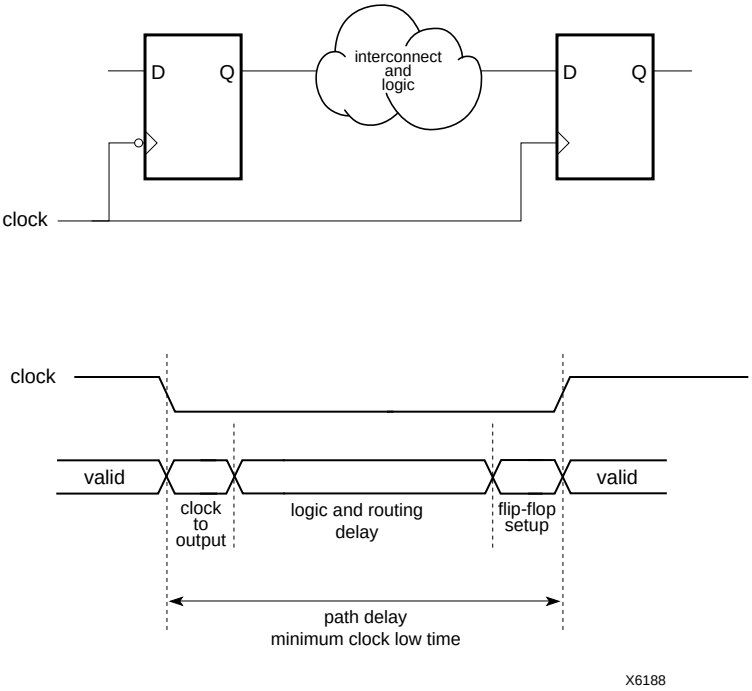


Figure 3-4 Clock-to-Setup Path (Falling to Rising Edge)

If the source and destination are clocked by different clock nets, the clock net on the destination must have a clock period greater than the path delay. The PERIOD constraints allow the Timing Analyzer to use the target flip-flop period for the delay path value. The following figure shows a path of this type.

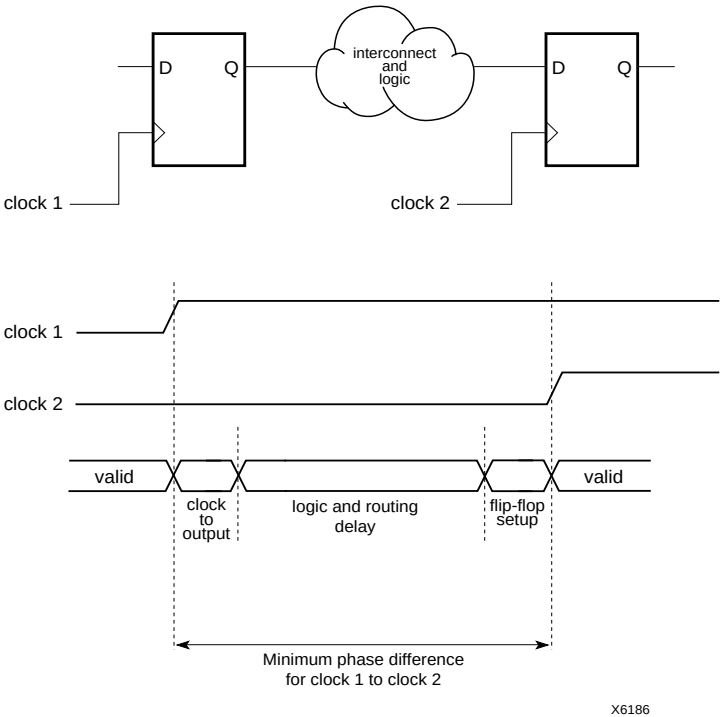


Figure 3-5 Clock-to-Setup Path (Different Clocks)

Clock-to-setup paths do not propagate from the flip-flop Q output through another flip-flop clock or asynchronous Set and Reset input as shown in the next figure. These paths are also broken at bidirectional pins.

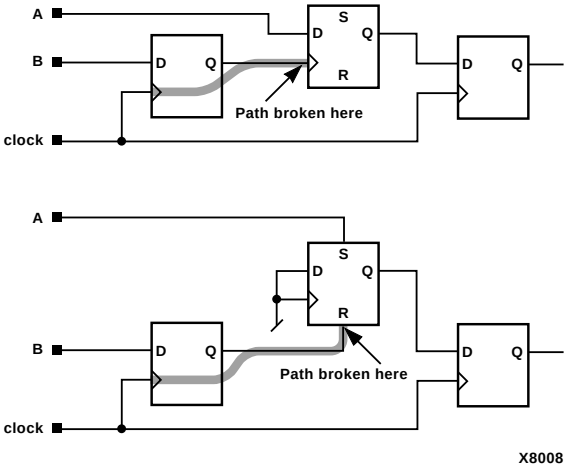


Figure 3-6 Not Propagating Through Asynchronous Set/Reset

Clock to Pad

A clock-to-pad path starts at a clock input of a flip-flop, propagates through the flip-flop Q output and any number of levels of combinatorial logic, and ends at an output pad. It includes the clock-to-Q delay of the flip-flop and the path delay from that flip-flop to the chip output. The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and leave the chip. When using the OFFSET constraint, the clock path is also used in the path delay. The following figure illustrates a clock-to-pad path, along with a timing diagram describing the path.

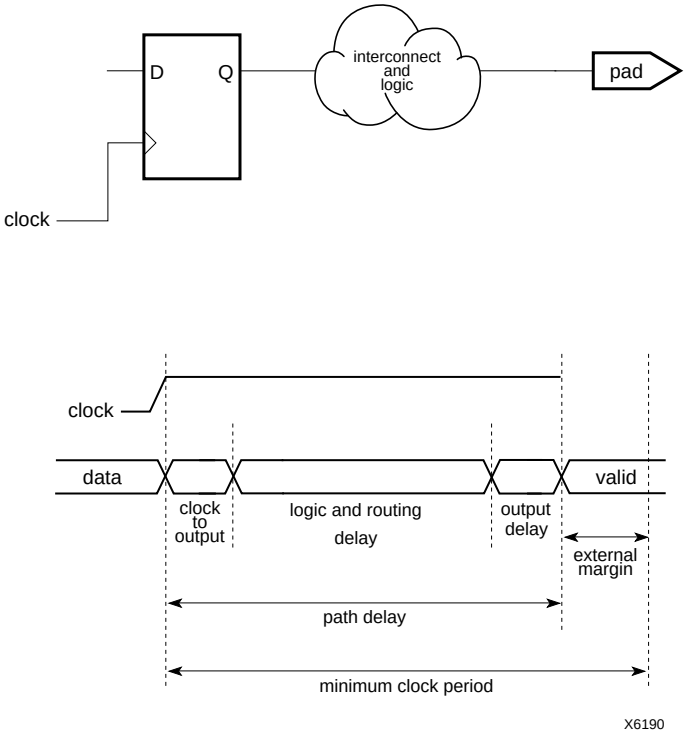


Figure 3-7 Clock-to-Pad Path

Clock-to-pad paths also trace through the enable inputs of tristate controlled pads, as shown in the next figure.

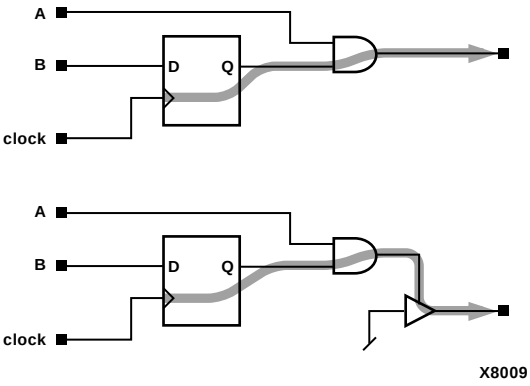


Figure 3-8 Through Tristate Controlled Pads

Clock-to-pad paths do not propagate from the Q output of a flip-flop through the clock of another flip-flop or asynchronous Set and Reset input as shown in the following figure. These paths are also broken at bidirectional pins.

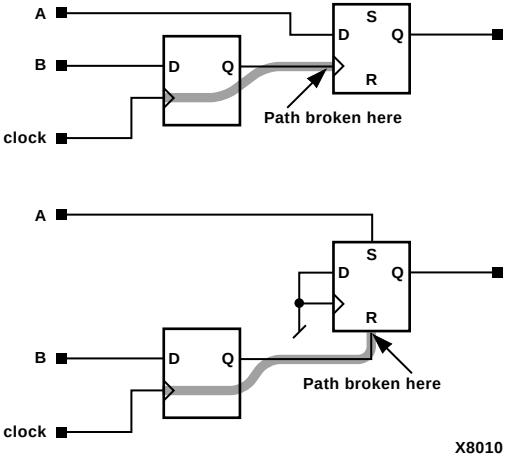


Figure 3-9 Clock-to-Pad Path Broken Through Set/Reset Inputs

Paths Ending at Clock Pin of Flip-Flops

A clock input path starts at a chip input or output. It propagates through any number of levels of combinatorial logic and ends at any clock pin on a flip-flip or latch enable. These paths do not propagate through flip-flops. The clock input path time is the maximum time required for the signal to arrive at the flip-flop clock input. Clock input paths help to determine system-level design timing.

The clock input time is the maximum time only; the Timing Analyzer currently does not calculate minimum clock times.

The next figure shows a clock input path.

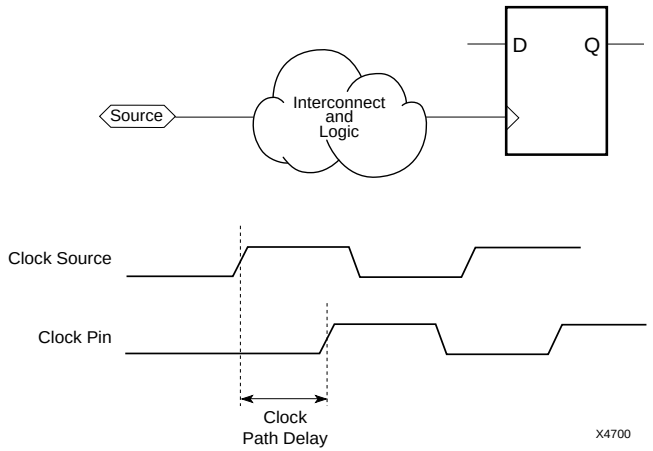


Figure 3-10 Paths Ending at Clock Pin of Flip-Flops

Setup to Clock at the Pad

A setup-to-clock-at-the-pad path starts at an input pad, propagates through input buffers and any number of levels of combinatorial logic, and ends at a flip-flop D/T input, which includes the receiving flip-flop's tSU. This path does not propagate through flip-flops and is also broken at bidirectional pins.

This delay reports tSU for data inputs relative to global or product term clock inputs. It is calculated according to the following formula for global and product term clocks.

```
tSU = Pad to Setup - Path Ending at Clock Pin of
Flip-Flop
```

Global clock paths start at global clock pads, propagate through global clock buffers and end at a flip-flop clock pin. Product term clock paths start at input pads, propagate through a single level of logic implemented in a clock product term, and end at the flip-flop clock pin. All three clock-at-the-pad paths are shown in the next figure.

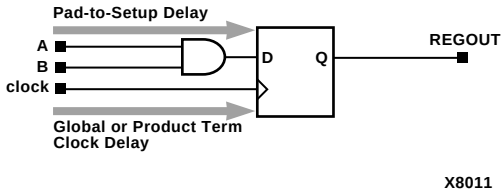


Figure 3-11 Setup-to-Clock-at-the-Pad Path

Clock Pad to Output Pad

A clock-pad-to-output-pad path starts at input pads and trace through all paths that include a flip-flop clock input (except when that path includes a flip-flop asynchronous Set/Reset input) before ending at an output pad. Clock-pad-to-output-pad paths trace through tristate controlled pad enable inputs.

Pad to Pad

A pad-to-pad path starts at an input pad of the chip, propagates through one or more levels of combinatorial logic, and ends at an output pad of the chip. Combinatorial paths also trace through the enable inputs of tristate controlled pads. The pad-to-pad path time is the maximum time required for the data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal. A pad-to-pad path, along with a timing diagram describing the path is displayed in the following figure.

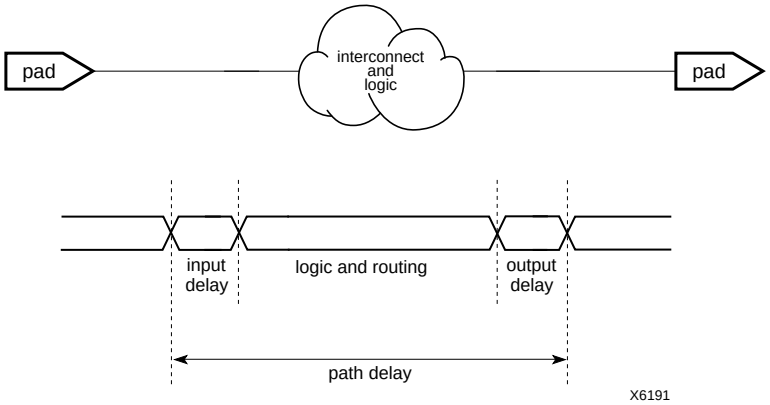


Figure 3-12 Pad-to-Pad Delay

Combinatorial paths are not traced through flip-flops. These paths are also broken at bidirectional pins. A second representation is shown in the next figure.

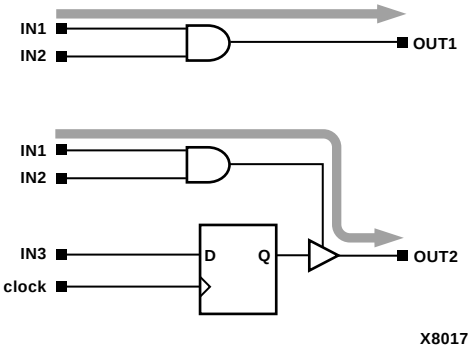


Figure 3-13 Pad-to-Pad Path

Pad to Setup

A pad-to-setup path starts at an input pad of the chip and ends at a D/T input to a flip-flop, latch, RAM, or the receiving flip-flop's tSU, wherever there is a setup time against a control signal. Along the way, it propagates through input buffers and any number of combinatorial logic levels. Pad-to-setup paths do not propagate through flip-flops and are broken at bidirectional pins. The pad-to-setup path time is the maximum time required for the data to enter the chip,

travel through logic and routing, and arrive at the output before the clock or control signal arrives. A pad-to-setup path and timing diagram is shown in the following figure.

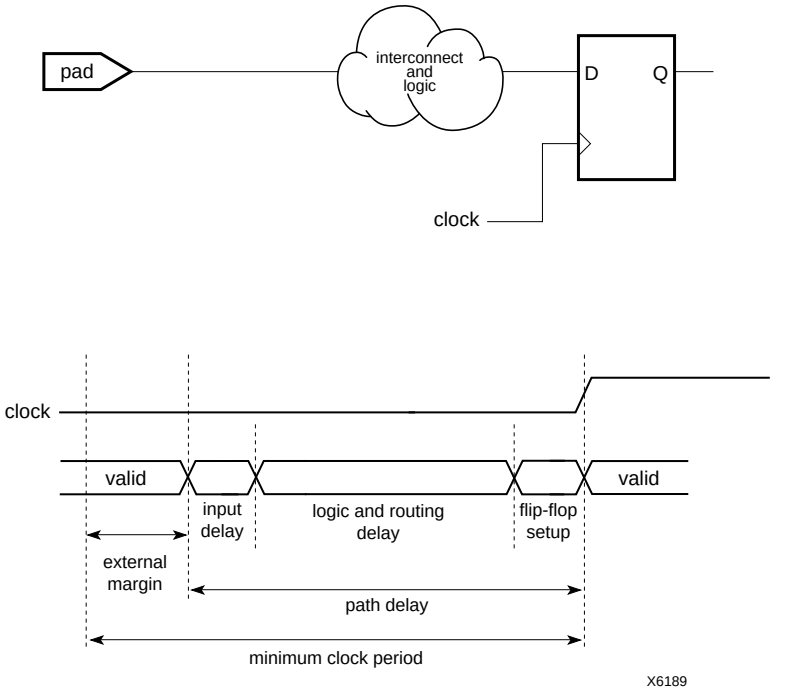


Figure 3-14 Pad-to-Setup Path

Design Analysis Issues

The Timing Analyzer can help you resolve some of the most frequently encountered design problems. This section describes common problems and solutions.

Feedback Loops

Asynchronous feedback paths in a design can cause many paths to be reported that may not actually be timing problems. The most common cases are feedback paths through asynchronous Set or Reset to banks of flip-flops, like a state machine or a counter. Another example is the construction of latches from function generators, which are built using asynchronous feedback paths.

To exclude specific nets that create feedback paths, such as an illegal-state Reset logic loop for a state machine, you can use the Exclude Paths with Nets command to exclude any paths that contain those nets from the timing report.

With the Control Path Tracing command, you can control some asynchronous points through logic; for example, you can exclude the asynchronous Reset of a flip-flop or TBUF input to output.

Timing Constraints

If you entered timing constraints before compiling your design with the mapper, you can use the Timing Analyzer to verify whether your constraints were met. The following example of portions of a Timing Analysis report shows how the Timing Analyzer finds paths that did not meet timing constraints; five errors occurred and three constraints were not met.

```
================================================
   ======================

Timing constraint: TS01 = MAXDELAY FROM TIMEGRP
   "FFS" TO
TIMEGRP "FFS"

2000.000000 pS PRIORITY 0 ;

 1 item analyzed, 1 timing error detected.

 Maximum delay is   3.340ns.

------------------------------------------------
   ----------------------

Slack:    -1.340ns path $1N11 to $1N11 relative to

           2.000ns delay constraint


Path $1N11 to $1N11 contains 2 levels of logic:

Path starting from Comp: CLB.K (from $1N19)
```

```
To                    Delay type         Delay(ns)
   Physical Resource

   Logical Resource(s)

-------------------------------------------------
   --------

CLB.XQ                Tcko                  1.830R
   $1N11

                                              $1N11

CLB.F2                net (fanout=2)     e  0.380R
   $1N11

CLB.K                 Tick                  1.130R
   $1N11

                                              $1N15

                                              $1N11

-------------------------------------------------

Total (2.960ns logic, 0.380ns route)       3.340ns
   (to $1N19)

      (88.6% logic, 11.4% route)

.

.

.


3 constraints not met.
```

```
Data Sheet report:

-----------------

All values displayed in nanoseconds (ns)


Setup/Hold to clock ck1_i

---------------+------------+------------+

               |  Setup to  |  Hold to   |

Source Pad     | clk (edge) | clk (edge) |

---------------+------------+------------+

res_i          |    6.202(R)|            |

start_i        |    2.213(R)|    0.000(R)|

---------------+------------+------------+

.

.

.


Table of Timegroups:

-------------------

TimeGroup PADS:

BELs:

 OUT  D    C    CLR
```

```
TimeGroup FFS:

BELs:

 $1N11


Timing summary:

---------------


Timing errors: 5  Score: 15874


Constraints cover 5 paths, 0 nets, and 5
   connections (100.0% coverage)


Design statistics:

   Maximum path delay from/to any node:  10.716ns


Analysis completed Wed Feb 24 14:29:35 1999

-------------------------------------------------
   ----------------------
```

Clock Skew

The Timing Analyzer can report clock skew, which is the difference between the time a clock signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop on the same clock net. Clock skew occurs most often when global routing is not used to route clock nets, because other routing is less predictable. The arrival of clock signals at different times can affect the required clock period. This section describes negative and positive clock skew and how the Timing Analyzer reports clock skew.

Negative Clock Skew

When the destination is clocked before the source, the clock skew is called negative clock skew. Negative clock skew means that the clock period must be longer than the path delay plus the amount of clock skew between the flip-flops. Negative clock skew is illustrated in the next figure.

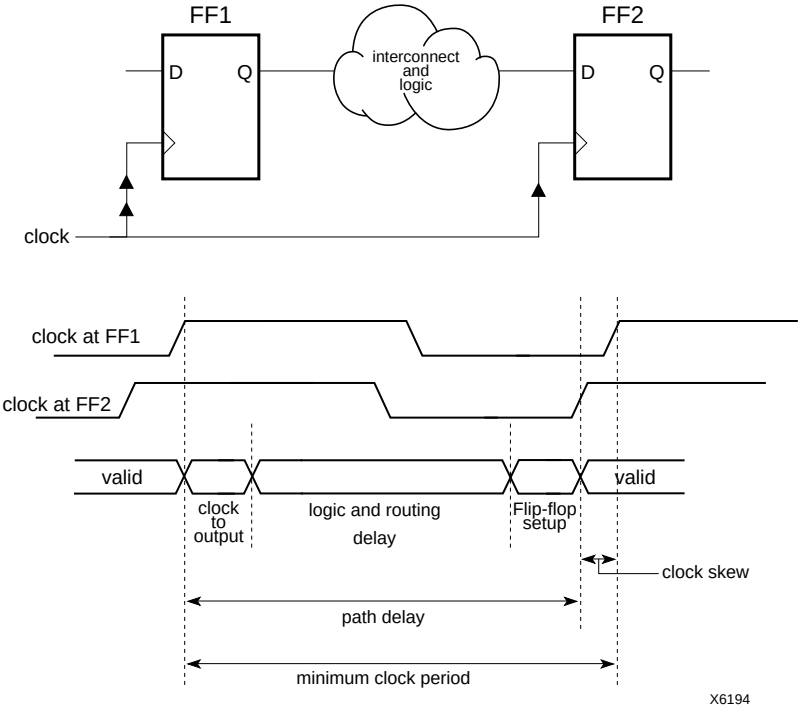


Figure 3-15 Negative Clock Skew

Positive Clock Skew

When the source is clocked first, the clock skew is called positive clock skew. Positive clock skew means that the clock period could be shorter than the path delay by the minimum amount of clock skew. The Timing Analyzer does not account for positive clock skew; it truncates positive clock skew to zero. Positive clock skew is illustrated in the following figure.

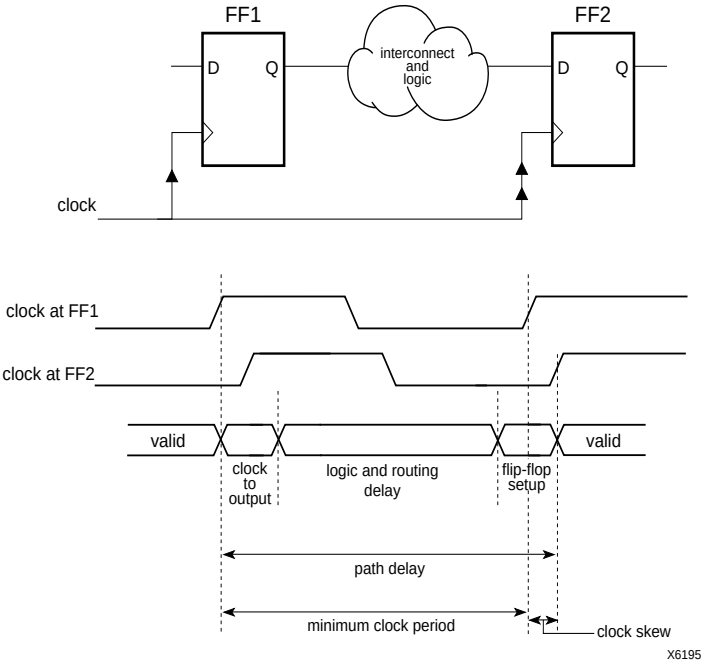


Figure 3-16 Positive Clock Skew

During Timing Analysis

The Timing Analyzer uses the timing constraints specified in the Physical Constraints File (FPGAs) or the VM6 design file (CPLD); it does not infer extra timing constraints. The Timing Analyzer accounts for clock skew for all register to register paths. The following example shows the clock skew portion of a Analyze Against Timing Constraints Analysis report.

```
S
lack: 12.667ns path SOURCE to DEST relative to

        4.633ns total path delay

       -2.300ns clock skew
```

```
       15.000ns delay constraint

Path SOURCE to DEST contains 2 levels of logic:

Path starting from Comp: CLB_R14C13.K (from
   SIG_CLK)

To                   Delay type        Delay(ns)
    Physical Resource


   Logical Resource(s)

------------------------------------------------- -
   -------

CLB_R14C13.YQ        Tcko 2.090R SOURCE


   BEL_SOURCE.FFY

CLB_R14C14.C4        net (fanout=1)        1.533R
   DATA_SRC_DST

CLB_R14C14.K         Tdick 1.010R DEST


   BEL_DEST.FFY

-------------------------------------------------

Total (3.100ns logic, 1.533ns route)      4.633ns
   (to SIG_CLK)

      (66.9% logic, 33.1% route)
```

You can use **Analyze** → **Query Nets** to generate a Query Nets report to display the clock skew across specific clock nets. See the "Querying for Information" section of the "Using the Timing Analyzer" chapter for the procedure to generate a Query Nets Report, an example of a Query Nets Report, and information on the report format.

Off-Chip Delay

To determine system-level clock speed, you must add any external delay to paths that travel off-chip. This way, the Timing Analyzer includes this external delay when calculating the delay for the path. There is no default delay; the Timing Analyzer does not add off-chip delay unless you specify it. See the *XILINX Software Conversion Guide from XACTstep v5.x.x to XACTstep vM!.x.x* for information on how to specify these delays with the OFFSET constraint in the UCF (User Constraints File) file.

Chapter 4

Using the Timing Analyzer

This chapter describes the various functions you can perform with the Timing Analyzer. It contains the following main sections.

- “Opening a Design”
- “Apply Physical Constraints Files”
- “Viewing Settings”
- “Viewing Clocks”
- “Querying for Information”
- “Creating Reports”
- “Specifying Report Appearance and Content”
- “Changing the Speed Grade”
- “Using Path Filtering Commands”
- “Using the Console Window”
- “Using Macros”

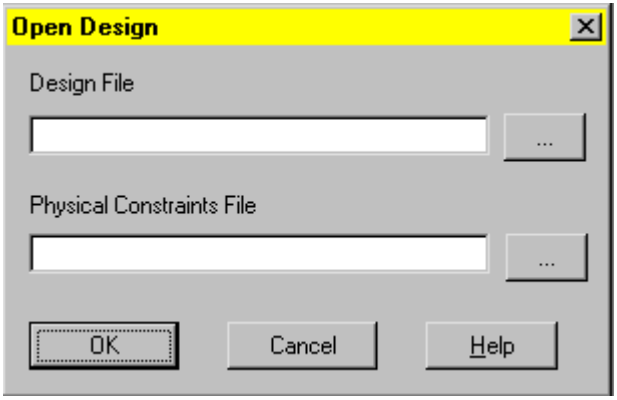
Note The commands and dialog boxes in this chapter are used in the context of procedures, but they are not explained in detail. For a detailed explanation of them, see the Timing Analyzer Online Help Menu Commands.

Opening a Design

Before you can create a timing report using the Timing Analyzer, load a mapped NCD (FPGA) or a completed placed and routed VM6 (CPLD) design file. The NCD (FPGA) can be mapped, placed, or routed. To open a design for timing analysis, follow these steps.

1. Select **File** → **Open Design**, or click on the Open Design toolbar button.

The Open Design dialog box appears, as shown in the following figure.



2. You can also enter a file name in the Physical Constraints File Field or use the Browse button to select a PCF file. If you do not enter a constraints file, Timing Analyzer looks for a physical constraints file with the same name as the design file, but with a .pcf extension
3. The Open dialog box appears.
4. The In the Look in / Directories list box, click on the directory containing the NCD (FPGA) or VM6 (CPLD) file to load.
5. Under Files of Type / List Files of Type, click on the pull-down the list box and select FPGA Designs (*.ncd) or CPLD Designs (*.vm6).

   All the available NCD or VM6 files are displayed in the list box.
6. Select an NCD or a VM6 file from the list box, or type the name in the field below File Name. (*.ncd appears by default; backspace over the asterisk before typing in the design file name.)

7. Click **OK**.

   The Timing Analyzer reads your design and device information, processes any timing constraints, and then loads your design. For FPGA designs, the Timing Analyzer also reads the .pcf physical constraints file with the same name as the design file, if one exists in the same directory as the design file (the PCF file contains physical constraints information). The order of the constraints in the PCF file is reflected by the Timing Analyzer.

   When your design is loaded, the path name and design file name appear at the top of the Timing Analyzer window.

You can now create a timing report. Refer to the "Creating Reports" section for instructions on this procedure.

Warning

If you open a design when another design is open, the Timing Analyzer resets the current settings to the defaults. If you re-open a design that is already open, the Timing Analyzer also resets the current settings to the defaults and opens the default PCF, if it exists.

Apply Physical Constraints Files

Physical Constraints Files (PCF) contain physical constraint information. They apply only to FPGAs, because CPLD timing information is contained in the (VM6) design file itself. The order of the timing constraints in the PCF file is reflected by the Timing Analyzer. This section describes methods for loading and opening Physical Constraints Files.

Manually Opening a Physical Constraints File

If you already have a design open and wish to load a different Physical Constraints File for use with the current design, follow these steps.

1. Select **File** → **Apply Physical Constraints**.

   The Open Physical Constraints dialog box appears.

2. In the Look in / Directories list box, click on the directory containing the PCF file to load.

3. Under Files of Type / List Files of Type, Physical Constraints (*.pcf) is the default and the only file type you can select.

   All the available PCF files are displayed in the list box.

4. Select a PCF file from the list box, or type the name in the field below File name. (*.pcf appears by default; backspace over the asterisk before typing in the physical constraints file name.)

5. Click **OK**.

   The Timing Analyzer reads the PCF file and the path name appears on the right side of the status bar at the bottom of the Timing Analyzer window.

Viewing a Physical Constraints File

In some cases you may want to open a PCF file for viewing from within the Timing Analyzer. When you open a PCF file by this method, the Timing Analyzer does not load the PCF file for use with the current design. It just opens the file for viewing but does not replace the PCF file that is loaded for use with the current design. To open a PCF file in this way, follow these steps.

1. Select **File** → **Open** →**Physical Constraints File**.

   The Open Physical Constraints dialog box appears.

2. Under Files of Type / List Files of Type, select All Files (*.*).

3. Select a PCF file from the list box, or type it in the field below File Name.

4. Click **OK**.

   The PCF file is displayed in a window but the path name on the right side of the status bar at the bottom of the Timing Analyzer window does not change since opening a PCF file by this method does not load the PCF file for processing with the current design.

Viewing Settings

To view current Timing Analyzer settings, select **View** → **Settings**.

The Timing Analyzer displays a pop-up window with the current settings and options. The following figure displays an example of the Settings window.

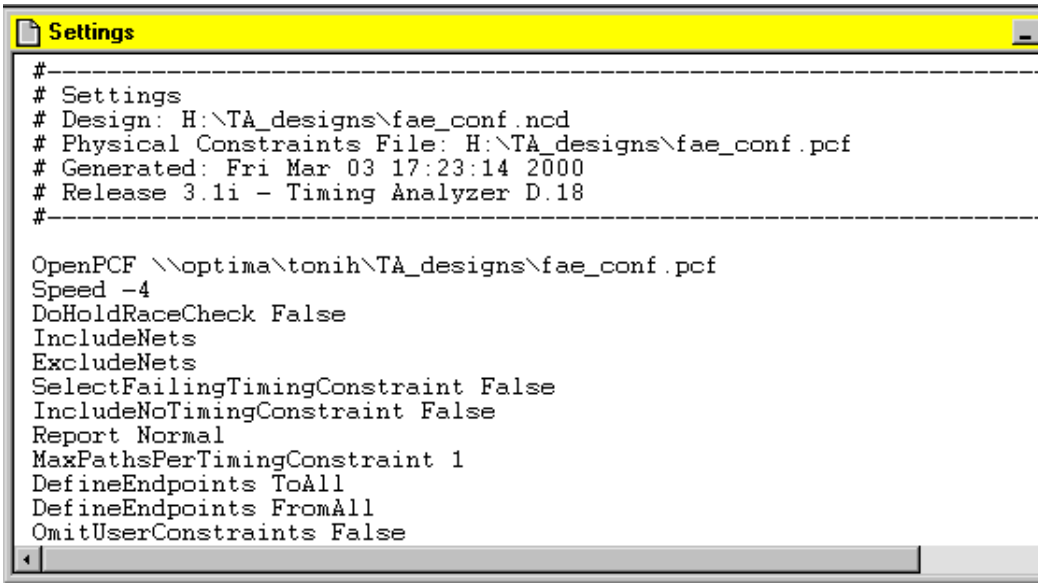


Figure 4-1 Settings Window

When this window is the active window and you change an option setting or a path filter, the change is immediately reflected in the window. If it is not the active window and you change an option or a filter, you must click inside the Settings window to update it automatically.

The contents of the window can be saved as an .xtm file to save the settings as a macro to return the system to the same state as when the settings were saved. See the “Saving a New Macro” and the “Running a Macro” sections for more information. You can also save the contents of the window to a .twr file. TWR files are listed as Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes. See the “Saving a Report” section for the procedure to save a report.

Viewing Clocks

The Clocks report lists the names of all of the clocks in the design. To generate a Clocks report, select **View** → **Clocks**. The Timing Analyzer displays the Clocks report in a pop-up window. You can save the contents of the window as a (.twr) file. TWR files are listed as Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes. See the "Saving a Report" section for the procedure to save a report.

Querying for Information

You may want to focus on the source, destination, and timing of a particular net or time group. You can obtain information about the timing of particular nets or the members of a time group using the Query commands. These commands only applies to FPGAs; it is disabled if a CPLD design is open.

To perform a query, follow this procedure.

1. Select **Analyze** → **Query Nets** or **Analyze** → **Query Timegroups**.

   The Query Nets or Query Timegroups dialog box appears depending on your selection.

2. The following information is generated for each option.

   - Nets — The Timing Analyzer shows the fanout, the timing from the source CLB to each of the destination CLBs, and the CLB names in the generated Query Nets Report.
   - TimeGroups — The Timing Analyzer lists the elements in the specified timing groups in the generated Query TimeGroups Report.

3. If you select Nets, enter a value in the Delay Greater Than field of the Filter for Available Nets.

   The Delay Greater Than value specifies a minimum net delay in nanoseconds. The Timing Analyzer displays only those paths that have a delay greater than or equal to the specified value.

4. Enter a filter in the other portion of the Filter for Available Nets / TimeGroups section, if desired, and click **Apply**.

If you enter a value in the Delay Greater Than and a filter in the filter field, the Timing Analyzer lists the nets that meet both criteria.

5. Select the nets or timing groups that you want to query from the Available Nets / TimeGroups list box and move specific ones or all of them to the Selected Nets / TimeGroups list box.

   See the "Common Fields" section of the "Getting Started" chapter for details on selecting and moving items between list boxes.

6. Click **OK**.

   The Timing Analyzer displays the Query Nets / TimeGroups Report in a pop-up window, which can be saved as a TWR file. Nets / TimeGroups is Nets or TimeGroups, corresponding with your dialog box selection in step 1. See the "Saving a Report" section for the procedure to save a report.

Query Nets Report

The following is an example of Query Nets Report.

```
M-- $1N15 ............... $1I37.O.............. 4.0 $1N6.F4
                                                $1I45.O 4.0 $1N6.F4
--- $1N32 ............... C.I2.................. 2.0 $1I45.T
                                                2.0 $1N6.F3
--- $1N34 ............... D.I2.................. 1.0 $1N6.F1
--- $1N6 ................ $1N6.X................ 1.0 O1.O
                                                1.0 O2.O
--- $1N51 ............... A1.I2................. 0.0 $1I45.I
--- $1N38 ............... B.I2.................. 2.0 $1I37.T
--- $1N41 ............... A.I2.................. 2.0 $1I37.I
```

The contents of the Query Nets Report example have been placed in the following table to illustrate the format of the report. Connections are listed by net, then by source; each is only listed once. Explana-

tions of the information in Net Characteristics and Delay columns follow the table.

Table 4-1 Query Nets Report Format

Net Characteristics	Net Name	Driver Pin Name	Delay Value	Load Pin Name
M--	$1N15	$1I37.O	4.0	$1N6.F4
		$1I45.O	4.0	$1N6.F4
---	$1N32	C.I2	2.0	$1I45.T
			2.0	$1N6.F3
---	$1N34	D.I2	1.0	$1N6.F1
---	$1N6	$1N6.X	1.0	O1.O
			1.0	O2.O
---	$1N51	A1.I2	0.0	$1I45.I
---	$1N38	B.I2	2.0	$1I37.T
---	$1N41	A-I2	2.0	$1I37.I

Net Characteristics

The entries in the Net Characteristics column are comprised of three characters. The characters indicate aspects of the net(s) you query. Each character position is independent of the others. The character position and values of each position are illustrated in this table.

Left = Net Source	Middle = Net Load	Right = If Critical
S = No Source	L = No Load	C = Net marked with CRITICAL property in the design or Net PRI is ≥ 10
M = Multiple Sources		- = Not Critical

Delay Value

The entries in the Delay Value column can include asterisks (*), question marks (?), or tildes (~).

- The pin is unrouted or one or both pins are not yet placed if three asterisks (***) appear as the delay value. An asterisk preceding a

number, *3 for example, indicates the connection delay is estimated, if timing analysis is performed on an unrouted design. Because the Timing Analyzer can perform timing analysis on mapped FPGA designs, generating a Query Nets report can determine if a design does not meet timing requirements before a design is routed.

- A question mark (?) indicates the net was routed incorrectly.
- A tilde (~) preceding a delay value indicates that the delay value is approximate. The delay can be longer than estimated.

Query Time Groups Report

The Query Time Groups report lists the contents of each time group that you select. Time group information is also generated in the Timing Constraints Analysis report.

Creating Reports

After you load a design file, you can decide what kind of report you want to generate. This section describes how to create all the reports available in the Timing Analyzer as well as how to save and print them.

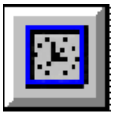
With the Find command on the Edit menu, you can search for specific text strings in reports. Directions for this procedure are given in the "Searching for Text in a Report" section.

The Timing Analyzer has default settings that you can change using filters with various commands. Filters modify the scope of generated reports by specifying which paths you want to analyze. For more information, refer to the "Using Path Filtering Commands" section. To view the current settings, refer to the "Viewing Settings" section.

Timing Constraints Analysis

The Timing Constraints Analysis report compares the design's performance to the timing constraints.

There are several ways to generate a Timing Constraints Analysis report. You can use the following toolbar button to generate a Timing Constraints Analysis report.

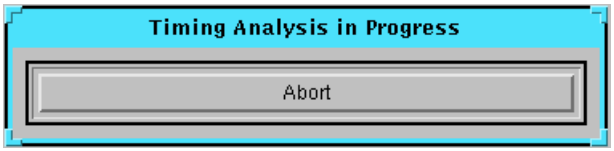


In addition to the button the **`Analyze` → `Against Timing Constraints`** dialog box includes the Timing Constraints tab that contains the following radio button options.

- Report paths against timing constraints
- Report failing paths against timing constraints

To generate a Timing Constraints Analysis report, select one of the previous options.

This command has an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears.



Clicking the Abort button, the Esc key, or the Enter/Return key aborts the analysis and no report is generated or displayed.

In addition to using the above commands, you can use the following path filter options commands to modify the Timing Constraints Analysis report (See “Using Path Filtering Commands” section of the “Using the Timing Analyzer” chapter for more details).

- Disable Timing Constraints (Timing Constraints tab)
- Include Paths with Nets (Filter Paths by Net tab)
- Exclude Paths with Nets (Filter Paths by Net tab)

After processing the design, the Timing Analyzer displays the Timing Constraints Analysis report in a pop-up window. The contents of the window can be saved as a TWR file; see the “Saving a Report” section for the procedure to save a report. Following is an example of a Timing Constraints Analysis report.

```
Timing Analyzer 2.1i
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.

Design file:              testclk.ncd
Physical constraint file: testclk.pcf
Device,speed:             xcv100,-5 (x1_0.71 1.76 Advanced)
Report level:               verbose report, limited to 1 item per
constraint
--------------------------------------------------------------------
-------

================================================================
========
Timing constraint: TS_ck1_i = PERIOD TIMEGRP "ck1_i"  20 nS
HIGH 50.000 % ;
 955 items analyzed, 0 timing errors detected.
 Minimum period is  14.655ns.
--------------------------------------------------------------------
-------
Slack:     5.345ns path core_inst1/counter1/cont<1> to core_inst1/
counter1/cont<9> relative to
          20.000ns delay constraint
Path core_inst1/counter1/cont<1> to core_inst1/counter1/cont<9>
contains 12 levels of logic:
Path starting from Comp: CLB_R10C8.S0.CLK (from ck1)
To                  Delay type         Delay(ns)  Physical Resource

                                                    Logical Resource(s)

-------------------------------------------------  --------
CLB_R10C8.S0.YQ     Tcko               1.203R  core_inst1/counter1/
                                                    cont<1>
                                                    core_inst1/
counter1/
                                                    cont_reg<1>
CLB_R11C10.S0.G1     net (fanout=5)        3.073R  core_inst1/
counter1/
                                                    cont<1>
CLB_R11C10.S0.COUT   Topcyg             1.545R  core_inst1/counter1/
C9/
                                                    C3/C1/O C369
```

```
                                                      core_inst1/
counter1/
                                                      C9/C3/C1
.
.
.
CLB_R9C10.S1.F1       net (fanout=1)          1.491R  core_inst1/
counter1/
N362
CLB_R9C10.S1.CLK    Tas               1.043R  core_inst1/counter1/
                                                      cont<9>
                                                      C303
                                                      core_inst1/
counter1/
                                                      cont_reg<9>
--------------------------------------------------
Total (6.638ns logic, 8.017ns route)      14.655ns (to ck1)
      (45.3% logic, 54.7% route)
--------------------------------------------------------------------
-------
.
.
.
All constraints were met.

Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+

Setup/Hold to clock ck2_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
```

```
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    5.861(R)|            |
---------------+------------+------------+

Clock ck1_i to Pad
---------------+------------+
               | clk (edge) |
Destination Pad|   to PAD   |
---------------+------------+
out1_o         |   16.691(R)|
---------------+------------+

Clock ck2_i to Pad
---------------+------------+
               | clk (edge) |
Destination Pad|   to PAD   |
---------------+------------+
out2_o         |   14.969(R)|
---------------+------------+

Clock to Setup on destination clock ck1_i
- | Src/Dest| Src/Dest| Src/Dest| Src/Dest|
Source Clock   |Rise/Rise|Fall/Rise|Rise/Fall|Fall/Fall|
---------------+---------+---------+---------+---------+
ck1_i          |   14.655|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock ck2_i
---------------+---------+---------+---------+---------+
               | Src/Dest| Src/Dest| Src/Dest| Src/Dest|
Source Clock   |Rise/Rise|Fall/Rise|Rise/Fall|Fall/Fall|
---------------+---------+---------+---------+---------+
ck1_i          |   11.886|         |         |         |
ck2_i          |   14.813|         |         |         |
---------------+---------+---------+---------+---------+


Table of Timegroups:
--------------------
TimeGroup ck1_i:
```

```
BELs:
 core_inst1/counter1/regist1_reg<0>  core_inst1/counter1/
regist1_reg<1>  core_inst1/counter1/regist1_reg<2>
 core_inst1/counter1/regist1_reg<3>  core_inst1/counter1/
regist1_reg<4>  core_inst1/counter1/regist1_reg<5>
 core_inst1/counter1/regist1_reg<6>  core_inst1/counter1/
regist1_reg<7>  core_inst1/counter1/regist1_reg<8>
 core_inst1/counter1/regist1_reg<9>  core_inst1/counter1/
regist0_reg<0>  core_inst1/counter1/regist0_reg<1>
core_inst1/counter1/regist0_reg<2>  core_inst1/counter1/
regist0_reg<3>  core_inst1/counter1/regist0_reg<4>
 core_inst1/counter1/regist0_reg<5>  core_inst1/counter1/
regist0_reg<6>  core_inst1/counter1/regist0_reg<7>
 core_inst1/counter1/regist0_reg<8>  core_inst1/counter1/
regist0_reg<9>  core_inst1/counter1/cont_reg<0>
 core_inst1/counter1/cont_reg<1>     core_inst1/counter1/
cont_reg<2>     core_inst1/counter1/cont_reg<3>
 core_inst1/counter1/cont_reg<4>     core_inst1/counter1/
cont_reg<5>     core_inst1/counter1/cont_reg<6>
 core_inst1/counter1/cont_reg<7>     core_inst1/counter1/
cont_reg<8>     core_inst1/counter1/cont_reg<9>

TimeGroup ck2_i:
BELs:
 core_inst2/counter1/regist1_reg<0>  core_inst2/counter1/
regist1_reg<1>  core_inst2/counter1/regist1_reg<2>
 core_inst2/counter1/regist1_reg<3>  core_inst2/counter1/
regist1_reg<4>  core_inst2/counter1/regist1_reg<5>
 core_inst2/counter1/regist1_reg<6>  core_inst2/counter1/
regist1_reg<7>  core_inst2/counter1/regist1_reg<8>
 core_inst2/counter1/regist1_reg<9>  core_inst2/counter1/
regist0_reg<0>  core_inst2/counter1/regist0_reg<1>
 core_inst2/counter1/regist0_reg<2>  core_inst2/counter1/
regist0_reg<3>  core_inst2/counter1/regist0_reg<4>
 core_inst2/counter1/regist0_reg<5>  core_inst2/counter1/
regist0_reg<6>  core_inst2/counter1/regist0_reg<7>
 core_inst2/counter1/regist0_reg<8>  core_inst2/counter1/
regist0_reg<9>  core_inst2/counter1/cont_reg<0>
 core_inst2/counter1/cont_reg<1>     core_inst2/counter1/
cont_reg<2>     core_inst2/counter1/cont_reg<3>
 core_inst2/counter1/cont_reg<4>     core_inst2/counter1/
cont_reg<5>     core_inst2/counter1/cont_reg<6>
```

```
 core_inst2/counter1/cont_reg<7>     core_inst2/counter1/
cont_reg<8>     core_inst2/counter1/cont_reg<9>

Timing summary:
---------------

Timing errors: 0  Score: 0

Constraints cover 2184 paths, 0 nets, and 380 connections (100.0%
coverage)

Design statistics:
   Minimum period:  14.813ns (Maximum frequency:  67.508MHz)

   Minimum input arrival time before clock:   6.202ns
   Minimum output required time after clock:  16.691ns

Analysis completed Fri Mar 12 12:10:11 1999
------------------------------------------------------------------
------
```

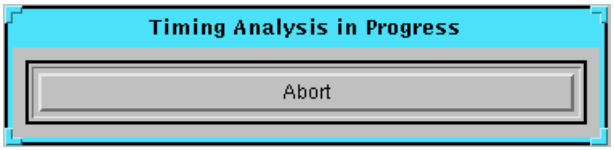
Analyze Against Auto Generated Design Constraints Analysis Report

The Analyze Against Auto Generated Design Constraints Analysis report provides a set of summary statistics for the paths from the timing requirements submitted for analysis. This report is essentially an error report that displays a summary header for each constraint whether it passes or not and lists paths in error for constraints that are violated.

If the PCF file contains no constraints, the Analyze Against Auto Generated Design Constraints Analysis report creates four basic constraints: PERIOD, OFFSET IN, OFFSET OUT, and PAD TO PAD.

To generate an Analyze Against Auto Generated Design Constraints Analysis report, select **Analyze** → **Analyze Against Auto Generated Design Constraints**, or click on the Analyze Against Auto Generated Design Constraints button in the toolbar.

This command has an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears.



Clicking the Abort button, the Esc key, or the Enter/Return key aborts the analysis. A report is not generated or displayed.

After processing the design, the Timing Analyzer displays the Analyze Against Auto Generated Design Constraints Analysis report in a pop-up window. The contents of the window can be saved as a TWR file; see the “Saving a Report” section for the procedure to save a report. Following is an example of an FPGA Analyze Against Auto Generated Design Constraints Analysis report.

```
--------------------------------------------------------------------
-------
Timing Analyzer 2.1i
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.

Design file:              C:\designs\loop.ncd
Physical constraint file: C:\designs\loop.pcf
Device,speed:             xc4036ex,-3 (x1_0.08 3.7f )
Report level:                error report, limited to 1 item per
constraint
--------------------------------------------------------------------
-------


====================================================================
========
Timing constraint: TS01 = MAXDELAY FROM TIMEGRP "FFS" TO
TIMEGRP "FFS"
```

```
2000.000000 pS PRIORITY 0 ;
 1 item analyzed, 0 timing errors detected.
 Maximum delay is   3.340ns.
--------------------------------------------------------------------------
-------


==============================================================================
========
Timing constraint: TS02 = MAXDELAY FROM TIMEGRP "PADS" TO
TIMEGRP "FFS"
1500.000000 pS PRIORITY 0 ;
 3 items analyzed, 3 timing errors detected.
 Maximum delay is   4.006ns.
--------------------------------------------------------------------------
-------
Slack:    -2.506ns path D to $1N11 relative to
           1.500ns delay constraint

Path D to $1N11 contains 2 levels of logic:
Path starting from Comp: IOB.PAD
To                  Delay type         Delay(ns)  Physical Resource

                                                  Logical Resource(s)

-------------------------------------------------  --------
IOB.I1               Tpid                  1.810R  D
                                                   D
                                                   $1N13
CLB.F1               net (fanout=1)     e  1.066R  $1N13
CLB.K                Tick                  1.130R  $1N11
                                                   $1N15
                                                   $1N11
-------------------------------------------------
Total (2.940ns logic, 1.066ns route)       4.006ns (to $1N19)
      (73.4% logic, 26.6% route)

--------------------------------------------------------------------------
-------

==============================================================================
```

```
========
Timing constraint: TS03 = MAXDELAY FROM TIMEGRP "FFS" TO
TIMEGRP "PADS"
2500.000000 pS PRIORITY 0 ;
 1 item analyzed, 1 timing error detected.
 Maximum delay is  10.716ns.
--------------------------------------------------------------------
-------
Slack:    -8.216ns path $1N11 to OUT relative to
           2.500ns delay constraint

Path $1N11 to OUT contains 2 levels of logic:
Path starting from Comp: CLB.K (from $1N19)
To                  Delay type         Delay(ns)  Physical Resource

                                                     Logical Resource(s)

-------------------------------------------------  --------
CLB.XQ              Tcko                  1.830R  $1N11
                                                  $1N11
IOB.O               net (fanout=2)     e  1.066R  $1N11
IOB.PAD             Tops                  7.820R  OUT
                                                  OUT.OUTBUF
                                                  OUT
-------------------------------------------------
Total (9.650ns logic, 1.066ns route)      10.716ns
      (90.1% logic, 9.9% route)

--------------------------------------------------------------------
-------


2 constraints not met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
```

```
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+
.
.
.

Table of Timegroups:
--------------------
TimeGroup PADS:
BELs:
 OUT  D    C    CLR

TimeGroup FFS:
BELs:
 $1N11



Timing summary:
---------------

Timing errors: 4  Score: 15874

Constraints cover 5 paths, 0 nets, and 5 connections (100.0%
coverage)


Design statistics:
   Maximum path delay from/to any node:  10.716ns


Analysis completed Wed Mar 3 14:30:42 1999
-------------------------------------------------------------------
-------
```

The format of a CPLD Analyze Against Auto Generated Design Constraints Analysis report differs from the FPGA report format, as shown in the following report excerpt.

```
Design:     tspec1d
Device:     XC9572-7-PC84
Program:    Timing Report Generator Version Internal-M1.0.0a
Date:       Thu Feb 18 10:41:18 1999
Performance Summary:
Worst case Pad to Pad path delay  :     9.0ns (1 macrocell levels)

 (Includes an external input margin of 0.0ns.)
 (Includes an external output margin of 0.0ns.)
Pad 'X19' to Pad 'Y1'
------------------------------------------------------------------------
-------
                Combinational Pad to Pad Delays(nsec)
\ From        B    B    C    C    X    X    X    X   X    X    X    X

 \                 B         C    0    1    1    1   1    1    1    1

  \                                    0    1    2   3    4    5

   \
    \
     \
      \
    To \-------------------------------------------------------------
-----
Y1         7.5    7.5         7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5

Y2                            7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5

Y3              9.0      9.0
Y4
------------------------------------------------------------------------
-------
                Combinational Pad to Pad Delays(nsec)
\ From        X    X    X    X    X    X    X    X    X    X    X    X

 \           1    1    1    1    2    3    4    5    6    7    8    9
```

```
  \           6    7    8    9
   \
    \
     \
      \
       \
    To \-------------------------------------------------------
------
Y1         7.5  7.5  9.0  9.0  7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5

Y2                             7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5

Y3
Y4
.
.
.
Path Type Definition:
Pad to Pad (tPD) -                          Reports pad to pad paths
that start
                                 at input pads and end at output pads.
                                        Paths are not traced through
                                           registers.
Clock Pad to Output Pad (tCO) -          Reports paths that start at
input
                                   pads trace through clock inputs of
                                    registers and end at output pads.
                                  Paths are not traced through PRE/CLR
                                           inputs of registers.

Setup to Clock at Pad (tSU) -            Reports external setup time
of data
                                   to clock at pad. Data path starts at
                                   an input pad and end at register D/T
                                  input. Clock path starts at input pad
                                  and ends at the register clock input.
                                        Paths are not traced through
                                           registers.

Clock to Setup (tCYC) -                Register to register cycle time.
                                        Include source register tCO and
                                             destination register tSU.
```

You can use the following path filtering commands to modify the scope of the Analyze Against Auto Generated Design Constraints Analysis report.

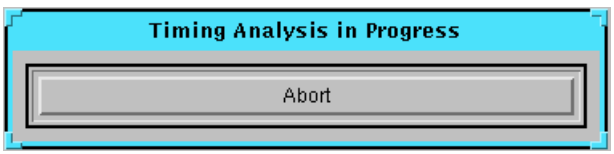
- Include Paths with Nets (Filter Paths by Net tab)
- Exclude Paths with Nets (Filter Paths by Net tab)
- Path Tracing (Path Tracing tab)

Analyze Against User Specified Paths by Defining Endpoints Analysis Report

The Analyze Against User Specified Paths by Defining Endpoints report displays a detailed analysis of all specified paths. It contains the worst-case path delays for all paths that are not filtered out.

To generate a Analyze Against User Specified Paths by Defining Endpoints report, select **`Analyze` → `Analyze Against User Specified Paths by Defining Endpoints`**, or click on the Analyze Against User Specified Paths by Defining Endpoints button in the toolbar.

This command has an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears.



Clicking the Abort button, the Esc key, or the Enter / Return key aborts the analysis. A report is neither generated nor displayed.

After processing the design, the Timing Analyzer displays the Analyze Against User Specified Paths by Defining Endpoints report in a pop-up window. The contents of the window can be saved as a TWR file; see the “Saving a Report” section for the procedure to save a report. Following is an example of this report.

```
--------------------------------------------------------------------
-------
Timing Analyzer 2.1i
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.

Design file:              C:\designs\loop.ncd
Device,speed:             xc4036ex,-3 (x1_0.08 3.7f )
Report level:               verbose report, limited to 1 item per
constraint
--------------------------------------------------------------------
-------


====================================================================
========
Timing constraint: PATH "PATHFILTERS" = FROM TIMEGRP
"SOURCES" TO TIMEGRP
"DESTINATIONS" ;
 5 items analyzed, 0 timing errors detected.
 Maximum delay is  10.716ns.
--------------------------------------------------------------------
-------
Delay:    10.716ns $1N11 to OUT

Path $1N11 to OUT contains 2 levels of logic:
Path starting from Comp: CLB.K (from $1N19)
To                  Delay type         Delay(ns)  Physical Resource

                                                  Logical Resource(s)

-------------------------------------------------  --------
CLB.XQ              Tcko                  1.830R  $1N11
                                                  $1N11
IOB.O               net (fanout=2)     e  1.066R  $1N11
IOB.PAD             Tops                  7.820R  OUT
                                                  OUT.OUTBUF
                                                  OUT
-------------------------------------------------
Total (9.650ns logic, 1.066ns route)      10.716ns
      (90.1% logic, 9.9% route)
```

```
------------------------------------------------------------------------
-------


All constraints were met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+
.
.
.


Table of Timegroups:
--------------------
TimeGroup SOURCES:
BELs:
 $1N11  OUT    D      C      CLR

TimeGroup DESTINATIONS:
BELs:
 $1N11  OUT    D      C      CLR



Timing summary:
---------------

Timing errors: 0  Score: 0
```

```
Constraints cover 5 paths, 0 nets, and 5 connections (100.0%
coverage)


Design statistics:
   Maximum path delay from/to any node:  10.716ns


Analysis completed Wed Mar 3 14:31:19 1999
--------------------------------------------------------------------
-------
```

You can use the following path filtering commands from the analyze tabs to modify the scope of the Analyze Against User Specified Paths by Defining Endpoints report.

- Select Sources (Path Endpoints tab)
- Select Destinations (Path Endpoints tab)
- Include Paths with Nets (Filter Paths by Net tab)
- Exclude Paths with Nets (Filter Paths by Net tab)
- Path Tracing (Path Tracing tab)

Viewing a Report

When a Timing Analysis report (TWR file) is opened in the Timing Analyzer window, the report window contains three sub-windows, as shown in the following figure.

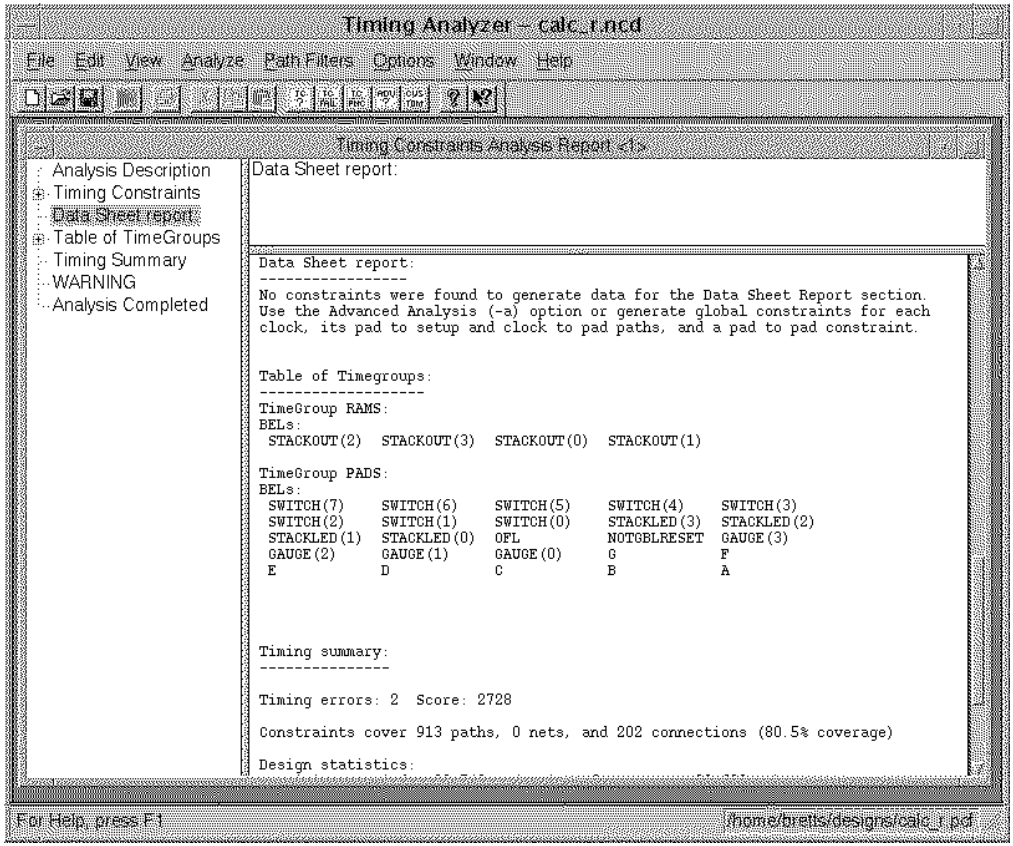


Figure 4-2 Timing Analyzer Report Window

The report itself is displayed in the lower right window. The upper right window shows what section of the report is currently displayed on the screen. As you scroll through the report, the section name in the upper right window automatically changes.

The window on the left contains a hierarchical display of the headings in the report. Selecting a heading causes the report to scroll immediately to that location. You can click on a box with a plus sign (+) in it to show the sections within that heading.

The size of the three windows can be adjusted as needed.

Saving a Report

Follow this procedure to save a generated report as a file.

1. Make sure the report that you want to save is the active window by clicking on it. The active window has a colored border.
2. Select **File** → **Save**, or click the Save button.

   The Timing Analyzer displays the Save As dialog box.
3. Under List Files of Type, click on the down arrow to display the pull-down list box of available file types. Highlight Timing Analysis Reports (*.twr) to select it. File names of that format appear in the list box below the File Name field.
4. In the File Name field, type in the name of the file in which to store the report. The .twr extension is added automatically.

   If this is the first time you are saving the file, the Timing Analyzer provides a default name corresponding with the type of information contained in the window (timing constraints, clocks, and so forth).

   If you want to overwrite an existing file with the new report, click on that file name in the list box, so it appears in the File Name field.

   You can use word processor applications to open and edit the report file.
5. In the Save in field / Directories list box, select the directory in which you want to save the report.
6. Click **OK**.

   The Save As dialog box closes.

Searching for Text in a Report

You can use the Find command to search for any text string in the active report window, including normal grammatical symbols like

hyphens or underscores. You cannot search for special characters like tabs or hard returns, however.

To search for a text string in a report, do the following.

1. Open or select the report window in which you want to search.
2. Select **Edit** → **Find**.

   The Find dialog box appears.
3. Enter the text string that you want to search for in the Find What field.
4. You can optionally match the case of the search string by selecting Match Case. Then only instances that have the same case as the text string will be found. By default, case is ignored.
5. Indicate the search direction, as follows.
   - Up searches backward from the present location of the cursor to the beginning of the report. Searching stops at the beginning of the report.
   - Down searches forward from the present location of the cursor to the end of the report. Searching stops at the end of the report. This direction is the default.
6. Click the Find Next button, the F3 key, or select **Edit** → **Find Next** to find the next instance of the text string.
7. Click **Cancel** to close the Find dialog box.

Printing a Report

You can send a Timing Analyzer report to your default printer, or you can send it to a printer that you specify.

Note Print dialog boxes vary between platforms and window operating systems. The procedure in this section is basic; consult your specific system documentation for details.

To send a report to the default printer, follow these instructions.

1. **Select File** → **Print**, or click the Print button.

The Timing Analyzer displays the Print dialog box.

2. If you want to print more than one copy, enter the number of copies that you want to print in the Copies field.
3. If you want to print a range of pages, enter “From” and “To” pages in the corresponding boxes.
4. If you want to print to a file, select Print to File.
5. Click **OK**.

Closing a Report

To close a report, use one of the following methods.

Using Menu Commands

Select **File** → **Close**.

If the report has been previously saved, the window closes. If it has not been saved, the Save As dialog box appears; see the “Saving a Report” section for the procedure to save a report.

Using the Mouse

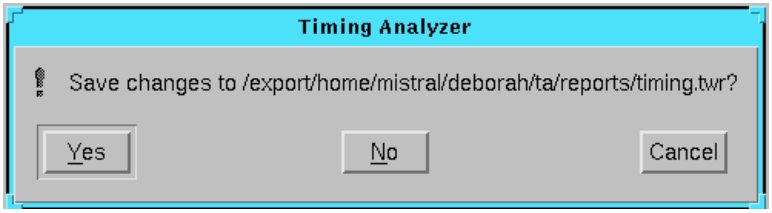
Make sure the report that you want to close is the active window by clicking on it. The active window will have a colored border.

1. Click on the horizontal bar in the upper left-hand corner of the report pop-up window.

   A pop-up menu appears.

2. Select Close from the menu.

   The following prompt box appears.



3. Click **Yes** to save the report window.

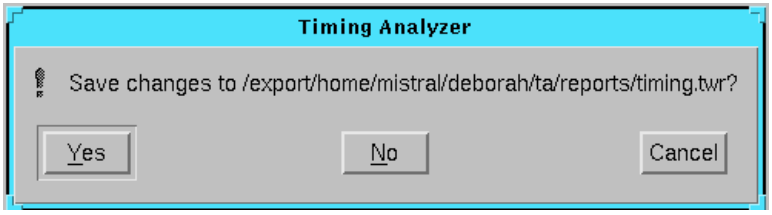
   The Save As dialog box appears; see the "Saving a Report" section for the procedure to save a report. If you click No, the dialog box and report window both close without saving. If you click Cancel, the dialog box closes and the report window remains open.

Using the Keyboard

Make sure the report that you want to close is the active window by clicking on it. The active window will have a colored border.

1. Type **Ctrl F4** from the keyboard.

   The following prompt box appears.



2. Click **Yes** to save the report.

   The Save As dialog box appears; see the "Saving a Report" section for the procedure to save a report. If you click No, the dialog box and report window both close without saving. If you click Cancel, the dialog box closes and the report window remains open.

Opening a Saved Report

You can open a previously saved report to view or print by following these steps.

1. Select **File** → **Open**.

The Open dialog box appears.

2. In the Look in / Directories list box, click on the directory containing the report file to load.
3. In the List Files of Type field, select Timing Analysis Reports (*.twr) is selected. The default is Timing Analysis Macros (*.xtm).

   All the available report files are displayed in the list box (below the File Name field).
4. Select a report file from the list box, or type the name in the field below File Name after backspacing over the asterisk. If you do not specify a file extension, the Timing Analyzer loads an XTM (macro) file by default.
5. Click **OK**.

Specifying Report Appearance and Content

By default, the Timing Analyzer analyzes and reports on all paths in a design. However, you can determine the appearance and the content of the reports that the Timing Analyzer generates.

Perform the steps described in the following sections to customize generated reports. Each section describes a report output option you can specify.

1. Select **Analyze Against Timing Constraints → Options (Tab)**.

   The Timing Analyzer displays the Options Tab.

   The following table lists each option in the Option tab dialog and indicates if the option is available for FPGA or CPLD designs.

Option	FPGA	CPLD
Speed Grade	Yes	Yes
Summary Only	Yes	No
No Limit	Yes	Yes
Limit Report To	Yes	Yes
Perform Hold / Race Checks	No	Yes
Wide Report	Yes	Yes

Option	FPGA	CPLD
Voltage Prorating	Yes	Yes
Temperature Prorating	Yes	Yes

2. After specifying all desired report options, click **OK**.

   The Options tab dialog closes. You can now select additional filtering commands or generate a Timing Analysis report, as described in the "Timing Constraints Analysis" section.

Creating a Summary Report

Note The Summary Only option only applies to FPGAs; it is disabled if a CPLD design is open.

To generate a summary report, select Summary Only in the Report Options dialog box. A summary report contains only the path source and end point. It lists one delay path per line and does not display cumulative delays.

Setting the Maximum Number of Paths Per Timing Constraint

To limit the total number of paths per timing constraint that the Timing Analyzer reports, select the Limit Report To radio button and enter a value in the Limit Report To field.

You can use this option with the criterion you specify in the Sort On field when generating an Analyze Against User Specified Paths by Defining Endpoints report. For example, if you enter 10 in the Maximum Number of Paths per Timing Constraint field and set the Sort On option to Descending Delay, the Timing Analyzer reports the 10 paths with the longest delay.

You can optionally use a keyboard command to set this option.

1. Select **View** → **Console**.
2. In the field at the bottom of the Console window, type the following.

   ```
   MaxPathsPerTimingConstraint number_of_paths
   ```

   You can use this keyboard command in a macro.

Reporting Delays Less Than a Value

Note This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

To instruct the Timing Analyzer to report only those paths that have a delay less than or equal to the specified value, enter a value, in nanoseconds in the Report Delays Less Than field of the Report Options dialog box. Make the field blank to include paths regardless of how large the delays are.

Reporting Delays Greater Than a Value

Note This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

You can instruct the Timing Analyzer to report only those paths that have a delay greater than or equal to the specified value. To do so, enter a value, in nanoseconds, in the Report Delays Greater Than, field of the Report Options dialog box.

Sorting Path Report Order

Note This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

You can specify how the Timing Analyzer sorts path types when they are reported. To specify how paths are sorted, right click on a selected box, Sort On field in the Path Tracing tab, and select a path type.

- Ascending Delay
- Descending Delay
- Source Net
- Destination Net
- Source Clock Net
- Destination Clock Net

Reporting Only Longest Paths Between Points

Note This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

If there is more than one path between two end points, you can direct the Timing Analyzer to report only the path with the longest delay. Select Report Only Longest Paths Between Points in the Report Options dialog box.

Generating Wide Reports

By default, the Timing Analyzer generates a report formatted with 80 characters per line. To generate a wide report, select Wide Report. Wide reports have 132 characters per line. They help reduce the number of truncated net names, since names are truncated to 132 characters instead of 80 characters as in a default report.

Changing the Speed Grade

The speed grade is usually set during the design implementation process. Changing the speed grade helps you determine if you need to target a faster device to meet your timing requirements, or if using a slower speed grade still meets timing constraints.

Changing the speed grade may affect the worst case and range of values available in the Options tabbed dialog box.

Note Changing the speed grade with the Timing Analyzer only affects analysis. The speed grade in the design file is not changed.

To change the speed grade for timing analysis, perform the following steps.

1. Select **`Analyze`** → **`Analyze Against...`** → **`Options (Tab)`**.

   The Options tab appears, including the Speed Grade option box.

2. Click OK.

The Speed Grade dialog box closes. You can now select additional filtering commands or generate a report.

Using Path Filtering Commands

By default, the Analyze Against User Specified Paths by Defining Endpoints reports the path delays for all paths in the design. However, you can instruct the Timing Analyzer to analyze and report on a subset of paths by using commands in the Path Endpoints tab in

the Analyze Against User Specified Paths by Defining Endpoints dialog box.

The Path Filters menu consists of the Reset All Path Filters command and the Timing Constraint Filters, Custom Filters, and Common Filters submenus.

The types of commands contained in these submenus are described in the "Path Filtering Commands" section of the "Introduction" chapter. Also, see the "Specifying Report Appearance and Content" section for information on report format and general content customizing.

After using these commands to specify specific paths and to apply filters, you can generate reports using the commands in the Analyze menu. Refer to the "Creating Reports" section for more information on report generation.

The procedures in the following sections often direct you to specify a filter in a dialog box or to move items between list boxes. Refer to the"Common Fields" section of the "Getting Started" chapter for detailed instructions on specifying a filter and on selecting and moving items between list boxes.

Timing Constraint Filters

The Timing Constraints Tab includes Filters that Disable Timing Constraints which you can use to prevent the Timing Analyzer from analyzing specific timing constraints. These commands function only if a design is loaded. They do not alter the Analyze Against Auto Generated Design Constraints Analysis report or the Analyze Against User Specified Paths by Defining Endpoints report.

To prevent the Timing Analyzer from analyzing specified timing constraints, perform the following steps.

1. Select **`Analyze`** → **`Analyze Against Timing Constraints`** → **`Timing Constraints (Tab)`**.

   Note If an FPGA design is open, the Include PCF Entered Constraints radio button is selected by default. Click the Omit PCF Entered Constraints radio button, if you want to include user constraints during analysis. User constraints are contained in the "USER" section of the PCF. These two buttons and their functions are only visible and available for FPGAs.

2. If you would like to display a subset of timing constraints, enter a filter string in the Filter field and click Apply.

   The subset of timing constraints is displayed in the Enabled Constraints list box.

3. Select the timing constraints you want to exclude from the Timing Constraints Analysis report in the Enabled Constraints list box and move specific ones or all of them to the Disabled Constraints list box.

   See the "Common Fields" section of the "Getting Started" chapter for instructions on moving items between list boxes.

4. Click OK.

   The Disable Timing Constraints dialog box closes. You can now select another command or generate a Timing Constraints Analysis report.

Custom Filters

You can select starting points and ending points using commands described in this section to specify the scope of path analysis information reported in the Analyze Against User Specified Paths by Defining Endpoints report. These commands are in the Custom Filters submenu of the Path Filters menu. By default, the Timing Analyzer selects all sources and all destinations for path analysis.

Selecting Sources

To select specific sources for path analysis.

1. Select **`Analyze`** → **`Analyze Against...`** → **`Path Endpoints (Tab)`**.
2. Use the grid based dialog to make your selections.
3. Click **`OK`**.

Selecting Destinations

To select specific destinations for path analysis, follow this procedure.

1. Select **`Analyze`** → **`Analyze Against...`** → **`Path Endpoints (Tab)`**.

2. Select the ending point type by clicking the down arrow of the Destination Element Type pull-down list box to display the list of destinations, then highlight it. The default is Flip-Flops.

   FPGA destination types can be flip-flops, RAMs, latches, pads, nets, pins, CLBs, clocks, or timegroups. CPLD destination types can be flip-flops, pads, nets, macrocells, or clocks.

   If an element type is not used in the design, the type will not appear in the pull-down list.

   Element in the Destination Element list box changes to match the destination type you select.

3. Click **OK**.

Common Filters

You can include or exclude paths with nets or Path Tracing using commands described in this section to specify the scope of timing analysis. These commands exist in the Common Filters submenu of the Path Analysis menu.

Although the Include Paths with Nets and Exclude Paths with Nets commands in the Common Filters submenu appear to be similar, they are not mutually exclusive. For example, you might want to exclude any path that goes through the synchronous Reset net of the counter but include all paths that go through bit 1 of the counter. By using the Exclude Paths with Nets command to exclude the synchronous Reset, and the Include Paths with Nets command to include paths through the bit 1, you can include or exclude specific nets that are attached to the counter.

After using the path filtering commands in the Common Filters submenu, you can generate a Timing Constraints Analysis, Analyze Against Auto Generated Design Constraints Analysis, or Analyze Against User Specified Paths by Defining Endpoints report.

Including Paths with Nets

Use the Include Paths with Nets command to limit analysis to paths that contain specified nets. If a net is not selected, paths through that net are not analyzed. However, if no nets are selected, which is the default, all paths, except those subject to other filtering commands,

are analyzed. To select nets to be included for analysis, use this procedure.

Select **Analyze** → **Analyze Against** → **Filter Paths by Nets (Tab)**.

Excluding Paths with Nets

Use the Exclude Paths with Nets command to exclude paths containing specific nets from analysis, regardless of which paths are specified in the Include Paths with Nets command or other filters. If a net is selected, paths through that net are not analyzed. The default does not exclude any nets from analysis. To exclude specific nets from analysis, use this procedure.

Select **Analyze** → **Analyze Against** → **Filter Paths by Nets (Tab)**.

Path Tracing

Use the Path Tracing command to enable or disable path analysis through delay path types for specific components, such as latches, RAMs, and TBUFs. These paths may be irrelevant to your analysis.

Note This command only applies to FPGAs; it is disabled if a CPLD design is open. (CPLD path timing analysis ignores paths through Set/Reset logic and breaks paths at bidirectional I/O pins.)

After specifying which path types to control through which components, you can generate a Timing Constraints Analysis, Analyze Against Auto Generated Design Constraints Analysis, or Analyze Against User Specified Paths by Defining Endpoints report. Use the following procedure to specify path types through components for path analysis.

Select **Analyze** → **Analyze Against** → **Paths Tracing (Tab)**.

Select the path type that you want to control from the Path Type pull-down list box. Right click on the pull-down menu, then highlight one of the path types. The following types are available.

- Asynchronous
- Set/Reset to Output
- Data to Output for Transparent Latch

- RAM Data to Output
- RAM WE (Write Enable) to Output
- TBUF Tristate Control to Output
- TBUF Input to Output
- I/O Pad to Input
- I/O Tristate Control to Pad
- Bidirectional Tristate I/O Output to Input
- I/O Output to Pad

The Timing Analyzer displays all components that use the specified path type in the Enabled Components or Disabled Components list box, corresponding with the default of that path type. The path type default is the state when you initially open a design or use the Reset All Path Filters command.

1. Enter some text in the Filter field to display a subset of components of the specified type, if desired, and click **Apply**.

   The Filter changes to match the default state of the path type.

2. Click **OK**.

   The Path Tracing dialog box closes. You can now select another filtering command or generate any timing report.

Resetting Path Filters to Defaults

You can reset all of the path filters to the design default settings. After opening a design, select **Path Filters** → **Reset All Path Filters**. To then view the default settings, select **View** → **Settings**.

Using the Console Window

The Console window records all the commands that you have used in a Timing Analyzer session. You can use these commands to form macros. In addition, it provides an alternative to using some menu commands by allowing you to enter commands from the keyboard.

Executing a Command

To execute a command in the Console window, follow these steps.

1. To open the Console window, select **View** → **Console**.

   The Console window appears.

   Note You cannot delete text from within the Console window.

2. You can add a command manually by typing it in the field at the bottom of the window below the Show Command Status box. See the Timing Analyzer Online Help for syntax commands. After you enter the command and press the Return key, the command is executed and is reflected in the Console window.

Re-Executing Commands

If you want to re-execute a command shown in the Console window, you can use one of the following three methods in the field at the bottom of the window below the **Show Command Status** box.

- Type two exclamation points (!!) to repeat the last command.
- Type an exclamation point (!) and the number of the command that appears to the left of the command in the Console window.
- Type in an exclamation point (!) and the first letter or first few letters of the command.
- Use the up or down arrow keys to move to the command, select it, and press the Return key.

  With all these methods, the Timing Analyzer starts the search from the bottom of the command list.

  To see if the system issued a response to the command, such as an error or warning message, click the Show Command Status box.

Using Macros

A macro command is a script file for running Timing Analyzer commands and options. You can create a macro, save it in a new file, the same file, or another existing file, and run it in the Console window. The Timing Analyzer records all commands executed during the current session.

Creating a Macro

To create a macro, perform the following steps.

1. Select **`View`** → **`Console`** to open the Console window.

   Alternatively, you can create or edit a macro manually or create one by entering keyboard commands in a text file.

2. From the menus, select the commands that will constitute the macro or type keyboard commands in the field at the bottom of the window.

   These commands are recorded in the Console window numerically. See the Timing Analyzer Online Help for listings, descriptions, syntax, abbreviations, and examples of keyboard commands.

3. Select **`File`** → **`New Macro`** or click the New Macro button.

   A New Macro window appears.

4. In the Console window, hold down the left mouse button and highlight the sequence of commands that will constitute the macro.

5. Click the Copy Button.

6. Position the cursor in the New Macro window and click the Paste Button.

The lines from the Console window are pasted into the New Macro window.

You can also highlight, copy, and paste individual lines from the Console window to the New Macro window.

You can add text in the New Macro window by inserting the cursor and typing. Delete text by pressing the backspace key or by highlighting and pressing the Delete key.

7. Save the new macro by following the instructions in the "Saving a New Macro" section.

Saving a New Macro

To save a new macro, follow these steps.

1. Make sure the macro that you want to save is the active window by clicking on it. The active window has a colored border.
2. Select **File** → **Save**, or click the Save button.

The Save As dialog box appears.

3. In the Look in / Directories list box, select the directory in which you want to save the macro.
4. In the List Files of Type field, make sure that Timing Analysis macros (*.xtm) is selected. (File names of that format appear in the list box below the File Name field).

   A default name corresponding with the type of information contained in the window (timing constraints, clocks, and so forth), with an .xtm extension appears in the File Name field.
5. In the File Name field, type in a name for your new macro.

   You must save the macro in a file with an .xtm extension.
6. Click **OK**.

   The Save As dialog box closes. You can use word processor applications to open and edit the report file.

Running a Macro

Follow these instructions to run an existing macro.

1. Select **File** → **Run Macro**.

   The Run Macro dialog box appears.

2. In the Look in / Directories list box, select the directory in which the macro file is located. All macro files with an XTM extension are listed in the list box.

3. Click on the macro file in the list box that you want to run.

4. Click **Open**.

   To run a macro already displayed in an editor window, follow these instructions.

5. Click on the window to make it the active window.

6. Click the Run Macro toolbar button.

Editing a Macro

You can also edit an existing macro.

1. Select **File** → **Open**.

   The Open dialog box appears.

2. In the Look in / Directories list box, select the directory in which the macro file is located.

3. In the List Files of Type field, select Timing Analysis Macros (*.xtm) from the pull-down list box.

4. In the File Name field, type in the name of the macro file that you want to open. Alternatively, click on the name of the XTM file in the list box above the File Name field.

5. Click **OK**.

The Open dialog box closes, and the macro window opens and remains active.

6. Edit the macro, using the information in the "Creating a Macro" section to add, delete, copy, and paste commands in the macro window.
7. If you want to save the edited macro in the same file, select **File** → **Save**, or click the Save button.

If you have saved the macro once, the Save command saves the macro in the existing file without activating the Save As dialog box.

If you want to save the edited macro to another file, follow the instructions in the "Saving an Edited Macro to a New File" section.

Overwriting an Existing Macro

If you want to save an edited macro in the same file, follow these steps.

1. Make sure the macro that you want to save is the active window by clicking on it or opening the macro file.
2. Select **File** → **Save**, or click the Save button.

The Save As dialog box appears.

3. In the Look in / Directories list box, select the directory in which the existing macro is located.
4. In the List Files of Type field, make sure that Timing Analysis macros (*.xtm) is selected. (File names of that format appear in the list box below the File Name field).

5. In the File Name field, type in a name of the existing macro, or click on that file name in the list box below the File Name field.
6. Click **OK**.

   The Timing Analyzer displays a prompt box asking if you want to overwrite the existing file, as shown in the following figure.

Saving an Edited Macro to a New File

Follow this procedure to save an edited macro to another file.

1. Make sure the macro that you want to save is the active window by clicking on it or opening the macro file.
2. Select **File** → **Save**, or click the Save button.

   The Save As dialog box appears.
3. In the Look in / Directories list box, select the directory in which you want to save the macro.
4. In the List Files of Type field, make sure that Timing Analysis macros (*.xtm) is selected. (File names of that format appear in the list box below the File Name field).

   A default name corresponding with the type of information contained in the window (timing constraints, clocks, and so forth), with an .xtm extension appears in the File Name field.
5. In the File Name field, type in a name for new macro.

   You must save the macro in a file with an .xtm extension.

6. Click **OK**.

   The Save As dialog box closes. You can use word processor applications to open and edit the report file.

Suppressing Informational Messages

When you run a macro, the commands in the macro file can generate informational, confirmational, and error messages. However, you can suppress the informational and confirmational messages by using the following procedure. You cannot suppress these messages while executing menu commands. This command does not have an equivalent menu command.

1. Open a design, as described in the "Opening a Design" section.
2. Select **View** → **Console**.

   The Console window appears.
3. In the field at the bottom of the Console window, below Show Command Status, type the following command.

   ```
   SetForce on
   ```
4. If you are creating a new macro or editing an existing one, follow the procedure in the "Creating a Macro" section, inserting the **SetForce on** command when you want to suppress messages. (For example, after opening a design.)
5. Select **File** → **Run Macro**, or click the Run Macro Button.

   
6. To restore the informational and confirmational messages, type the following command in the Console window.

   ```
   SetForce off
   ```

Glossary

BEL

A Basic ELement. Basic Elements are the building blocks that make up a CLB, IOB, BLOCK RAM, or TBUF—function generators, flip-flops, carry logic, and RAMs.

CLB

The CLB (Configurable Logic Block) constitutes the basic FPGA cell. The FPGA is an array of CLBs organized in columns and rows on the silicon die. CLBs are used to implement macros and other designed functions. They provide the physical support for an implemented and downloaded design. They have inputs on each side, and this versatility makes them flexible for the mapping and partitioning of logic. See The Programmable Logic Data Book for each device's CLB.

clock input path

A clock input path is a logic transition, which when applied to a clock pin on a synchronous element, captures data. It starts at either an input or an output of the chip, but can also start at other sequential elements. A clock input path propagates through any number of levels of combinatorial logic and ends at any clock pin on a flip-flo / p, latch, or synchronous RAM. These paths do not propagate through synchronous elements. The clock input path time is the maximum time required for the signal to arrive at the clock input of the synchronous element.

clock skew

The difference between the time a clock signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop.

clock-to-pad path

A path starting at the Q output of a flip-flop or latch and ending at an output of the chip. It includes the clock-to-Q delay of the flip-flop and the path delay from that flip-flop to the chip output. The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and arrive at the output.

clock-to-setup path

A path starting at the Q output of a flip-flop or latch and ending at an input to another flip-flop, latch, or RAM, where that pin has a setup requirement before a clocking signal. It includes the clock-to-Q delay of the source flip-flop, the path delay from that flip-flop to the destination flip-flop, and the setup requirement of the destination flip-flop. The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs.

component

A logical configuration that will, at some point, go into a physical site. Examples of components are CLBs, IOBs, tristate buffers, pull-up resistors, and oscillators.

console log

Record of the commands that you invoked during a session.

critical path

The path within a design that dictates the fastest time at which an entire design can run. This path runs from the source to a sink node such that if any activity on the path is delayed by an amount t, then the entire circuit function is delayed by time t.

destination

A sink node or stopping point for a timing analysis path, often the data input of a synchronous element or a pad.

endpoints

A node which acts as either the driver to begin a path or a load to end a path.

filter

A set of limitations or options applied to the timing analysis to more specifically target important items of interest.

fitting

The process of putting logic from your design into physical macrocell locations in a CPLD. Routing is performed automatically, and because of the interconnect architecture, all designs are routable.

high-density function block (HDFB)

A group of macrocells in a CPLD that can efficiently perform complex logic such as arithmetic operations.

hold time

The time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

IOB (input/output block)

A collection or grouping of basic elements that implement the input and output functions of FPGA and CPLD devices.

macro

A physical macro is a logical function which has been mapped into the components of a specific device family. Physical macros are stored in files with the extension .nmc. In addition to components and nets, the file can also contain placement, routing, or both kinds of information. A macro can be unplaced, partially placed, or fully placed.
It can also be unrouted, partially routed, or fully routed. See the "Working with Physical Macros" chapter of the FPGA Editor Guide for information about physical macros.Specific to the Timing Analyzer, a macro is an ASCII file containing a sequence of Timing Analyzer keyboard commands that are executed in script form.

main window

The background against which windows are displayed.

menu bar

The area located at the top of the main window that provides access to the menus.

net

A logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.

offset

Defines the timing relationship between an external clock and its associated data-in or data-out pin.

pad

The physical bonding pad on an Integrated Circuit. All signals on a chip must enter and leave by way of a pad. Pads are connected to package pins in order for signals to enter or leave an Integrated Circuit package.

pad group

A time grouping of pads.

pad-to-pad path

A path starting at an input of the chip and ending at an output of the chip. The pad-to-pad path time is the maximum time required for the data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal.

pad-to-setup path

A path starting at an input of the chip and ending at an input to a flip-flop, latch, or RAM—wherever there is a setup time against a control signal. The pad-to-setup path time is the maximum time required for the data to enter the chip, travel through logic and routing, and arrive at the input before the clock or control signal arrives.

path

An ordered set of elements identifying a logic flow pathway through a circuit. A path may consist of a single net or a grouping of related nets and components. There can be multiple paths (consisting of nets and components) between the two pins. When a component is selected as part of a path, both the input pin to the component and the output pin are included in the path. A path stops when it reaches the data input of a synchronous element (flip-flop) or pad. A path usually starts at the output of a synchronous element or pad.
Paths can be defined by using timing specifications. See the “Using Timing Constraints” chapter of the Development System Reference Guide. In the “Path Example” figure, there are three paths between Pin A and Pin B. One path travels from Pin A through LB2 and through LB6 to Pin B, another travels from Pin A through LB3 and through LB6 to Pin B, and another travels from Pin A through LB4, LB5, and LB6 to Pin B.

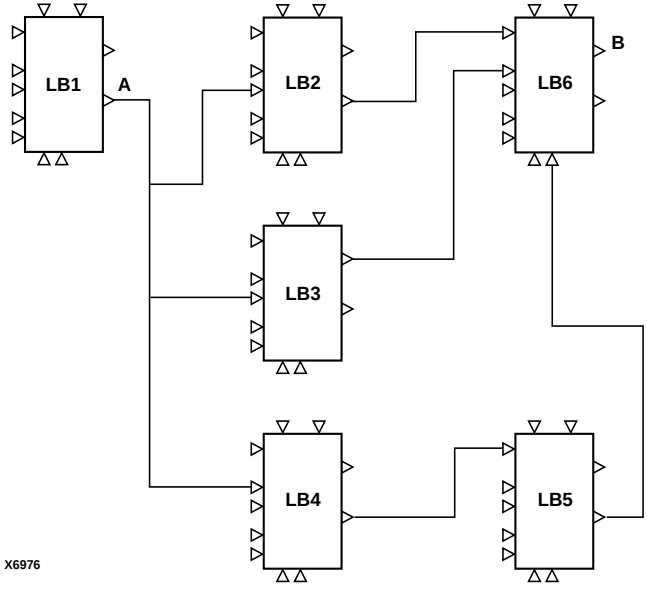


Figure Glossary-1 Path Example

period

The time specified for a clock signal to transition from a state back to

the same state. Also, a requirement placed on the clock signal that the place and route software is expected to meet. The period of the clock is affected by the amount of time it takes the output of one sequential element to pass to the next sequential element in a path.

pin

A symbol pin or package pin. A package pin is a physical connector on an Integrated Circuit package that carries signals into and out of an Integrated Circuit.
A symbol pin, also referred to as an instance pin, is the connection point of an instance to a net.

primitive

A logic element that directly corresponds, or maps, to a basic element.

schematic

A hierarchical diagram representing a design in terms of user and library components.

SDF

Standard Delay Format, which is an industry-standard file format for specifying timing information. It is often used for simulation.

sequential element

A flip-flop, synchronous RAM, or Latch.

setup time

The time relative to a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

slack

The difference between the constraint and the analyzed value, with negative slack indicating an error condition.

source

An output pin that drives a path. Sources are input pads and the outputs of synchronous elements.

static timing analysis

A point-to-point delay analysis of a design network with respect to a given set of constraints. It does not include insertion of stimulus vectors.

status bar

An area located at the bottom of an application window that provides information about the commands that you are about to select or that are being processed.

time group

A collection of design elements, including nets, BELs, components, and so forth that can be used to constrain many objects in the same way.

timing constraints

A series of constraints applied to a given set of paths or nets that dictate the desired performance of a design. Constraints may be period, frequency, net skew, maximum delay between end points, or maximum net delay.

toolbar

A group of buttons with graphic icons located under the menu bar in the application window that provide button access to frequently used commands in pull-down menus.

TRACE

The Timing Reporter And Circuit Evaluator provides static timing analysis of a design based on input timing constraints. Its two major functions are timing verification and reporting.

universal interconnect matrix (UIM)

The routing matrix for CPLD devices. This fully populated switching matrix allows any output to be routed to any input, guaranteeing 100 percent routability of all designs. The UIM can also function as a very wide AND gate, which can allow more logic to be placed in macrocells.

verification

In timing, the process of comparing the desired performance of a design using constraints against the expected performance, based on software models of the device speed and routing delays.

VHDL

An acronym for VHSIC Hardware Description Language (VHSIC is an acronym for Very High-Speed Integrated Circuits) or HDL, which can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level.