Foundation Series ISE 3.3i Release Notes and Installation Guide

About This Manual

This document explains how to install Xilinx Foundation Series™ Integrated Synthesis Environment (ISE) software.

This book also describes how to install the Xilinx online documentation. Information on technical support and known issues of the release is also included.

Note: This Xilinx software release is certified as Year 2000 compliant.

Manual Contents

This manual covers the following topics.

- Chapter 1,“Introduction,” details the titles and contents of the CDs in your Software Package. There is also information about changes to the installation process for this release.
- Chapter 2, “System Requirements,” gives the operating system and memory requirements needed to install and use this software. There are also instructions for various installation configurations.
- Chapter 3, “Installation Instructions,” describes how to install the Xilinx software tools, online documentation, the HDL Bencher™ / StateCAD® Xilinx Edition and the ModelSim™ Xilinx Edition.

- Chapter 4, “Known Issues,” lists the most critical known issues in the ISE Series release at press time.
- Chapter 5, “Software Service and Support,” details how to contact Xilinx for Customer and Technical Support and how to find the most up-to-date information about Xilinx products.
- Appendix A, “Troubleshooting,” describes workarounds to problems you might have when installing the ISE software and documentation.

Additional Resources

For additional information, go to `http://support.xilinx.com`. The following table lists some of the resources you can access from this Web site. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging `http://support.xilinx.com/support/techsup/tutorials/index.htm`
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at `http://support.xilinx.com/support/searchtd.htm`
Application Notes	Descriptions of device-specific design techniques and approaches `http://support.xilinx.com/apps/appsweb.htm`
Data Book	Pages from *The Programmable Logic Data Book*, which contain device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging `http://support.xilinx.com/partinfo/databook.htm`
Xcell Journals	Quarterly journals for Xilinx programmable logic users `http://support.xilinx.com/xcell/xcell.htm`
Technical Tips	Latest news, design tips, and patch information for the Xilinx design environment `http://support.xilinx.com/support/techsup/journals/index.htm`

Conventions

This manual uses the following typographical and online document conventions. An example illustrates each typographical convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: -100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

- Emphasis in text

  If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  edif2ngd [*option_name*] *design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  lowpwr ={**on** | **off**}

- A vertical bar " | " separates items in a list of choices.

  lowpwr ={**on** | **off**}

- A vertical ellipsis indicates repetitive material that has been omitted.

  ```
  IOB #1: Name = QOUT'
  IOB #2: Name = CLKIN'
  .
  .
  .
  ```

- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.

  allow block *block_name loc1 loc2* . . . *locn;*

Online Document

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

Contents

Chapter 3 Installation Instructions

Chapter 4 Known Issues

Chapter 5 Software Service and Support

Appendix A Troubleshooting

Chapter 1

Introduction

This chapter details the titles and contents of the CDs in your Software Package. There is also information about finding software features, software documentation, and Xilinx device architectures supported in this release.

The following sections are in this chapter.

- "Xilinx Software Installation"
- "Software CD Contents"
- "Software Features"
- "Architecture Support"
- "Software Documentation"

Xilinx Software Installation

The following items pertain to software installation in this software release.

Software Updates

Xilinx software Service Packs are available for download at: http://support.xilinx.com/support/techsup/sw_updates/. Please visit this site to see if any newer software updates are available.

Software Registration

In order to complete your software installation, you need to register your software with Xilinx. The registration process follows.

1. During the installation process, you are prompted to obtain your 12 digit Registration ID. You can choose to obtain this Registration ID using one of the following methods shown in Figure 1-1:
   - Web site Registration (fastest method)
   - E-mail
   - Fax

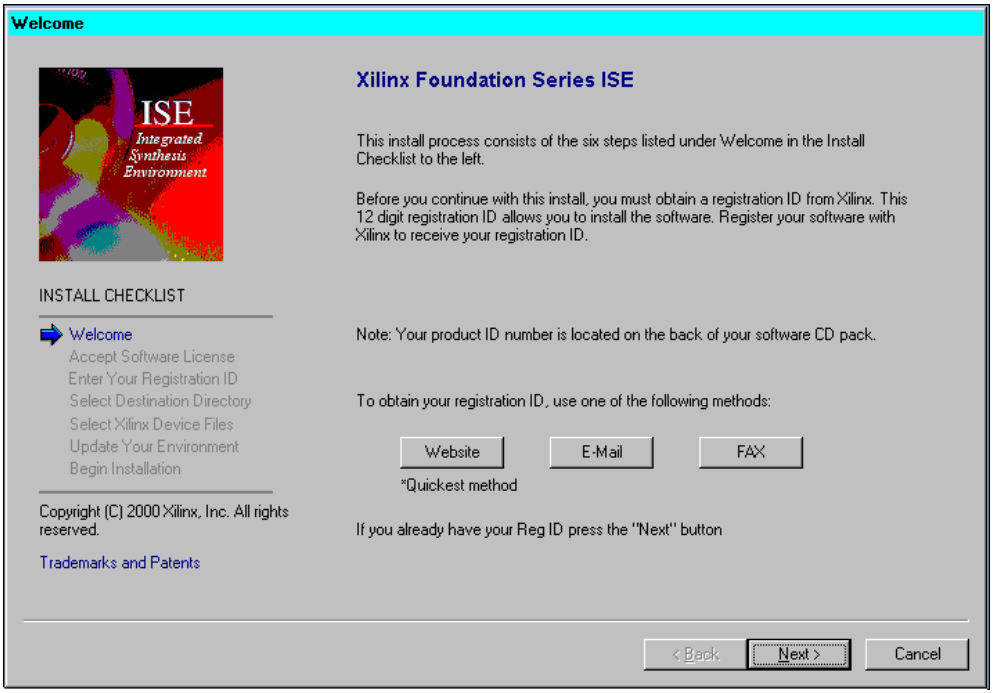

Figure 1-1 Install Checklist for Registration

2. When you fill out the Registration form, you are prompted to enter your Product ID. This ID is located on a sticker which is displayed on the back of the software CD pack.

3. After you have your Registration ID, return to the Software Installation web page and enter this number to complete your installation, as shown in Figure 1-2:

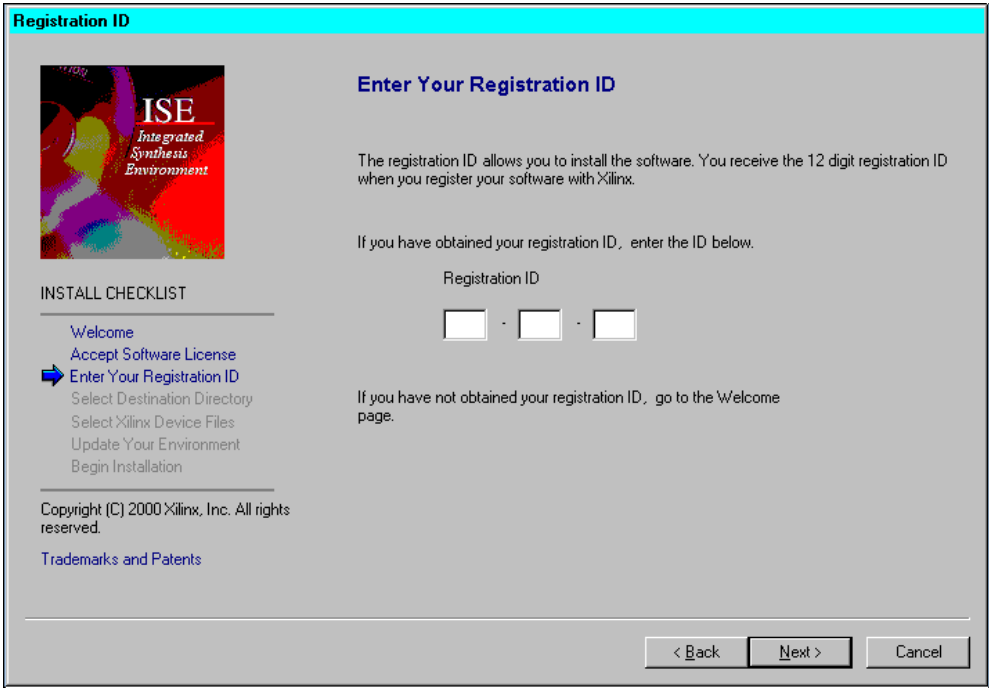

Figure 1-2 Install Checklist - Registration ID

Software CD Contents

This section lists the titles and contents of the CDs in your package. For a complete list of the other items in your box, see the printed "READ ME FIRST Hot Sheet and Welcome Letter."

CD Titles

There are three CDs included in your software folder. The CD titles are as follows.

- Design Environment
  Foundation Series ISE 3.3i
- Documentation
  Foundation Series ISE 3.1i
- ModelSim Xilinx Edition

CD Contents

The general contents of this release are listed in this section. The following table lists the contents of the Design Environment CD.

Table 1-1 Design Environment CD Contents

Software Component
Installation program
Foundation Series ISE 3.3i Design Implementation Tools Software
Marimba's Castanet Tuner™ (for future web downloads of Xilinx software)
Adobe Acrobat Reader 4.05™
README File (TXT)
Key Features File (HTML)
Netscape Navigator 4.72™
Synopsys FPGA Express version 3.5
Perl™ version 5

GNU License Agreement

Xilinx distributes the Perl program with the Foundation Series ISE software. Perl, which is used for the installation of software, is copyrighted by Free Software Foundation, Inc. (1989-1991), and is distributed without warranty of any kind pursuant to the GNU General Public License Agreement, a copy of which is available from Xilinx upon your request. For three years following your acquisition of the Perl program you can request a copy of the Perl source code from Xilinx Customer Support.

The following table lists the contents of the Documentation CD.

Table 1-2 Online Documentation CD Contents

Software Component
Installation Program
Software Manuals (HTML versions)
Software Manuals (PDF versions)
Document Viewer (index.htm), data/html, and /data/system doclinx.com directories)
Netscape Navigator 4.72
Documentation README File (HTML)

Software Features

A list of the key features in this software release can be found by selecting **Start → Xilinx Foundation Series ISE → Documentation → Key Features**. This file is in HTML format, and you must have a Web browser installed to read the file.

The latest versions of software manuals, which are also in HTML format, include information about how to use the software features. The *Foundation Series ISE Quick Start Guide* includes a tutorial which incorporates these features.

Note: You can install the Netscape Navigator Web browser from the Documentation CD.

Note: Windows Emulator's (such as eXceed Emulator) are not supported with Xilinx Software. For more information on this, please reference: `http://support.xilinx.com/techdocs/3578.htm`.

Architecture Support

The software supports the following architecture families in this release.

- Spartan™ / XL / -II
- Virtex™ / -E / -II
- XC9500™ / XL / XV
- XC4000™E / L / EX / XL / XLA

Refer to the *Programmable Logic Data Book* for more information on these devices. The online version is at

`http://www.xilinx.com/partinfo/databook.htm.`

For updated information regarding speed grades and package support, search the Xilinx Answers Database and the latest Application Notes. You can search the technical documentation at

`http://www.xilinx.com/support/searchtd.htm.`

Software Documentation

The resources described in the following sections provide answers to your questions about installing and using the Xilinx Foundation Series ISE software tools.

Note: All installation information is contained in this document. The *Foundation Series ISE Quick Start Guide*, which is the other printed book in your box, contains a tutorial.

Software Manuals Online

Xilinx provides software user manuals for most of its GUI tools, and also for many Foundation EDA vendor interface tools. The manuals may either be installed or viewed directly from the CD by opening the index.htm file on your Documentation CD. You can also access the Software Manuals on the Web through

`http://support.xilinx.com.`

Note: PDF versions of the Software Manuals can also be accessed from the Documentation CD at D:\print\printlist.htm or from the Design Environment CD at D:\documentation\print\printlist.htm.

Online Help

Context-sensitive online help is available for all Xilinx programs that are available with a GUI (Graphical User Interface). Use the **`Help`** → **`Help Topics`** Menu to access the online help, see Figure 1-3.

Figure 1-3 On-Line Help System

Xilinx Support Web Site Resources

There are many resources provided on the Xilinx Support Web site, `http://support.xilinx.com`, including additional software documentation, application notes, software solutions, tutorials, data sheets, and Technical Tips. Click **Library** from `support.xilinx.com` for a complete list of technical documentation.

Chapter 2

System Requirements

This chapter gives the operating system, equipment, and system memory requirements needed to install and use the Foundation Series ISE 3.3i software.

The following sections are in this chapter.

- “Software Installation Requirements”
- “Supported Operating Systems”
- “System Memory Requirements”
- “Special Installation Configurations”
- “Product Configurations”
- “Software Manuals Installation Options”
- “Equipment and Permissions”

Software Installation Requirements

During software installation the sizes of the files you are installing are calculated. You are given the option to select sub-components of each device family in order to tailor your installation to your needs. All file sizes are approximate. Windows users may notice differences between the calculated file sizes and the actual installation footprint on your system. This is due to a difference in the Fat 32 and Fat 16 file partitioning systems which are used by Microsoft platforms.

Supported Operating Systems

The Foundation Series ISE 3.3i software supports the following operating systems and versions

Table 2-1 Supported Operating Systems.

Platform Type	Version Number
Windows	NT 4.0 (with Service Pack 4-6a)
Windows	98 SE / 2000
Japanese Windows	NT
Japanese Windows	98
Chinese Windows	98
Korean Windows	98

Note: The Windows 95 Platform is not supported with this software release.

System Memory Requirements

This section gives the RAM and swap space needed to run Foundation Series ISE 3.3i on your system.

While the following table indicates the system requirements for typical designs, the unique characteristics of each individual design will affect the actual system resources required. Additional memory may be required for certain “boundary-case” or “pathological” designs, as well as for concurrent operation of other applications.

Some designs can be implemented using less than the specified memory while other complicated or large designs may require additional memory. It is recommended that each designer monitor the system resources being utilized and adjust the systems resources if necessary.

The following table gives the memory requirements for PCs:

Table 2-2 Memory Requirements for PCs

Xilinx Device	RAM	Virtual Memory
XC4003E/L through XC4008E/L XC4005XL through XC4008XL XC9536 through XC95216 XC9536XL through XC95216XL	32 MB	32 MB-64 MB
XC4010E/L through XC4025E/L XC4028EX through XC4036EX XC4010XL through XC4028XL XC4085XL XC4013XLA through XC4028XLA Spartan/XL XC95288/XL	64 MB	64 MB-128 MB
XC4036XL through XC4062XL XC4036XLA through XC4085XLA	128 MB	128 MB-256 MB
XC40110XV, XC40150XV XCV50, XCV100, XCV150, XCV200, XCV300, Spartan-II	128 MB	256 MB
XC40200XV, XC40250XV XCV400, XCV600	256 MB	400 MB
XCV800, XCV1000, Virtex E	512 MB	800 MB
XCV1600E, XCV2000E	1 GB	1 GB
XCV2600E, XCV3200E	1.5 GB	2 GB

Note: If you are using Windows NT, you must have Administrator permissions to alter the paging file.

Special Installation Configurations

If you maintain a special configuration of Xilinx and Xilinx partner software on your system, make sure you read the following document for information about which configurations are supported, setting up your user environment, and switching between software versions.

`http://www.xilinx.com/techdocs/8915.htm`

A “special configuration” could be one of the following:

- Xilinx 2.1i and Xilinx 3.x Software tools on the same machine
- A combination of Xilinx 3.x Alliance, Foundation or ISE Software Tools on the same machine
- A combination of Xilinx 3.x software tools and different vendor versions (such as Cadence Concept) on the same machine

Note: Make sure you do not save your design files under the XILINX directory tree; you could accidentally erase your designs. Xilinx recommends an uninstall before the software is updated. You will be prompted by the installation program if a previous version is detected. The installation program will not automatically remove the older tools. If you receive this warning, then you should exit the installation, uninstall the previous versions, and launch the installation again.

Product Configurations

Following is a list of the product configurations for this release:

- Base-Express (DS-ISE-BSX-PC)
- Express (DS-ISE-EXP-PC)
- Elite (DS-ISE-ELI-PC)

All of these configurations contain FPGA Express, StateCAD Xilinx Edition, and HDL Bencher Xilinx Edition Software Versions.

Warning: The installation program will automatically overwrite the previous versions of Xilinx Alliance or Foundation tools on your system, if you install to the same directory.

Software Manuals Installation Options

There are several ways that you can read the Xilinx software manuals. The first time you access the software manuals, you will have to **Grant** access to the Digital Certificate. The following list details your options.

- Install all the manuals to a local or Network drive

  If you install the Software Manuals locally, you will be able to access them through your Foundation Series ISE GUI tools, using the **`Help`** → **`Online Documentation`** menu command.

  Xilinx recommends that you install all the software manuals, not just a partial set. If you install a partial set, you must constrain your searches to only the books you installed. Otherwise search hits may appear for books you did not install. If you want to install the manuals, see the "Installation Instructions," chapter. You must install your Xilinx Implementation Tools before installing the Software Manuals, and they must be installed under the same directory so that the Xilinx variables are set properly.

- Read the manuals from the Documentation CD

  Use this option if you have slow internet access or are accessing the documentation away from the office.

  After verifying that you have the appropriate Web browser installed, go to your CD directory and open the "index.htm" file in your browser window. The documentation viewer will start, opening with the Table of Contents in the left-hand frame.

- Read the manuals on the Web

  If you have fast internet access, you can read the manuals on the Web. The books are optimized for fast internet viewing.

  Go to the Software Manuals Online Web page, which is part of the Xilinx Support Web site at

  `http://support.xilinx.com.`

  Click the **`Software Manuals`** button in the left-hand column.

Online software manuals include the following:

- *Constraints Editor Guide*
- *CORE Generator Guide*
- *Development System Reference Guide*
- *Floorplanner Guide*
- *Foundation Series ISE 3.1i User Guide*
- *Foundation Series ISE 3.1i Quick Start Guide*
- *FPGA Editor Guide*
- *Hardware Debugger Guide*
- *Hardware User Guide*
- *JTAG Programmer Guide*
- *Libraries Guide*
- *LogiBLOX Guide*
- *PROM File formatter Guide*
- *Synthesis and Simulation Design Guide*
- *Timing Analyzer Guide*
- *Synopsys VHDL Reference Guide* (PDF only)
- *Synopsys Verilog Reference Guide* (PDF only)
- *XST User Guide*

Equipment and Permissions

The following table provides information about related equipment, permissions, and network connections:

Item	Requirement
Directory Permissions	Write permissions must exist for all directories containing design files to be edited.
Hardware Component	Xilinx recommends that you have an IBM- compatible Pentium class machine.
Monitor	Color VGA operating at the following modes. Minimum Resolution: 640 x 480 Minimum Recommended: 1024 x 768
Mouse	You should have a 2-button (Microsoft Windows compatible) or 3-button (Microsoft Windows compatible) mouse.
CD Drive	You should have an ISO9660 compliant drive on your system.
Ports	You should have two ports (one for a mouse and one parallel port for the parallel download cable, if needed).
Network Compatibility	The Xilinx installation program supports TCP/IP networks. If you are using a Windows NT operating system, then the TCP/IP protocol needs to be installed first. For more information, see the solution record at the following location: `http://support.xilinx.com/techdocs/2510.htm`

Chapter 3

Installation Instructions

This document describes how to install the Xilinx software tools, online documentation, and Xilinx ALLSTAR Program software consisting of HDL Bencher / StateCAD and ModelSim Xilinx editions, as well as how to set up the system environment to be able to run the tools. This chapter is comprised of the following sections.

- "Installation Types"
- "Step 1: Install Xilinx Software"
- "Step 2: Licensing FPGA Express"
- "Step 3: Install Xilinx ALLSTAR Program Software"
- "Step 4: Install Online Documentation"
- "Network Installations"
- "Adding Devices and Software Updates"

Installation Types

There are three types of installs that are supported with the Xilinx Foundation Series ISE 3.3i software:

1. Local Install: The Xilinx 3.3i software is installed to the local hard drive.
2. Server Install: The Xilinx 3.3i software is installed to a remote drive on the network.
3. Network Install: The Xilinx 3.3i software already exists on the network. (This was accomplished through #1 or #2 above). The client machine needs to be set up to point to this installation.

Both the first and second options are treated the same in the Xilinx 3.3i Installer. When prompted by the installer to specify a destination directory, simply select the desired location, either local or remote. Then proceed with the installation instructions in the following sections.

If you are doing a network install, then you should read the instructions in the "Network Installations" section.

Note: There is no Lab Installation in this release.

Step 1: Install Xilinx Software

This section explains how to install the Foundation Series ISE 3.3i software.

1. You should close all programs before you begin installation.
2. Ensure that your system meets the requirements described in the "System Requirements" chapter.
3. Check the "Known Issues" chapter for any installation issues that pertain to your system or configuration.
4. Insert the Design Environment Foundation Series ISE 3.3i CD.
5. Run the installation program.

   Using Windows Explorer, select **`Start`** → **`Run`**. Type **`D:\setup.exe`** in the Open field of the Run window and click **`OK`**. (If your CD drive is not the "d" drive, substitute the appropriate drive designation.)

   Follow the instructions on the screen to install the software. You will be asked to register the product from the Welcome screen during install. You can register via the web, e-mail, or fax.

   In order to register the product, you need to provide the following information:

   - Product ID

     Your product ID number is located on the back of your software CD pack.

   - Your name
   - Company

- Mailing address
- Phone number
- E-mail address

When you register, Xilinx gives you a Registration ID. You must have the registration ID in order to complete the installation.

The installer first installs all of the Xilinx software and documentation and then invokes the installer for FPGA Express. Your FPGA Express synthesis FlexLM license file will be e-mailed to you.

You need to reboot your PC to allow the environment variables and path statement to take effect before you can run any of the ISE design implementation tools.

6. **Networked Installations:** If you have installed the software to a networked location, make sure that your client machines are set up properly. Refer to the "Network Installations" section for more information.

Step 2: Licensing FPGA Express

The FPGA Express software requires that a FlexLM license file be present on the machine and placed in the location pointed to by the `LM_LICENSE_FILE` environment variable. After you have completed the online registration during the installation process, a valid license file is emailed to you. Place this license file on your disk and set the `LM_LICENSE_FILE` variable to point to it as follows:

```
set LM_LICENSE_FILE=path_to_license\license.dat
```

Make sure the *`path_to_license`* is the path to the directory containing the license file, for example, `C:\Flexlm`.

The Foundation Series ISE installer also delivers a *Load and Go* license file to `%XILINX%\data\license.dat`. This Load and Go license provides full synthesis functionality within the Foundation ISE environment, but does not authorize use of the FPGA Express Constraints Editor, Schematic Viewer, or stand-alone FPGA Express GUI. To use this Load and Go license, be sure that your `LM_LICENSE_FILE` environment variable is pointing to the file as follows:

```
set LM_LICENSE_FILE=%XILINX%\data\license.dat
```

Step 3: Install Xilinx ALLSTAR Program Software

This section provides you with instructions for installing your ALLSTAR tools, ModelSim, HDL Bencher, and StateCAD.

If you already have installed versions of HDL Bencher, StateCAD, or a ModelSim simulator, please refer to the "Using Other Versions of ModelSim, HDL Bencher, and StateCAD" section.

Installing ModelSim Xilinx Edition Software

For complete product and purchasing information for ModelSim Xilinx Edition, contact your local Xilinx representative or visit the following Xilinx web site:

```
http://www.xilinx.com/products/software/mxe.htm
```

To install a 30-day evaluation of ModelSim Xilinx Edition software, perform the following steps:

1. Insert the ModelSim Xilinx Edition CD.
2. Select **Start** → **Programs** → **Xilinx Foundation Series ISE** → **Partner Products** →**Install ModelSim Xilinx Edition**
3. Select the Evaluation Edition.
4. Follow the instruction on the screen to complete the installation.
5. Select "yes" when asked to "Complete the license request process following setup?".
6. Complete the license request form and submit it

   You will be emailed a 30- day license file.
7. Copy the contents of the license.dat file. Paste it to the location where the LM_LICENSE_FILE points.
8. Remove the ModelSim Xilinx Edition CD .
9. Visit http://support.xilinx.com/mxelibs to download the latest MXE simulation libraries.

Installing HDL Bencher and StateCAD Software

HDL Bencher provides automatic testbench generation and StateCAD provides graphical state diagram entry. These software programs may be installed by invoking their respective installers from the Design Environment Foundation Series ISE 3.3i CD.

1. Insert the Design Environment Foundation Series ISE 3.3i CD. If the installer automatically starts, quit the ISE installation program.
2. To install the HDL Bencher, select **Start** → **Programs** → **Xilinx Foundation Series ISE** → **Partner Products** → **Install HDL Bencher Xilinx Edition**.

   Follow the instructions on the screen to install the product.
3. StateCAD is included with Foundation Series ISE 3.3i to facilitate design entry, debug, and analysis of state machines. StateCAD includes a translation tool for importing designs originally created with the Xilinx Foundation State Editor. StateCAD significantly enhances state machine design through its FSM, and Logic Wizards. StateCAD generates FPGA optimized and error-free HDL. It also detects hundreds of logic errors and warnings up-front, and provides solutions for them before it generates any HDL.

   To install the StateCAD software, select **Start** → **Programs** → **Xilinx Foundation Series ISE** → **Partner Products** → **Install StateCAD Xilinx Edition**.

   Follow the instructions on the screen to install the product.

Using Other Versions of ModelSim, HDL Bencher, and StateCAD

You can integrate non-Xilinx Editions of ModelSim, HDL Bencher, and StateCAD with ISE as follows.

1. Within the Project Navigator, select **Edit** → **Preferences** and then select the Partners tab. The following dialog box is displayed:

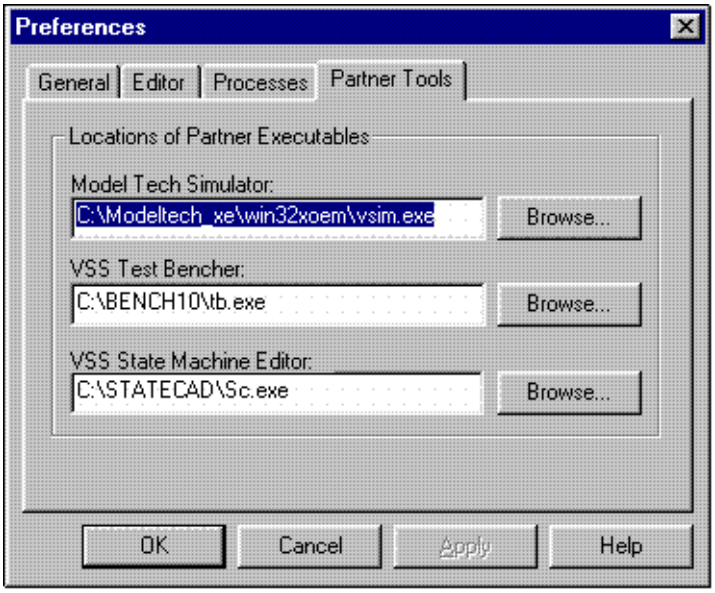

Figure 3-1 Preferences Dialog Box

2. Enter the full path name to each of your tools or browse to the location of the desired executable (that is, `vsim.exe` for the Modeltech Simulator, `tb.exe` for the VSS Test Bencher, and Sc.exe for the VSS State Machine Editor).

Step 4: Install Online Documentation

This section explains how to install the online documentation onto your system. You can also read the software manuals online at

`http://support.xilinx.com.`

You may install the documentation from either the Design Environment CD or from the Documentation CD. From the Design Environment CD installer, the documentation is a selectable option in the main installer. The following section details the installation procedure from the Documentation CD.

Warning: This section assumes that you have already installed the Foundation Series ISE 3.3i software. You must use the same destination directory for both the Foundation ISE software, the Software Manuals, and the online documentation viewer. If you do not use the same directory, you will not be able to access the manuals from the **Help** menu of your GUI tools.

The following list details the installation procedure.

1. Insert the Documentation CD.
2. Run the installation program.

   From Windows Explorer, select your CD drive and open the **NT** folder. Double-click the **setup.exe** file.

   It is recommended that you install all of the books. If you do not, the search functions of the online document viewer will not work properly.
3. Start your online viewer using the following method.

   From the Foundation GUI tool, select the **`Help` → `Online Documentation`** menu command.

   When you start the online document viewer, you will see a "Digital Certificate" screen. Click **Grant** and enable the "Remember this decision" checkbox so this certificate does not appear every time you access the online viewer tool.

   For Online help and more instructions about using the new document viewer, click **Help** in the upper left-hand corner when the screen is loaded. To search the manuals, click **Search**.

Warning: When the online viewer opens in your web browser window, do not attempt to resize the window until the information is completely loaded. Otherwise, your browser window may hang. If this happens, close and then restart your browser.

Network Installations

This section gives more information about setting up your networked installation properly for all of the clients on the network. A client install means that the Xilinx 3.x tools already exist on the network, and you need to set up a client machine to point to this installation.

Make sure your users have set up the appropriate variables as described in this section and the *Foundation Series ISE Release Notes and Installation Guide*, and refer to the following sections for more information.

PC Networks

If you have installed the Foundation Series ISE 3.3i software tools to a PC network, make sure that your users know the location of the software tools and have access to the installation directory.

Once the software has been installed to the network location, the client machines need to be setup to point to the remote location as well as to set local registry settings and program groups and icons.

There is an executable that resides in the install location on the network which will perform the necessary local client system modifications. From the local client machine, browse to the following directory: *network_install_location* / bin / nt and run the program setXenv.bat.

This will set up your environment and all needed registry settings in order to run the Xilinx tools from the remote location

Adding Devices and Software Updates

Xilinx 3.x Software Updates (also called Service Packs) will be made available on the `support.xilinx.com` web site. Instructions for your platform are given when you install the Service Packs.

If you wish to add a device family to your existing Foundation Series ISE Software tools installation, you must run the installation program and reapply the service pack

If you wish to uninstall a Service Pack, you should re-install the 3.3i Software tools, and then install the Service Pack(s) that you desire.

Chapter 4

Known Issues

This chapter lists the most critical known issues in the Foundation Series ISE release at press time.

The following sections are in this chapter.

Finding All Known Issues

For a complete, up-to-date listing of Known Issues, go to the Xilinx Technical Support Web site at `http://support.xilinx.com` and use one of the following methods.

- Look for solutions about a specific software tool

  The "Technical Tips" area provides updated lists of the top and hot issues of each software release. These lists are organized by CAE tool, implementation tool, and design flow step. The following location is the Technical Tips index. Go to the following location and click the link for the tool you are using.

  `http://support.xilinx.com/support/techsup/journals/index.htm`

  "Technical Tips" used to be the "Expert Journals" section on the Technical Support Web site.

- Use "Answers Search" to search the Solutions Database

  The advanced answers search form and a link to the Solutions Database are located at the following URL.

  `http://support.xilinx.com/search/searchtd.htm`

Installation Issues

You can check the following places for software installation known issues. For installation instructions, see the printed document included in your software box. For installation tips, see the "Troubleshooting" Appendix.

1. Read the brightly colored "READ ME FIRST Hot Sheet and Welcome Letter" which is included in your software package.
2. Install Problem Solver

   `http://www.support.xilinx.com/support/troubleshoot/psolvers.htm`
3. Xilinx Answer Browser at

   `http://www.xilinx.com/support/ansbrowse.htm`
4. Xilinx Answers Search at

   `http://www.xilinx.com/support/searchtd.htm`

5. Title: 3.1i Foundation ISE Install - Closing the README after the Synopsys Installation Aborts the Foundation ISE Install

   Description: At the end of the Foundation ISE 3.1i Synopsys install, the user is prompted with the option of viewing the Synopsys readme. If this readme is viewed, and the user dismisses the Synopsys InstallShield Installation with the 'X' in the corner, a dialog is prompted that states “Do you want to exit install?”

   If the user does exit, the install will not complete successfully.

   Reference: http://support.xilinx.com/techdocs/8159.htm

Design Entry Project Navigator Issues

The following issues pertain to Design Entry Project Navigator:

1. Title: 3.1i Foundation ISE: Multiple entity/architecture pairs defined in one source file not displayed.

   Description: Source files containing multiple pairs of entity/architecture definitions are not correctly displayed. Only the last entity/architecture in the file is displayed in Module view.

   Reference: http://support.xilinx.com/techdocs/9095.htm

2. Title: 3.1i Foundation ISE: Printing from Report Browser requires user to specify font.

   Description: Users are required to specify a font each time a report or file is printed from the Report Viewer.

   Reference: http://support.xilinx.com/techdocs/9108.htm

3. Title: 3.1i Foundation ISE: 'Delete Implementation Data' does not delete Express files or directory

   Description: The 'Delete Implementation Data' menu pick does not delete the FPGA Express files or directory.

   Reference: http://support.xilinx.com/techdocs/9124.htm

4. Title: 3.1i Foundation ISE: Using user defined packages in VHDL files

   Description: The VHDL language is compile order dependent, so users who want to have packages utilized by entities must consider the following.

   Reference: http://support.xilinx.com/techdocs/9131.htm

5. Title: 3.1i Foundation ISE: Remote source file causes inconsistent behavior

   Description: When a source file from another directory is added to a project and synthesis fails, users will see inconsistent error reporting.

   Reference: http://support.xilinx.com/techdocs/9133.htm

6. Title: 3.1i Foundation ISE: Project Navigator does not recognize functions included in HDL files

   Description: When source files containing functions are added to the project a red? is displayed next to the function name. The red? indicates that Project Navigator can not find a matching entity or module declaration.

   Reference: http://support.xilinx.com/techdocs/9134.htm

7. Title: 3.1i Foundation ISE: Removing source file, causes cursor to jump to the next file

   Description: When deleting source files, a dialog is displayed with the following question, “Remove Selected File?” and two buttons “Yes” and “No”.

   However, the file selected in the source window is not the file originally selected to be deleted. The problem is that once the delete key is hit or the remove menu pick is selected, the cursor is moved to the next file.

   Reference: http://support.xilinx.com/techdocs/9135.htm

8. Title: 3.1i Foundation ISE: Symbol generator does not preserve the case of the Verilog modules

   Description: When the “Create Schematic Symbol” process is run on a Verilog Module, the component names are generated as lower-case names. This can result in synthesis errors because the associated components will not be found.

   Reference: http://support.xilinx.com/techdocs/9259.htm

9. Title: 3.1i Foundation ISE: Edit UCF File does not open user specified ucf files

   Platform: Win98 - CPLD Only

   Description: Running the “Edit UCF File” process can result in the following error: cannot open C:*path*\\file.ucf

   This is caused when user created UCF file is specified in the Translate Options.

   Reference: http://support.xilinx.com/techdocs/9260.htm

10. Title: 3.1i Foundation ISE: Back-annotated Pin locations Process fails with exit code: 0002

    Description: Running the Back-annotated Pin locations Process with long source file names or deep design paths causes the following error: failed with exit code: 0002

    Reference: http://support.xilinx.com/techdocs/9273.htm

11. Title: 3.1i Foundation ISE: File → Save As does not copy Coregen files

    Description: File → Save As copies the project source files but does not copy the Coregen implementation and project files. This will result in NGDBuild unexpanded block errors.

    Reference: http://support.xilinx.com/techdocs/9290.htm

12. Title: 3.1i Foundation ISE: NGDAnno output is not displayed in the transcript window

    Description: When the “Simulate Post Route HDL Model” is run, NGDAnno and NGD2VHDL or NGD2VER is run to create a timing simulation netlist. The output of NGDAnno is not written to the console window.

    Reference: http://support.xilinx.com/techdocs/9291.htm

13. Title: 3.1i Foundation ISE: Implementation Status incorrectly displayed when a process fails

    Description: If the Implement Design process is run and synthesis fails, a red checkmark is placed on Implement Design and not synthesis.

    Reference: http://support.xilinx.com/techdocs/9317.htm

14. Title: 3.1i Foundation ISE: Checkmarks on top level module not updated when a sub-module is changed

    Description: Checkmarks on the top level module are not properly updated when lower level module is changed.

    Reference: http://support.xilinx.com/techdocs/9318.htm

15. Title: 3.1i Foundation ISE: New Project dialog may take several seconds to open.

    Description: When selecting File → New Project in Project Navigator, it may appear that the system is hung since the dialog can take several seconds to open. Additionally, after closing the dialog, it can again take several seconds for the dialog to close and the project to open in Project Navigator.

    Reference: http://support.xilinx.com/techdocs/9368.htm

16. Title: 3.1i Foundation ISE: Double clicking on XCO file from within Project Navigator fails.

    Description: In Project Navigator, when a Coregen module is generated, the associated XCO file is added to the project. Double clicking on the XCO reloads Coregen with the Core information and allows you to change any parameters and regenerate.

Xilinx Synthesis Technology (XST) Issues

The following issues pertain to the Xilinx Synthesis Technology:

1. Title: 3.1i XST: ERROR: (VLG__5002). top.v Line xx. Component 'component_name' is not in up, down, or top-level path

   Description: Hierarchical names are not currently supported (contrary to the XST Users Guide).

   Reference: http://support.xilinx.com/techdocs/6687.htm

2. Title: 3.1i XST: Done: failed with exit code: 0002. --ISE and Web Pack installed on the same computer

   Description: ISE and Web Pack can have coexistence issues.

   Reference: http://support.xilinx.com/techdocs/6688.htm

3. Title: 3.1i XST: ERROR: (VHP__0854). The expression can not be converted to type std_logic_vector.

   Description: XST will generate an error when encountering an UNSIGNED to STD_LOGIC_VECTOR conversion.

   Reference: http://support.xilinx.com/techdocs/8333.htm

4. Title: 3.1i XST: XST evaluates "?" in case statements as a don't care.

   Description: In the Verilog Language "?" is defined to represent a don't care "-". However most synthesis tools do not support the use of a "?" and evaluate it as false.

   Reference: http://support.xilinx.com/techdocs/8335.htm

5. Title: 3.1i XST: How do I add the IOB=TRUE attribute to output flip flops in XST?

   Description: The IOB=TRUE attribute currently must be applied to the internal signals driven by flip-flops in order to be processed. (If the attribute is placed on the port signal, it gets applied to the I/O buffer). This methodology works for input flops, output tristate flops, and output flops that will be tristated, but not direct output flops.

   Reference: http://support.xilinx.com/techdocs/8904.htm

Engineering Capture System (ECS) Issues

The following issues pertain to the Engineering Capture System:

1. Title: 3.1i ECS: ERROR:NGDBuild:455 - logical net 'xxx' has multiple drivers

   Description: The following NGDBuild errors:

   ERROR:NGDBuild:467 - output pad net 'xxxx' has an illegal buffer

   ERROR:NGDBuild:455 - logical net 'xxxx' has multiple drivers

   can be caused by the following:

   - Using IO macros in an ECS schematic (IBUF4, ILD_1, etc)
   - Naming two driving nets the same name

   Reference: http://support.xilinx.com/techdocs/9306.htm

2. Title: 3.1i ECS: Schematic must be saved in order to Push or Pop into new symbols

   Description: Push/Pop mode is not functional or new symbols because the ECS hierarchy is handled by Project Navigator. If the schematic has not been saved, Project Navigator does not know the symbol has been placed; therefore, Push/Pop does not work.

   Reference: http://support.xilinx.com/techdocs/9307.htm

3. Title: 3.1i ECS: Case not preserved in HDL netlist written by ECS

   Description: When the HDL netlist is written by ECS, all symbol names are written to lower case. This can result in synthesis errors because the associated components will not be found.

   Reference: http://support.xilinx.com/techdocs/9308.htm

4. Title: 3.1i ECS: decode32 and decode64 have incorrect port type (virtex_macro_comp.vhd)

   Description: When utilizing the decode32 or decode64 components, the following errors will be generated.

   XST: ERROR: (VHP__1411) Parameter my_out of mode out cannot be associated with a formal parameter of mode inout.

   ERROR: (VHP__0900) The label i10 is not declared.

   FPGA Express: Error: Ports of mode OUT or LINKAGE can not be read. (VSS-793) Syntax Errors

   Reference: http://support.xilinx.com/techdocs/9314.htm

Translation Issues

The following issues pertain to Translation:

1. Title: 3.1i NGDBuild - NGDBuild crashes on Win95 machines

   Platform: Win95

   Description: Running 3.1i NGDBuild on a Windows 95 machine may result in various errors.

   Reference: http://support.xilinx.com/techdocs/8623.htm

FPGA Express Issues

The following issues address FPGA Express:

1. Title: 3.1i .SCF file contains exported constraints when using Block Level Incremental Synthesis flow with FPGA Express.

   Description: Constraints that are normally written to the .NCF file by Express are instead written to a .SCF when the Block Level Incremental Synthesis flow is used. The .SCF file is not read automatically by the Xilinx implementation tools, and therefore the contents of the file must be manually copied into the user's .UCF file.

   Reference: http://support.xilinx.com/techdocs/9365.htm

2. Title: 3.1i Netlists always are always rewritten when using Block Level Incremental Synthesis with the FPGA Express flow in ISE.

   Description: The timestamps on all design netlists are updated when using FPGA Express BLIS feature inside of ISE. Unchanged modules are not resynthesized, however, therefore providing the desired functionality for BLIS.

   Reference: http://support.xilinx.com/techdocs/9366.htm

FPGA Implementation Issues

The following issues pertain to FPGA device implementation.

1. Title: 3.1i Floorplanner - The IBUFG placement is not verified by DRC check

   Description: The Floorplanner DRC does not verify the IBUFG placement.

   If placed in the wrong location, MAP fails with the following:

   ERROR:xvkpu - The symbol clk.pad failed to join a global clock I/O component as required. The symbol has a constraint (LOC=B0) that specifies an illegal physical site for the component.

   Reference: http://support.xilinx.com/techdocs/6164.htm

2. Title: 3.1i FPGA Editor - When adding probes to Virtex, the banking information is required.

   Description: When adding a probe to a Virtex design, the I/O banking information is not used and it leaves the particular I/O unchecked

   Reference: http://support.xilinx.com/techdocs/6413.htm

3. Title: 3.1i Floorplanner allows illegal BUFG placement.

   Description: The Floorplanner allows the BUFG to be placed in a position on the die that is not closest to the pin that is driving it. For example, the BUFG could be at one corner of the die while the pin driving it is at the opposite side of the die.

   Reference: http://support.xilinx.com/techdocs/6510.htm

4. Title: 3.1i FPGA Editor - DesignRules:9, 10 - Netcheck: The signal "netname" is completely unrouted after drag and drop

   Description: FPGA Editor allows one to move placed components by right clicking, dragging and dropping components into new locations. However, when performing this operation, the following warning may be issued:

   WARNING: DesignRules: 9 - The signal "netname" is only partially routed

   WARNING: DesignRules: 10 - The signal "netname" is completely unrouted

   Reference: http://support.xilinx.com/techdocs/9007.htm

5. Title: 3.1i FPGA Editor - End block command does not work in script playback

   Description: In FPGA Editor playback mode, the end block command will close a Logic Cell after it has been edited. This command works fine when run from the command line, but fails whenever run from the playback script option.

   Reference: http://support.xilinx.com/techdocs/9009.htm

6. Title: 3.1i Floorplanner - Error Portability 3: application has run out of memory or Segmentation Fault

   Description: After implementing a large design (V2000E), starting Floorplanner results in "Error Portability 3: Application has run out of memory or Segmentation Fault."

   Reference: http://support.xilinx.com/techdocs/9033.htm

7. Title: 3.1i Floorplanner - Replace with Placement crashes with large v2000e design

   Description: After implementation of a large design (V2000E), selecting the "Replace with Placement" menu item crashes the tool with a Dr. Watson or Segmentation Fault.

   Reference: http://support.xilinx.com/techdocs/9034.htm

8. Title: 3.1i Floorplanner - Splash / Title Screen is displayed for too long of a time

   Description: The splash screen appears to be displayed for a lengthy period of time when the Floorplanner is loading a large design (i.e - V2000E). When attempting to access other windows, the splash screen continues to overlay others.

   Reference: http: / / support.xilinx.com / techdocs / 9035.htm

CPLD Implementation Issues

The following issues pertain to CPLD Implementation tools:

1. Title: 3.1i XC9500 Hitop / Hprep6 - PROHIBIT property does not exclude pins from "Programmable Ground Pins" option

   Description: All unused I / O pins, including those with a PROHIBIT property, will be connected to the device's internal ground network.

   Reference: http: / / support.xilinx.com / techdocs / 4100.htm

2. Title: 3.1i XC9500 Hitop - Global OFFSET timespec is not supported

   Description: The global OFFSET attribute is not yet supported in XC9500 Family designs.

   Reference: http: / / support.xilinx.com / techdocs / 5999.htm

3. Title: 3.1i XC9500 Chipviewer - Printing capabilities are not currently supported

   Description: Chipviewer does not support printing at this time.

   Reference: http: / / support.xilinx.com / techdocs / 8744.htm

4. Title: 3.1i 9500XV Hitop - Only LVTTL bi-directional signals allowed

   Description: The software currently only allows bi-directional pins to have voltage standard of LVTTL.

   Reference: http: / / support.xilinx.com / techdocs / 9004.htm

5. Title: 3.1i XC9500 Hitop - Multiple sites for single signal not allowed.

   Description: FPGAs allow you to give multiple sites for a signal to be pin locked to. This feature is not supported in this version of software for the XC9500 family.

   Reference: http://support.xilinx.com/techdocs/9017.htm

Timing & Constraints Issues

The following known issues relate to timing and constraints:

1. Title: 3.1i Timing Analyzer - Timing Analyzer Auto Generated Analysis loses Pad to Setup paths

   Description: If you run an Auto Generated Timing Analysis disabling io_pad_i, then run another with it enabled no OFFSET IN constraint is generated.

   Reference: http://support.xilinx.com/techdocs/7437.htm

2. Title: 3.1i Trace/Timing Analyzer - OFFSET/OUT/BEFORE when register clocks static data results in an error.

   Description: During analysis, the tool issues an error when a period can't be found for a static register to do the calculation of an OFFSET OUT BEFORE.

   Reference: http://support.xilinx.com/techdocs/8667.htm

3. Title: 3.1i Constraints Editor - Not able to modify FROM TO constraints for tpthru or delete tpthru

   Description: Constraints Editor does not allow the following modification: Creating a TPTHRU group constraint with a FROM TO, then deciding to disable or delete the TPTHRU or FROM TO

   Reference: http://support.xilinx.com/techdocs/8668.htm

4. Title: 3.1i Trace / Timing Analyzer - FATAL_ERROR: Timing: bastwprcntl.c: 1922:1.27

   Description: When running timing analysis, the user gets the following message: FATAL_ERROR:Timing:bastw-prcntl.c:1922:1.27 - There is no PERIOD constraint for the OFFSET constraint TIMEGRP "OPADS" OFFSET = OUT 25 nS BEFORE COMP “CLK”;. Process will terminate.

   Reference: http: / / support.xilinx.com / techdocs / 8675.htm

5. Title: 3.1i Constraints Editor - “Not yet implemented.” message appears when clicking Help button

   Description: The error message dialog box, “Not yet implemented.” appears when clicking Help button in New and Open dialog box.

   Reference: http: / / support.xilinx.com / techdocs / 8869.htm

6. Title: 3.1i Timing Analyzer -Offset Constraint Specified with No Period Causes Core dump during Advanced Analysis

   Description: When trying to do an advanced analysis on a design with no period constraint and only an offset constraint specified Timing Analyzer Core dumps.

   Reference: http: / / support.xilinx.com / techdocs / 8877.htm

7. Title: 3.1i Timing Analyzer - Slave clock 'club' is not available as port for creating offsets for LVDS

   Description: In Timing Analyzer, when you select Analyze → Analyze Against User Defined Paths by Defining Clock and IO Timing, the slave clock of 'club' of an LVDS pair is not available as a port for creating offset constraints.

   Reference: http: / / support.xilinx.com / techdocs / 8963.htm

CORE Generator and IP Modules Issues

The following issues pertain to the CORE Generator System tools and IP Modules.

1. Title: 3.1i Coregen - Some IP customization GUIs may not fit on PC screens set to 800 x 600 resolution.

   Description: Using CORE Generator 3.1i on a PC some GUIs may not fit on the PC screens when the resolution is set to 800 x 600.

   Reference: http://www.xilinx.com/techdocs/5977.htm

2. Title: 3.1i Coregen - Not all user-specified XCO parameter settings are loaded when launching an XCO file in Project Navigator

   Description: When you launch Coregen by clicking on an XCO file for a Core in Project Navigator, not all of the XCO parameters are loaded into the Core customization GUI (many remain at their default settings). If you do not notice that this is happening, you may end up generating a Core with incorrect settings.

   Reference: http://www.xilinx.com/techdocs/8823.htm

3. Title: 3.1i Coregen, DISTRIBUTED MEMORY: Unable to open file for Memory Initialization: MIF file - radix error: <value>

   Description: Using the 3.1i CORE Generator (or C_IP4). Creating a Distributed Memory (Version 1.0.2 or 1.0.3), CORE Generator is unable to open the (MIF) Memory Initialization File when the format is not binary. If a HEX or decimal format must be specified, a parameter in the.COE file can be used.

   Reference: http://www.xilinx.com/techdocs/8873.htm

4. Title: 3.1i Coregen, VHDL - Unison library must be compiled before Xilinx Core Lib components

   Description: Using CORE Generator 3.1i VHDL flow, the Xilinx UNISIM library components must be compiled before compiling the Xilinx Core Lib components.

   Reference: http://www.xilinx.com/techdocs/8966.htm

5. Title: Some Cores within CORE Generator may require more than 128MB of memory

   Description: Using the CORE Generator some larger Cores may fail to create the EDIF implementation netlist. This may be the result of CORE Generator needing more memory when generating the module.

   Reference: http://www.xilinx.com/techdocs/8970.htm

6. Title: 3.1i Foundation ISE: Coregen ECS Symbol is not generated by default

   Description: After a Core has been created Project Navigator creates an ECS symbol and adds the XCO file to the project. This does not happen if the options in CORE Generator are opened.

   Reference: http://support.xilinx.com/techdocs/9263.htm

7. Title: 3.1i Foundation ISE: Coregen ECS Symbol is not generated by default for Fixed Point Cores

   Description: After a Core has been created Project Navigator creates an ECS symbol and adds the XCO file to the project. This does not happen for Fixed-Point Cores.

   Reference: http://support.xilinx.com/techdocs/9264.htm

8. Title: 3.1i Foundation ISE: Coregen Instantiation Template included in the Language Templates is incorrect.

   Platform: Win98

   Description: After a Core has been created Project Navigator creates an ECS symbol, adds the XCO file to the project, and adds an instantiation template for the Core in the Language Templates.

   On Windows98 the template is missing everything but the comments.

   Reference: http://support.xilinx.com/techdocs/9265.htm

9. Title: 3.1i Foundation ISE: Coregen module names longer than 11 characters causes Dr. Watson

   Description: Coregen modules created in the Foundation ISE environment, which have module names longer than 11 characters will cause a Dr. Watson error in Foundation Series ISE 3.1i.

   Reference: http://support.xilinx.com/techdocs/9292.htm

LogiCORE PCI Issues

The following issues relate to LogiCORE PCI functionality:

1. Title: 4000XLA LogiCORE PCI - Signals are not guided during PAR

   Description: Signals are not guided from the supplied guide file during PAR.

   Reference: http://support.xilinx.com/techdocs/9026.htm

2. Title: V1000 LogiCORE PCI - VERILOG Timing simulation hangs

   Description: VERILOG Timing simulation never completes when using SDF file for a V1000.

   Reference: http://support.xilinx.com/techdocs/9028.htm

3. Title: Spartan-II LogiCORE PCI - Timing simulation fails

   Description: Timing simulation fails.

   Reference: http://support.xilinx.com/techdocs/9029.htm

Boundary Scan/JTAG Issues

The following issues relate to Boundary Scan and JTAG functionality:

1. Title: 3.1i JTAGProgrammer - The splash screen may cover initial error message dialog.

   Description: When initializing JTAGProgrammer attempts to open a log file. If the user does not have write access in the working directory, an error dialog is displayed to indicate this condition and allow the user to select a different log file location. Sometimes the JTAGProgrammer splash screen covers up this dialog giving the appearance of a frozen application. Any key click on the splash screen will bring the error dialog forward.

   Reference: http://support.xilinx.com/techdocs/8994.htm

2. Title: JTAGProgrammer - Chain Initialize followed by Reset Cable followed by Chain Initialize operation when using XChecker cable may cause application to abort.

   Description: When using the XChecker cable and you have modified the composition of your boundary-scan chain, it is recommended that you restart JTAGProgrammer rather than using the Reset Cable operations to re-initialize the application.

   Reference: http://support.xilinx.com/techdocs/8995.htm

3. Title: JTAGProgrammer - Deferring two or more device definitions after chain initialization operation may cause application to abort

   Description: After performing a chain initialization operation in which at least one device does not have IDCODE support, JTAGProgrammer automatically asks for device identification information. If there are two or more such devices and in all cases the user selects to defer device definition by selecting CANCEL the application may abort.

   Reference: http://support.xilinx.com/techdocs/8996.htm

4. Title: Multilinx USB Connection will not work on Windows 98 Second Edition or Windows 2000

   Description: The Multilinx USB connection will not work on Windows 98 Second Edition or Windows 2000 platforms. A modified device driver that resolves this issue is available via support.xilinx.com. (Note that this issue is a JTAGProgrammer, HardwareDebugger and Chipscope/ILA known problem)

   Reference: http://support.xilinx.com/techdocs/8997.htm

Chapter 5

Software Service and Support

This chapter details how to contact Xilinx for Customer and Technical Support and how to find the most up-to-date information about Xilinx products. The following sections are in this chapter.

- "Technical Support"
- "Customer Service"
- "Customer Education"

Technical Support

This section provides information about how to find technical answers, and how to contact your technical support and customer service representatives.

Searching for Technical Answers

If you experience problems with your software installation or operation, Xilinx suggests you do the following:

- Search the Advanced Answers Search on support.xilinx.com

  The following URL search allows you to search the *Programable Logic Data Book*, solution records, Excell Journal, Technical Tips, and Application Notes for answers and solutions.

  `http://support.xilinx.com/support/searchtd.htm`

- Search the Online Manuals for information

  Go to the following URL and click the **Search** button in the upper left corner.

  `http://support.xilinx.com/support/sw_manuals/3.1i/index.htm`

- Open a Support Case online

  The Xilinx technical support web site provides forms for easily submitting your technical questions by e-mail. To access these forms, go to the **Services** area of `support.xilinx.com` and click the **Open New Case** link.

Technical Support Web Site Resources

Online technical support is available 24 hours a day, 7 days a week at `http://support.xilinx.com`. Use the site map to view a list of all the resources available from this site. Following are a few of the resources available from a few of the tabs on the Support Home page.

- Troubleshoot
  - Advanced Search: Save time with this powerful trouble-shooting tool. Our robust search engine indexes over 3,000 unique problem solving documents.
  - Configuration Problem Solver: Troubleshoot your configuration issues quickly and easily.
- Software
  - Service Packs: Keep your software up to date with our easy-to-use interface. Service Packs keep your software running at peak performance levels.
  - IBIS models: Find FPGA and CPLD IBIS file information all in one place.
- Library
  - Technical Tips: Learn tips and techniques from the masters of programmable logic design.
  - Software Manuals: Read software user and reference manuals in your Web browser. Search across the manual collection to find the information you need.
- Design
  - Application Notes: Browse our extensive library of IP and reference designs. Our application notes provide both common and high performance solutions.

  - Virtex Power Estimator: Easily predict the amount of power your Virtex device will consume before it is downloaded.
- Education
  - Courses: Sign up for one of our acclaimed design courses today.
  - Tutorials: Teach yourself Xilinx design flows with easy-to-use tutorial modules.
- Services
  - Contacts: Get up-to-date sales and distributor contact information.
  - Feedback: Provide us with your feedback so we can improve the accessibility and content of our Web site.

Contact the Support Hotline

If you need additional support, contact the Xilinx Technical Support hotline by phone or fax. When faxing inquiries, provide your complete name, company name, and phone number, along with the software version you are using.

Location	Telephone	Electronic Mail	Facsimile (Fax)
North America	1-408-879-5199 1-800-255-7778	open a case at `http://support.xilinx.com`	1-408-879-4442
United Kingdom	44-870-7350-610	ukhelp@xilinx.com	44-870-7350-620
France	33-1-3463-0100	frhelp@xilinx.com	33-1-3463-0959
Germany	49-89-93088-130	dlhelp@xilinx.com	49-89-93088-188
Japan	local distributor	jhotline@xilinx.com	local distributor
Korea	local distributor	korea@xilinx.com	local distributor
Hong Kong	local distributor	hongkong@xilinx.com	local distributor
Taiwan	local distributor	taiwan@xilinx.com	local distributor
Corporate Switchboard	1-408-559-7778	N / A	N / A

Customer Service

This section provides information for contacting your local Xilinx Customer Service representative. Contact your local distributor for international countries not listed.

Refer to the Xilinx Web site at `http://support.xilinx.com/support/custserv.htm` for the most up-to-date customer service information. The customer service toll-free number for North America is 1-800-624-4782.

The offices for the US and Canada are open Monday through Friday from 8:00 am to 5:00 pm Pacific time.

The European offices are open Monday through Friday from 9:00 am through 5:30 pm, United Kingdom time. These offices are English-speaking only.

Country	Telephone	Facsimile (Fax)
United States and Canada	1-800-624-4782	408-559-0115
United Kingdom	01932-333550	01932-828521
Belgium	0800 73738	N / A
France	0800 918333	N / A
Germany	0130 816027	N / A
Italy	1677 90403	N / A
Netherlands	0800 0221079	N / A
Other European Locations	(44) 1932-333550	(44) 1932-828521
Japan	81 3 3297 9153	81 3 3297 9189

If you are an international customer, contact your local sales representative for customer service issues. Refer to the Xilinx web site for contact information at

`http://www.xilinx.com/company/sales/int_reps.htm`

A complete list of Xilinx worldwide sales offices is at

`http://www.xilinx.com/company/sales/offices.htm`

Customer Education

There are several ways you can learn to use the Xilinx software tools, including using the software manuals and online help, taking a customer education course, or taking an online tutorial.

- Training Classes

  Xilinx offers various specialized training modules and software update classes at many different locations.

  For more information about customer training classes and software training for Xilinx products, please use the Xilinx Support Web site at `http://support.xilinx.com`.

  You can also contact a Xilinx Training Administrator at the following toll-free number.

  `1-877-XLX-CLASS`

  International customers please contact your local sales representative or distributor for area-specific training programs.

- User Tutorials

  - All tutorials on the Web: `http://support.xilinx.com/techsup/tutorials/index.htm`
  - Printed Implementation Tools Tutorial: *Foundation Series ISE 3.1i Quick Start Guide*

- Software Manuals Online

  All manuals on the Web: `http://support.xilinx.com/support/sw_manuals/3.1i/index.htm`

- E-learning

  This is a new system that provides in-depth technical training sessions on Xilinx programmable logic products over the Web. For more information, please use the following Web site:

  `http://www.support.xilinx.com/support/training/e-learn_sched.htm`

Appendix A

Troubleshooting

This appendix describes workarounds to problems you might have when installing the Foundation Series ISE 3.3i software and documentation.

Troubleshooting Tips

The following section addresses errors that might happen on all systems.

Software Install Hangs My System

You must close all applications (including Web browsers, e-mail applications, and virus scan software) before attempting to install the Xilinx software tools. Otherwise, you may experience system difficulties while attempting to install the software.

Insufficient Space for Installation

The Setup program gives an indication if sufficient space is not available. In some cases you must increase your disk space. However, if you see negative required disk space numbers, the warnings are not valid and you should continue with the install. These warnings are cused by the install program's inability to detect and calculate available space on very large disk drives.

Data is Removed from the Installation Directory

Xilinx strongly recommends that you install this release of the software in a completely separate directory from any earlier Xilinx releases. Installing Xilinx 3.x software over an existing previous version of Xilinx software can cause problems and is not recommended.

Software Manuals Search Does Not Work

If you did not install all of the software manuals locally, you may experience this problem.

Index