New Spartan-3 FPGAs Are Cost-Optimized for Design and Production

The new Xilinx Spartan-3 FPGA family offers up to 5 million system gates with the lowest cost per gate and lowest cost per I/O compared to any other programmable logic alternative. Why use a gate array or standard cell ASIC when you can get a low-cost, high-density, and faster time-to-market solution with Spartan-3 FPGAs?

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Today's design engineers deal with a dilemma every time they start a new logic development project. They want to develop a product fast and get it to market first – but they also must meet demands to lower costs. Many times, engineers have turned to ASIC solutions to meet their cost objectives, but that often means high NRE costs and long development times. Using ASICs also often means running the risks of:

- Missing the market window
- Losing out to competition
- Design problems
- Design changes
- Skyrocketing NRE costs.

Xilinx offers you a better solution with the new class of Spartan™-3 Platform FPGAs. Built on four generations of proven Spartan success in high-volume consumer and automotive applications, this new family of Platform FPGAs delivers unprecedented density, field reprogrammable functionality, and competitive price points. You also get a platform with the density, scalability, and features to tackle tough connectivity, DSP, and embedded design problems.

With Spartan-3 FPGAs, you can develop logic for many new consumer, networking, and automotive applications, including blade servers, low-cost routers, and medical imaging. You can get those products to market fast, because you manufacture the system with the same FPGA you use to develop and prototype the design.

Driving Down FPGA Costs

Design engineers have been looking for an alternative to long ASIC development cycles and high ASIC NRE costs. To support an industry requirement that has grown to over $20 billion, Xilinx set the goal of low cost, unprecedented density range, and high capability for the Spartan-3 family of FPGAs so they could be used both for prototyping and for production of high-volume products. To meet that aggressive target, Xilinx developed this Platform FPGA architecture with a small die size, a wide logic density range, and sufficient I/Os to support the mid-range of gate array and standard cell logic designs. In addition, Xilinx included the features most needed for today's designs:

- Up to 1.8 Mb of block RAM can be used for large FIFOs and data storage.
- Abundant distributed RAM, implemented from logic cells, can be used for small FIFOs, shift registers, and constant coefficients. This combination of block RAM and distributed RAM provides a unique flexibility found only in Xilinx FPGAs.
- Digital clock managers (DCMs) and pre-engineered clock networks facilitate the design of high-speed systems.
- High-speed multipliers are embedded for DSP applications, such as adaptive filters and forward error correction.
- Programmable SelectIO™-Ultra supports 23 I/O standards and provides a low-cost bridge from one I/O standard to another.

Figure 1 - Staggered pad technology

- XCITE digitally controlled impedance technology supports increased signal integrity for both single-ended and differential I/Os.

The result is a cost-optimized FPGA fabric that is, nevertheless, flexible, scalable, and able to provide the capability to support many designs.

Process Leadership in 90 nm

Xilinx integrated a large logic density range with all of the above features – and then took another giant step to drive down cost using a new 90 nm process technology. The Spartan-3 FPGA family is the first programmable logic built with this process technology, which leads to die sizes 50% to 80% smaller than any competing solution.

Xilinx also uses 300 mm wafer technology to deliver the efficiency and capacity needed to produce high-volume Spartan-3 FPGAs. These 300 mm wafers deliver almost 2.5 times the number of die compared to the mature 200 mm wafers, but at a fraction of the cost per die. We also implemented a dual wafer fabrication strategy, using world-class foundries at both IBM and UMC to reduce production risks and increase capacity.

Our process technology leadership makes Xilinx the world's lowest-cost, lowest-risk FPGA provider. The Xilinx investment in design optimization, 90 nm manufacturing technology, and 300 mm wafer production delivers price points for Spartan-3 FPGAs at under $20 for a 1M-gate FPGA and under $100 for a 4M-gate FPGA.

Delivering More I/Os in Smaller Die

Spartan-3 FPGAs offer a remarkably small die for the number of logic gates using 90 nm process technology. Naturally, with a smaller die comes a smaller perimeter for the necessary number of I/O pads. This could be a problem for an application that demands a high I/O count. However, by using staggered pad technology (Figure 1), Xilinx is able to deliver two rows of I/Os on each edge of the die versus one row found in all other FPGAs and ASIC alternatives. You get more I/Os in a smaller die, resulting in a low cost per I/O and low cost per gate for Spartan-3 FPGAs.

Spartan-3 FPGAs: The Complete Design Platform

Spartan-3 Platform FPGAs offer a complete solution of logic, memory, and I/Os – along with features such as multipliers – to provide a rich fabric to support connectivity, DSP, and embedded design applications (Figure 2).

Spartan-3 Connectivity Solution

Many design problems revolve around getting data on and off the FPGA. The best way to ease these connectivity problems is a robust I/O solution. All Spartan-3 I/O pins

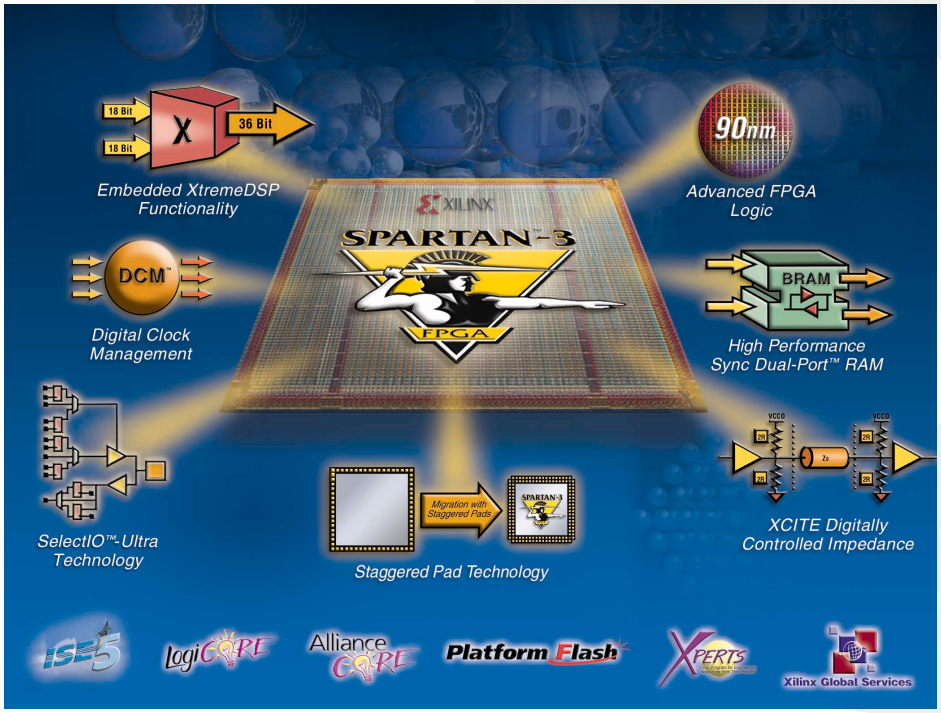

Figure 2 - Spartan-3 Platform FPGA

support the Xilinx SelectIO™-Ultra functionality, dramatically increasing design flexibility. Each user I/O pin can support any of the 23 electrical interface standards. With the abundant I/Os in the Spartan-3 FPGA family, you get the lowest cost per parallel interconnect available in the industry.

The differential I/O standards assist you in achieving higher performance, lower power consumption, and lower pin count. These standards are supported by soft IP building blocks for important new interface protocols, such as PCI 32/33 and PCI 64/33, RapidIO™, POS PHY Level 4, Flexbus 4, SPI-4, and HyperTransport™.

To further simplify the design process and reduce costs, the Spartan-3 FPGAs support XCITE digitally controlled impedance technology for both single-ended and differential I/O standards. XCITE technology provides I/O impedance matching that adapts to changes in supply voltage and temperature. XCITE technology reduces board cost by eliminating the need for most external termination resistors. What's more, XCITE technology increases signal integrity.

Low-Cost Points for High-Performance DSP

The abundant RAM resources – along with 18X18 multipliers – give Spartan-3 FPGAs a significant DSP capability that can deliver up to 330 billion MACs/second. This economical and robust performance makes Spartan-3 devices a cost-effective solution for low-cost applications, such as digital communications, video and imaging, and industrial control.

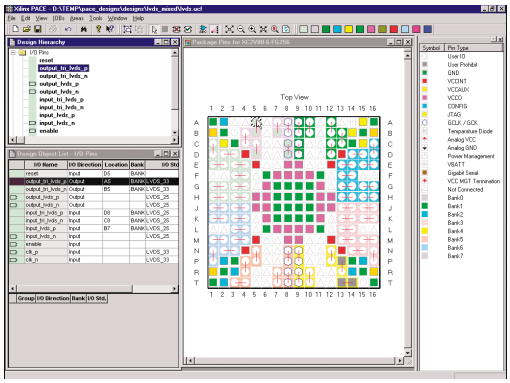

Figure 3 - ISE 5.2i design suite

In addition, the partnership between Xilinx and The MathWorks offers a simple, familiar design flow with MATLAB™/Simulink™ software to design the DSP functions.

Industry's Lowest Cost Soft Processor Solution

The high feature set of the Spartan-3 FPGA family provides a low-cost platform for embedding the Xilinx MicroBlaze™ soft processor. When you combine the MicroBlaze processor and available peripherals with Spartan-3 logic, memory, and I/Os, you can develop a custom embedded design for your specific requirements. You increase on-chip integration, reduce board cost, and minimize the risk of vendors choosing to make obsolete a specific microcontroller.

Xilinx Complete Development Support

Spartan-3 FPGAs also come fully supported in the current Xilinx ISE 5.2i software design suite (Figure 3). ISE 5.2i is the most prevalent design methodology in the industry, with more than 150,000 installed users. ISE includes a full spectrum of easy-to-use productivity options that can be inserted to fit in almost any existing corporate logic design methodology. Xilinx ISE tools increase your productivity, which in turn slash design times by as much as 50% when compared to ASIC methodologies.

For design verification, the Xilinx ChipScope™ Pro debugging environment delivers unmatched power to uncover critical bottlenecks and optimize your design.

For engineers using the MicroBlaze processor to develop a field programmable controller, Xilinx offers a complete hardware and software solution with the Xilinx Embedded Design Kit (EDK). Software tools similar to those used for IBM PowerPC™ designs are available to:

- Configure peripherals
- Develop protocols
- Integrate the logic.

Then you can verify your design in the system at speed in the Spartan-3 FPGA. It's an easy solution for today's complex designs.

Conclusion

The Xilinx Spartan-3 FPGA offers the lowest cost FPGA in the industry, as well as a true low-cost design platform for many applications. You get the density and features you need for a wide range of designs, plus a development environment to get you through the design cycle and into production quickly. To learn more about the Spartan-3 family, visit *www.xilinx.com/spartan3/*.