Spartan-3 FPGAs Add SPI-4.2 "Lite" Core to Slash Design Costs

The SPI-4.2 "Lite" solution for Spartan-3 FPGAs delivers 2.5 Gbps but remains compliant with the SPI-4.2 10 Gbps specification to deliver a low-cost, high-end solution perfect for existing MAN/LAN networks.

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Finding creative ways to keep costs low has become a mandate for designers of advanced systems. This is especially true in the telecommunications space, where the demand for ultra-fast 10 Gbps infrastructure performance is still in the formative stages. Therefore, providing 10 Gbps levels of performance is not a market or product priority at this time.

Instead, metro access and WAN/LAN equipment providers are focused on building and servicing the more mainstream 2.5 Gbps infrastructure as a way to ride out the current economic doldrums. Their priorities have shifted from features and performance to cost and risk avoidance.

Given these market conditions, designers of Ethernet, Packet-Over-SONET, and ATM applications have demonstrated a keen interest in low-cost solutions for interconnecting PHY devices and traffic management components such as network processors and ASSPs using the SPI-4.2 interconnect standard.

Xilinx is responding to this interest with a pre-engineered, drop-in SPI-4.2 "Lite" intellectual property (IP) core that can be implemented on its low-cost Spartan-3 devices. The core is fully compliant with the 10 Gbps (OC-192) OIF-SPI4-02.0 specification while operating at a reduced line rate of 2.5 Gbps (OC-48). This article provides an overview of the benefits of the solution and the details of the SPI-4.2 Lite core.

Spartan-3 FPGAs and SPI-4.2 Lite

The sweet spot for new telecommunications equipment over the next 12 to 18 months will be products running at 2.5 Gbps. Because POS-PHY Level 3 (SPI-3) is targeted to 2.5-Gbps OC-48 applica-

tions, one way to meet this demand is to build SPI-3 compliant interfaces inside these products.

However, a powerful alternative to building a SPI-3 interface is to build an interface using the SPI-4.2 Lite solution hosted on a Spartan-3 FPGA. This approach achieves 2.5 Gbps line rates while still adhering to the OIF SPI-4.2 10 Gbps specification. Furthermore, the PCB design is simplified because this solution delivers better flow control than the SPI-3 standard and uses fewer pins.

Hosting the SPI-4.2 Lite IP core on a Spartan-3 allows gigabit network providers to meet the demand for 2.5 Gbps performance at the lowest possible cost – while also putting their designers in a great position for the transition to 10 Gbps data rates. Because the core runs at a line rate of 2.5 Gbps, compared to 10 Gbps for the full-rate core, it can be successfully hosted on a low-cost Spartan-3 device that delivers the requisite performance to achieve the lower line rate.

The SPI-4.2 Lite solution is a great starting point for network equipment providers that will scale their products to 10 Gbps data rates when the market moves in that direction. Because the SPI-4.2 Lite solution running at 2.5 Gbps is functionally compliant with the OIF SPI-4.2 10 Gbps specification, the internal interface, the functional testing, and the back-end application logic can all be reused. In the line card design, as shown in Figure 2, IP reuse is straightforward. Only the size of the SPI core will change. This significantly reduces the development time associated with building equipment targeted at a 10 Gbps-dominated marketplace.

SPI-4.2 Lite Core Overview

The SPI-4.2 Lite core is delivered as independent source (Tx) and sink (Rx) cores. A block diagram of the SPI4.2 Lite IP core and its interfaces is shown in Figure 3. It is a drop-in replacement for the Xilinx full-rate SPI-4.2 IP core – the signals and functionality of both the full-rate and Lite SPI4.2 core are identical.

SPI4.2 Lite Core Specifications:

- Performance: 200 Mbps on SPI-4.2
- Supported families: Virtex™-II, Spartan-3
- Slices Required: 1,450
- SelectRAM™ blocks: 6
- Global clock buffers: 3
- Digital clock managers: 2.

The source and sink cores provide data storage implemented with FIFOs using dual-port SelectRAM blocks that support independent read/write clock domains. These FIFOs allow the storage of up to 512 data words. The design optimizations developed for the full-rate SPI-4.2 source core are also implemented in the Lite release. This includes the unique ability of the Xilinx SPI-4.2 solution to maximize bandwidth utilization by not inserting filler idle cycles on the SPI-4.2 interface. Under normal operating conditions, back-to-back packets are separated by a single combined EOP/SOP control word.

You can request the insertion of idle cycles or training patterns regardless of the source FIFO status. By allowing the insertion of idle bus cycles in response to user requests, flow control latency is greatly reduced. In addition, the SPI-4.2 Lite core is able to transfer contiguous data bursts across the SPI-4.2 interface. The source FIFO will refrain from transmitting data until an entire burst has been written into the FIFO. Once a burst has been written into the FIFO, the data will be transferred across the SPI-4.2 interface without interruption until the entire burst has been transmitted.

SPI-4.2 Lite Interfaces

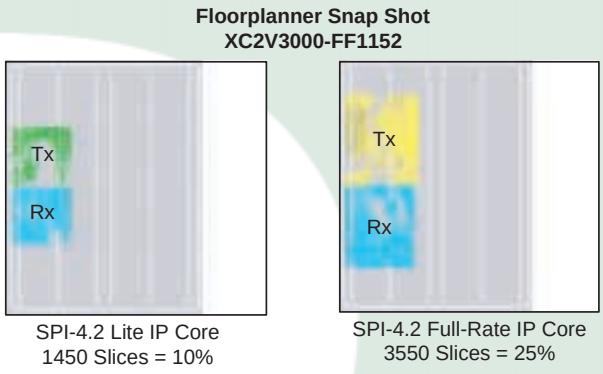

Figure 1 - Lite core requires 15% fewer slices.

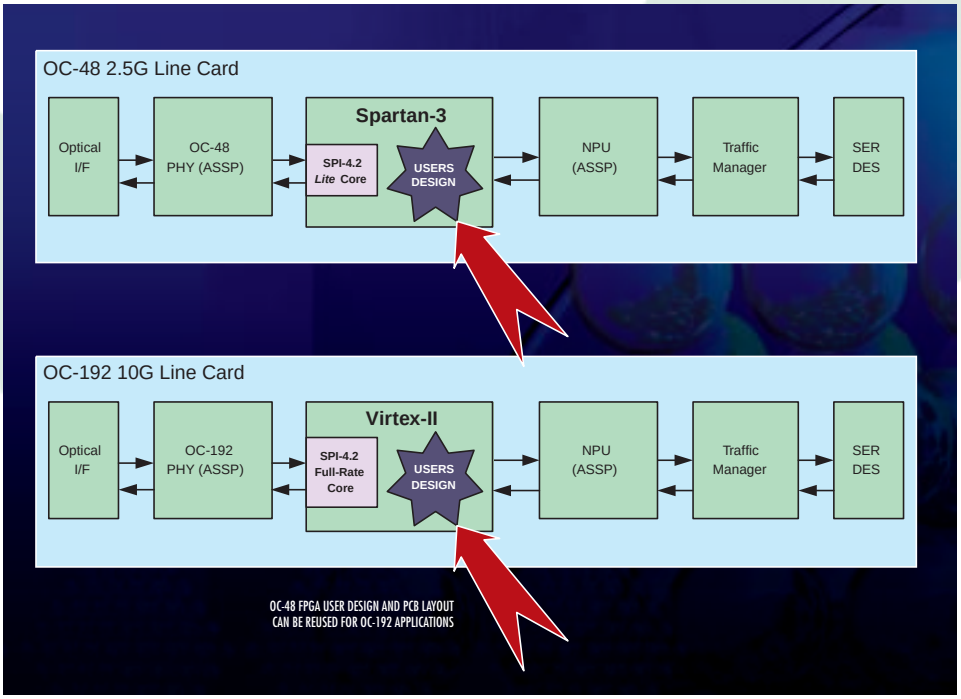

Figure 2 - SPI-4.2 Lite and full-rate design reuse example for OC-48 and OC-192 line cards

The SPI-4.2 Lite core has four primary interfaces:

1. User interface
2. SPI-4.2 interface
3. Status interface
4. Calendar interface, as shown in Figure 3.

The core also has a set of static configuration signals that are used for in-circuit customization of the core. The SPI-4.2 core's interface supports up to 200 Mbps (100 MHz LVDS DDR I/O) for an aggregate bandwidth of 2.5 Gbps. Like the full-rate SPI-4.2 IP core, the FIFO status path operates at a quarter of the data rate and its electrical interface can be user-configured to be either LVTTL or LVDS.

In order to support the widest range of applications, the SPI-4.2 Lite core offers you a choice of either a 32-bit or 64-bit user interface. The user interface operates at up to 150 MHz for both the 32-bit and 64-bit core configurations. With the 64-bit interface at frequencies greater than 100 MHz, the user interface can operate at a higher bandwidth than the SPI-4.2 interface. You can transmit and receive data from two FIFOs implemented in dual-port SelectRAM blocks that each support independent read/write clock domains.

This interface is designed with standard FIFO handshaking signals to simplify the user's logic. For additional flexibility, the source FIFO status channel interface comes in two configurations: the addressable interface and the transparent interface. The addressable calendar can be programmed to indicate the order and frequency of the channel's status on the user interface, enabling a polling implementation. The transparent calendar has a 2-bit interface for all channel configurations and is updated in the order that it is received by the sink interface, allowing minimal latency in the flow control implementation.

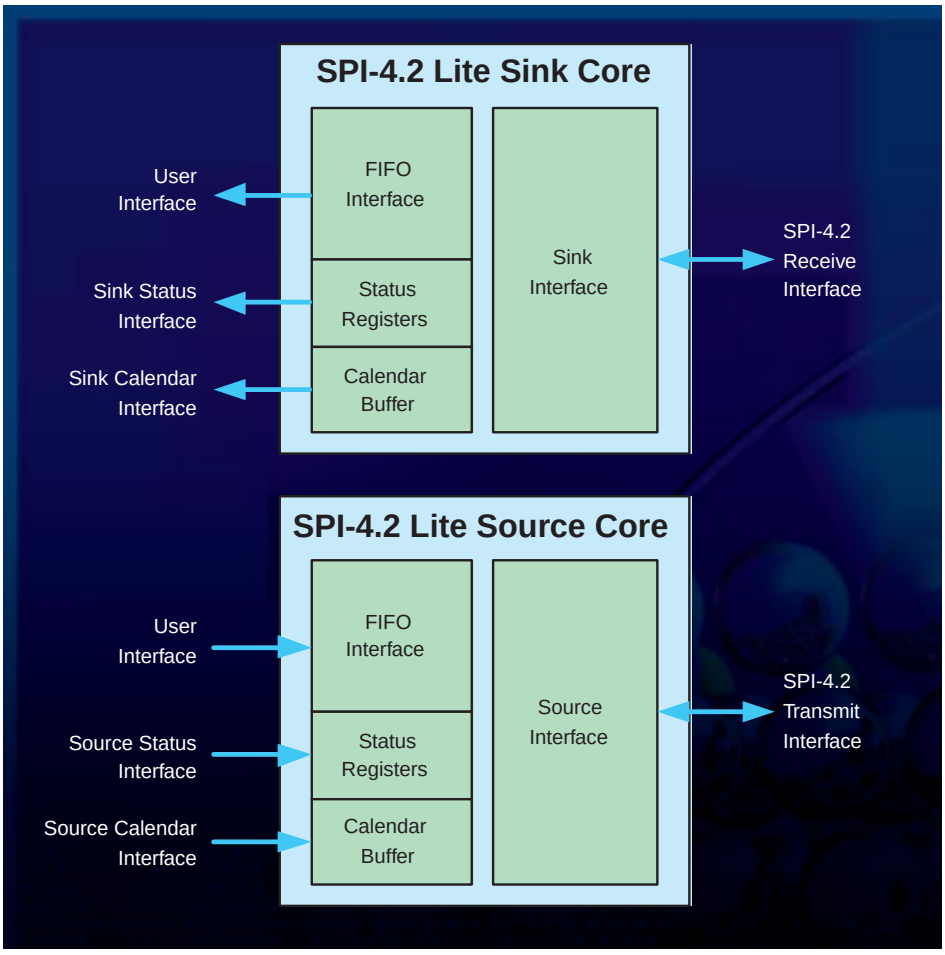

Figure 3 - Block diagram of SPI-4.2 Lite and full-rate core

Quick Start to Implementation

Two Xilinx implementation documents are provided with the core: the SPI-4.2 Design Example Guide and the SPI-4.2 Quick Start Guide. These documents help you quickly integrate the SPI-4.2 core into your design.

The SPI-4.2 Design Example Guide provides RTL code (along with a user's guide) that enables you to simulate the core immediately with automatically generated SPI-4.2 packet data. This illustrates how to connect to each of the core's interfaces. The provided code is also synthesizable so you can run it through Xilinx implementation tools. This allows you to instantly view the layout of the core in the Floorplanner, simulate the core with back-annotated timing information, and quickly evaluate performance compliance.

The SPI-4.2 Quick Start Guide contains the information necessary for you to modify the core to meet your design requirements. It walks you through the process of selecting the correct designs and netlists, customizing the timing and constraints necessary for their particular application, and running the automated implementation scripts.

Conclusion

The compact SPI-4.2 Lite core combined with the low-cost Spartan-3 architecture provides a powerful SPI-4.2 interconnect solution that helps telecommunications and networking infrastructure providers respond to the pressure to deliver low-cost solutions in today's marketplace. The SPI-4.2 Lite core is packaged with the full-rate core and is offered at $18,000 (USD). Customers with an in-maintenance license for the full-rate core are entitled to receive the new SPI-4.2 Lite core as an update.

For more information, or to evaluate the new SPI-4.2 Lite core, please contact your Xilinx sales representative.

References

[1] PMC-Sierra, Inc., POS-PHY™ Level-4, A Saturn Packet and Cell Interface Specification for OC-192 SONET/SDH and 10Gb/s Ethernet Applications. Issue 5: June 2000.

[2] OIF-SPI4-02.0 System Packet Interface Level-4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer Devices.