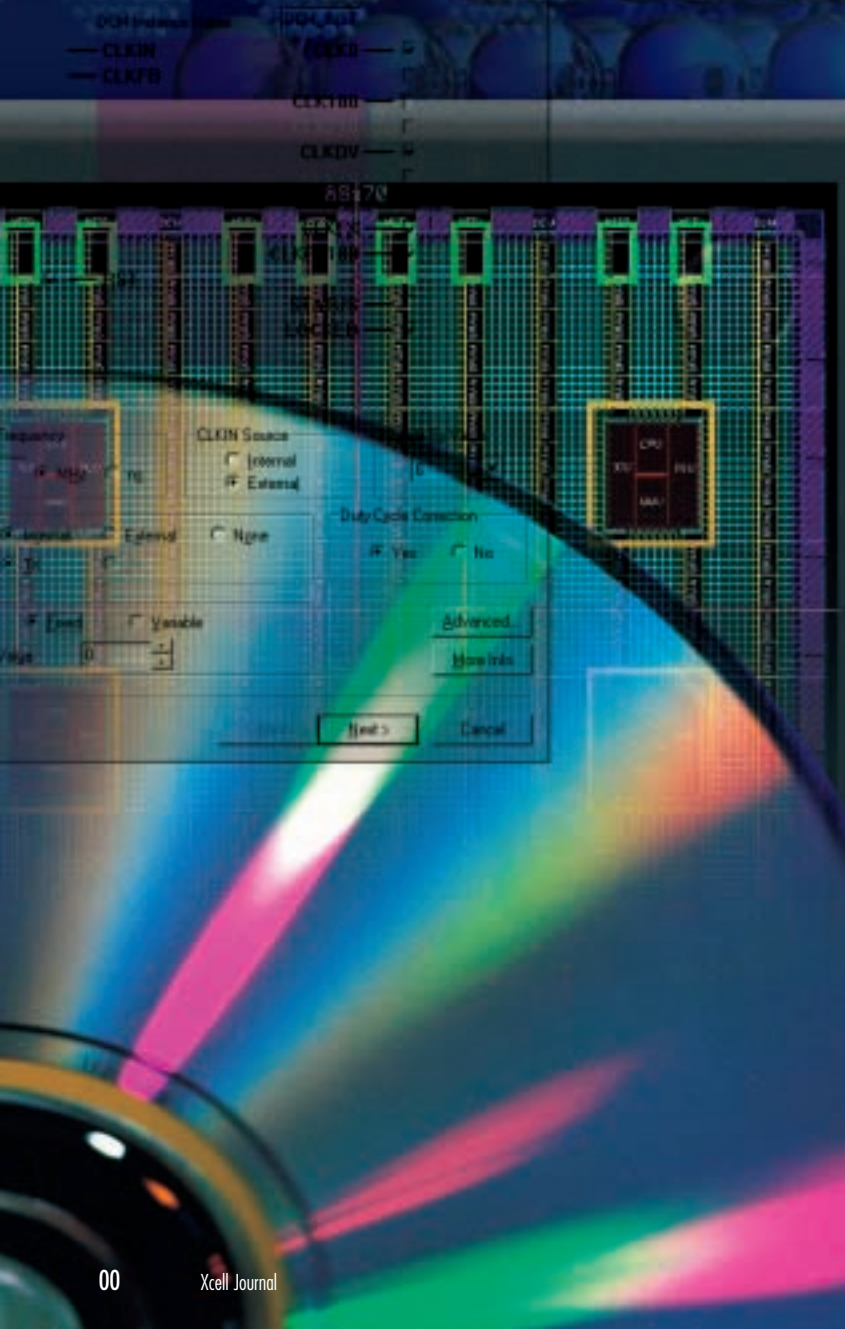
ISE 5.2i Delivers Head Start to Spartan-3 Designers

Xilinx ISE 5.2i design and development software allows you to take full advantage of the features of the newly released Xilinx Spartan-3 family of FPGAs.



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Why wait for critical, third-party software design support of the new, low-cost Spartan™-3 FPGAs when Xilinx ISE 5.2i design software is ready to go right now? You can hit the ground running with the newest and best-in-class FPGAs and development tools.

Spartan-3 FPGAs are based on the pioneering Virtex™-II Platform FPGA architecture introduced in late 2000. Virtex-II FPGAs exploded beyond the supposed limits of what a programmable logic device could do. Since then, the Xilinx ISE design environment has kept pace with the technology to make full use of the Platform FPGA architecture, including tight partner tool integration.

Leverage the Architectural Advantage

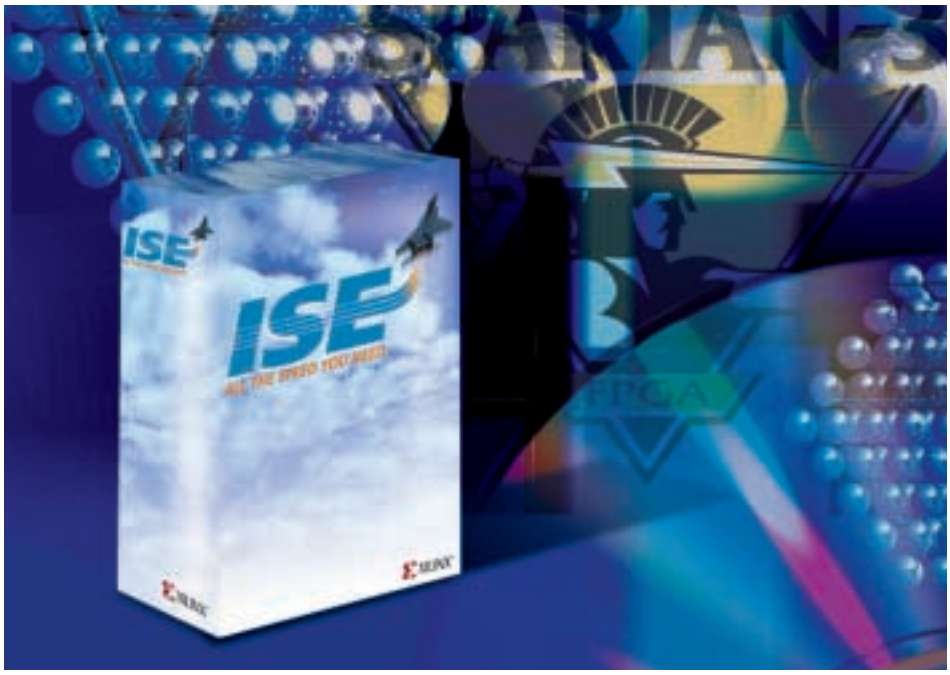
Spartan-3 FPGAs are ready to use with Synplicity™ and Mentor Graphics Exemplar synthesis support now. That means all of the internal logic structures can be put to maximum use in your Spartan-3 design today – not six months to a year from now, which is the usual timeline when a new architecture is released.

The ISE 5.2i toolset supports inferencing of internal logic structures. This allows the synthesis tools to make maximum performance choices for your design during implementation, and makes it easier to code, debug, and read HDL source code.

Spartan-3 devices also contain the "active interconnect" routing pioneered in Virtex-II FPGAs. The active interconnect technology with its buffered routing allows more logic structures to be reached with minimum impact on signal delay time. Because timing delay is minimized, even for long signal routes, you also see less impact to timing during the re-place and route phase. With active interconnect technology, more signal paths stay in time spec than with traditional architectures.

ISE 5.2i offers architecture wizard support for the Spartan-3 DCMs (digital clock managers), as shown in Figure 1. The architecture wizard lets you program the advanced clock features of the Spartan-3 DCMs through an easy-to-use design wizard. Just set the appropriate

Figure 1 - ISE 5.2i DCM architecture wizard



attributes in the dialog box, and fully editable VHDL or Verilog™ code is written into your HDL source, saving valuable design time. This HDL source is "correct by construction" without requiring you to understand every nuance of the device architecture.

The full range of I/O options for Spartan-3 FPGAs are completely supported in ISE, including differential routing, which gives you the maximum in system I/O protocol choices. Xilinx XCITE digital internal resistor I/O termination is fully supported in ISE, greatly reducing the number of external resistors on your board and freeing up valuable PCB real estate for essential devices.

Productivity Options

A full spectrum of ISE design productivity options is available to optimize your Spartan-3 design. Incremental design technology slashes design recompile times by limiting the re-implementation to only the design modules that need to change. The rest of the design is frozen and intact, preserving previous performance results.

Now included at no extra cost in ISE 5.2i is a modular design capability delivering a divide-and-conquer, team-based approach to high-density design. Teams of engineers can complete their modules in parallel, focusing on individual module performance rather than overall design completion. Modular design functionality speeds the design flow through to faster completion.

Although incremental design and modular design have similar capabilities, the incremental design approach provides a simple design flow and faster runtimes when all modules are available. On the other hand, the modular design option provides individual independence inside a team environment and can be used when you need the flexibility for design modules to arrive at different times.

The area mapping capabilities of ISE Floorplanner and PACE enable quick and easy logic grouping, leading to better timing results and faster design performance. RPM (relationally placed macros) allow design teams to save floorplanned HDL designs for later design reuse. RPMs let managers best utilize their HDL resources and deliver repeatable, guaranteed design performance.

Conclusion

With ISE 5.2i and Spartan-3 FPGAs, you now have at your fingertips the lowest cost FPGA design options available today. ISE 5.2i extends these advantages by adding the design edge that delivers more productivity and lower design costs, all in a package that's built on proven Xilinx architectural design advantages.