

Staying ahead of the competition is getting tougher everyday. Cost pressures, changing standards, and device obsolescence are just a few of the challenges. To stay ahead, you need a low cost, competitive processing solution that's customizable throughout the entire design cycle and can quickly be brought into high volume production.

The Xilinx Field Programmable Controller solution (FPC) allows you to create low-cost, customized processors with peripherals, memory, and logic – all on a single cost– optimized programmable logic device that can easily adapt to changing requirements (even after your product is in the field). We provide everything you need including development tools and a wide range of IP, so you get to market sooner with a better product that will stay in the market longer. There is no faster, easier, or cheaper way to develop microprocessor based products.

# **Processing Solutions for Cost-Sensitive Applications**



### Low Cost, High Performance, Easy to Use

The Xilinx FPC solution includes both the low cost Spartan<sup>™</sup>-IIE and Spartan<sup>™</sup>-3 FPGA families, coupled with our compact, high-performance MicroBlaze<sup>™</sup> 32-bit RISC processor core. You also get a wide assortment of peripherals and intellectual property, with full software support including compiler, assembler, and debugger, along with implementation, simulation and verification tools. You get:

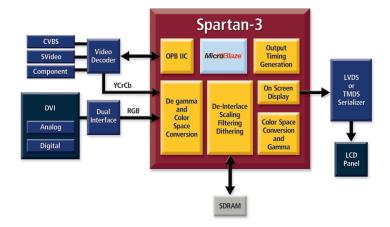
- **Flexibility** You can easily create a customized processor-based design, and you can modify your design to meet changing requirements. You can also create one PC board that meets a wide range of different applications just reconfigure the FPGA.
- No Obsolescence Xilinx allows you to purchase our MicroBlaze source code. This guarantees product availability for any application you choose. You can also port the core across Xilinx product lines or even target an ASIC.
- Lowest Cost per I/O The Spartan FPGA devices contain up to 784 user I/O, with over 90% more capacity and the lowest cost per I/O than competing FPGAs in the same density ranges. This competitive advantage allows you to integrate more features while at the same time shrink the form factor for each device. Additionally, the greater I/O coverage gives you the advantages of high I/O count Gate Arrays with the added advantage of reprogrammability.
- Reduce System Cost By integrating your design onto a single device, you not
  only save time and effort, you also reduce your overall costs. Spartan FPGAs are the
  lowest cost programmable logic devices you can get, and they also give you another key
  advantage– reduced inventory costs; one device type can meet a broad range of uses
  in different products. Spartan-IIE and Spartan-3 FPGAs also allow you to integrate costly
  board-level, features such as DLLs, RAM, and a variety of I/O translators into a single,
  compact, low cost platform.



# The Complete Xilinx FPC Solution

- MicroBlaze 32-bit RISC soft processor core
  - Efficient Harvard-style busses
  - Efficient 3-operand instruction word
  - 32-bit data path (no-multiplex)
  - 32-bit general purpose registers (32 registers)
  - 49 D-MIPs at 75 MHz in Spartan-IIE FPGA
  - 68 D-MIPs at 85 MHz in Spartan-3 FPGA
  - Uses only 1050 logic cells (15% of a XC2S300E; 27% of a XC2S150E; 6% of a XC3S1000; 24% of a XC3S200)
- · Peripherals:
  - For a complete listing of peripherals please visit www.xilinx.com/microblaze
- · Embedded Processor Software
  - GUI-based configuration and parameterized flow
  - GNU compiler, assembler, loader, and debugger
- · Advanced FPGA Development Tools
  - Download a free copy of the Xilinx ISE Foundation software from: www.xilinx.com/ise

## **Flat Panel Display**



Туре	Peripheral IP	Logic Cells*	Spartan-IIE Target Device	% Used	Spartan-3 Target Device	% Used	
<b>Processor Peripherals</b>	UART Lite, GPIO	1,638	XC2S100E	60%	XC3S200	38%	
Image Processing	Color Space Coversion	2,193	XC2S150E	56%	XC3S200	51%	
	Flat Panel Display	2,822	XC2S150E	72%	XC3S400	35%	
	2D DCT	4,911	XC2S300E	71%	XC3S400	61%	
Communication	HDLC 32 Channels	2,367	XC2S300E	34%	XC3S400	29%	
	ADPCM 128 Channels	9,686	XC2S400E	89%	XC3S1000	56%	
	Set Top Box	6,469	XC2S300E	94%	XC3S1000	37%	

<sup>\*</sup> Logic Cell total = (MicroBlaze) + (Peripheral or IP)

# Spartan-3 FPGAs-Cost-optimized FPGA Family

			CLB Resources				BLK I	RAM	CLK Resources			I/O Features					Speed					
	Spartan-3 F:	System Gates (see note 1)	CLB Array (Row x Col)	Number of Slices	Logic Cells (see note 2)	CLB Hip-Flops	Max. Distributed RAM Bits	# Block RAM	Block RAM (kbits)	Dedicated Multipliers	DLL Frequency (min/max)	# DCMs	Frequecny Synthesis	Phase Shift	Digitally Controlled Impedance	Number of Differential I/O Pairs	Maximum I/O	I/O Standards	Commercial Speed Grades (slowest to fastest)	Industrial Speed Grades (slowest to fastest)	ISP PROM Family	Configuration Memory (Bits)
SPARTAN-3	XC3S50	50K	16 x 12	768	1,728	1,536	12K	4	72K	4	25/325	2	YES	YES	YES	56	124	Single-ended LVTTL, LVCMOS3.3/2.5/1.8/ 1.5/1.2, PCI 3.3V - 32/64-bit 33MHz, SSTL2 Class I. 8. II, SSTL18 Class I, HSTL Class I, III, HSTL1.8 Class I, II & III, GTL, Differential LVDS2.5, Bus LVDS2.5, Ultra LVDS2.5, RSDS, LDT2.5	-4 -5	-4	XCF01S	0.3M
	XC3S200	200K	24 x 20	1,920	4,320	3,840	30K	12	216K	12	25/325	4	YES	YES	YES	76	173		-4 -5	-4	XCF01S	1.0M
	XC3S400	400K	32 x 28	3,584	8,064	7,168	56K	16	288K	16	25/325	4	YES	YES	YES	116	264		-4 -5	-4	XCF02S	1.7M
	XC3S1000	1000K	48 x 40	7,860	17,280	15,360	120K	24	432K	24	25/325	4	YES	YES	YES	175	391		-4 -5	-4	XCF04S	3.2M
	XC3S1500	1500K	64 x 52	13,312	29,952	26,624	208K	32	576K	32	25/325	4	YES	YES	YES	221	487		-4 -5	-4	XCF08P	5.2M
	XC3S1500	1500K	64 x 52	13,312	29,952	26,624	208K	32	576K	32	25/325	4	YES	YES	YES	221	487		-4 -5	-4	XCF08P	5.2M
	XC3S2000	2000K	80 x 64	20,480	46,080	40,960	320K	40	720K	40	25/325	4	YES	YES	YES	270	565		-4 -5	-4	XCF08P	7.7M
	XC3S4000	4000K	96 x 72	27,648	62,208	55,296	432K	96	1,728K	96	25/325	4	YES	YES	YES	312	712		-4 -5	-4	XCF16P	11.3M
	XC3S5000	5000K	104 x 80	33,280	74,480	66,560	520K	104	1,872K	104	25/325	4	YES	YES	YES	344	784		-4 -5	-4	XCF16P	13.3M

Note: System Gates include 20-30% of CLBs used as RAMs Logic cell is defined as a 4 input LUT + Flip-Flop + Carry Logic

Verify all data in this document with the device data sheet at http://www.xilinx.com/spartan3

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