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Spartan-3: Frequently Asked Questions

The following are the most frequently asked questions about the Xilinx Spartan™-3 family solution.

General

1. What is the Spartan-3 family and what criteria were used in its design?

The Spartan-3 solution is the latest platform FPGA offering from Xilinx. Based on the Virtex™-II family architecture, the Spartan-3 solution not only expands the density range and I/O over existing Spartan families to up to 5M system gates and up to 784 pins, but also includes platform capabilities in the areas of connectivity, DSP, and processing.

Other features include

- XCITE Digitally Controlled Impedance (DCI) technology for signal integrity management (new to the Spartan-3 family)
- Digital Clock Managers (DCM) enhanced for creating advanced clocking domains
- Dedicated XtremeDSP 18-bit x 18-bit multipliers for high-performance DSP applications (new to the Spartan-3 family)
- System I/O technology for support of 17 different single-ended and six differential I/O standards
- High performance Sync dual-port RAM (new to the Spartan-3 family)
- The most comprehensive offering of IP cores from Xilinx and third party AllianceCORE™ partners.

The Spartan-3 family introduces the first FPGA produced on the advanced 90nm process technology and has resulted in the industry's lowest cost FPGA touting the lowest cost per system gate and the lowest cost per I/O in the FPGA industry.

When Xilinx went to the drawing board for the Spartan-3 solution the goals were to achieve absolute low cost for customers. Then to develop a product that enables further penetration into new application segments traditionally serviced by gate array and standard cell ASIC offerings, and to win against competitive FPGA solutions.

2. What are the devices in the Spartan-3 family?

The Spartan-3 family consists of eight family members with platform features such as block RAM, clock management (DCM), and 18x18 multipliers. In total, the family contains densities from 50K to 5M system gates.

Table 1: **Spartan-3 Family**

	XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000
System Gates	50K	200K	400K	1000K	1500K	2000K	4000K	5000K
Logic Cells	1,728	4,320	8,064	17,280	29,952	46,080	62,208	74,480
Block RAM Blocks	4	12	16	24	32	40	96	104
Block RAM Bits	72K	216K	288K	432K	576K	720K	1,728K	1,872K
DCMs	2	4	4	4	4	4	4	4
IO Standards	23	23	23	23	23	23	23	23
Max Single Ended I/O	124	173	264	391	487	565	712	784
Max Differential I/O	56	76	116	175	221	270	312	344

3. Why does Xilinx call the Spartan-3 device a platform FPGA?

A platform FPGA combines a large amount of programmable logic, embedded intellectual property (IP) cores, advance clocking circuitry, and embedded memory with versatile, fast interconnect structures. Spartan-3 FPGAs provide a single platform that is easily customizable for system connectivity, DSP, and/or data processing applications necessary for sophisticated system on a chip (SoC) design in a single programmable device.

4. What markets and applications will the Spartan-3 family address?

Spartan-3 FPGAs will continue to play in the low-end in markets that the Spartan-II and Spartan-IIE families traditionally serviced such as networking/communications, video and imaging, automotive, and broadband in applications such as modems, line cards, video editing, etc. However, due to the higher volume crossover points with Spartan-3 devices, Xilinx is now better poised to compete in low-end applications in these same markets that are of higher volume which have more sensitivity to cost, like those found in the consumer and video/imaging markets.

Due to higher gate counts and I/O counts with the Spartan-3 family, the Spartan class FPGA now extends its play into the mid-range area where ASICs, ASSPs, and Virtex-II Pro™ devices traditionally compete. Some existing Virtex users who used Virtex devices only for prototyping because of higher volume requirements now have the ability to use a Spartan-3 FPGA in production. Previously, the only alternative was for designers to migrate to an ASIC for production cost reduction. Now designers have the choice to use a Spartan-3 device in applications such as low cost routers, SANs, super glades, medical imaging, DVD players, residential gateways, HDTV, and automotive

applications such as GPS navigation, telematics, infotainment and Driver Assistance Systems, etc.

5. Why are Spartan-3 devices a good alternative to ASICs?

As with all generations of Spartan products, designing with the Spartan-3 family helps ASIC designers to avoid the high initial NREs, lengthy development cycles and inherent risk of conventional ASICs. Its programmability permits design upgrades in the field with no hardware replacement necessary, which is impossible with ASICs. Spartan-3 also offers a very large selection of low cost IP solutions and features on-chip debugging capabilities through ChipScope™ Pro that are not available with conventional ASICs.

With gate densities up to 5M system gates, performance features like MicroBlaze™ soft processors, embedded DSP, four Digital Clock Managers (DCMs), 23 different I/O standards, and a robust package offering with more I/Os than any other cost optimized FPGA family, designers now have a cost competitive re-programmable alternative.

6. How does the Spartan-3 family compare to the Spartan-IIE and Virtex-II Pro families?

The Spartan-3 solution is the successor of the Spartan-IIE family but is architecturally based on the Virtex-II series products, so it has the best of all worlds – low cost, higher density, and platform features. Using 90 nm technology enabled Xilinx to dramatically increase the density range of the Spartan-3 family over the Spartan-IIE family. This enables Xilinx to offer the pricing levels known to Spartan devices for up to 5M gates, CREATING A “NEW CLASS OF FPGAs”.

Creating Spartan-3 FPGAs using a subset of Virtex-II series features gives Spartan-3 devices platform features such as block RAM, clock management (DCM), and 18x18 multipliers. However, Virtex-II and Virtex-II Pro devices will have a higher density range and more features and more performance across the board than that of the Spartan-3 device offering.

7. Why is there a density overlap between the devices in the Spartan-3 and Virtex-II Pro families?

The density overlap between Spartan-3 and Virtex-II Pro devices to address different market requirements. Virtex-II Pro devices are high-performance, high-density solutions with many features for high-end applications. Spartan-3 devices are the lowest cost per I/O and lowest cost per density devices in the market. The features and capabilities of Spartan-3 devices have been tailored for high-volume applications where the price is the most critical factor.

8. What is the density migration over multiple packages for the Spartan-3 family?

Table 1 below shows the scalability of the Spartan-3 family over a wide range of densities. Table 2 shows the details for each device. For instance, within the PQ208 package, a design can grow from the XC3S50 device to the XC3S400 device, realizing an 8x-density range, while remaining in the original package.

Table 2: **Density Migration over Device Packaging**

Device	XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000
VQ100	63	63						
TQ144	97	97	97					
PQ208	124	141	141					
FT256		173	173	173				
FG456			264	333	333			
FG676				391	487	489		
FG900						565	633	633
FG1156							712	784

Table 3: **Migration Scalability by Device**

TQ144	3 devices over 8x density range
PQ208	3 devices over 8x density range
FT256	3 devices over 5x density range
FG456	3 devices over 3x density range
FG676	3 devices over 2x density range
FG900	3 devices over 2x density range

Technology

9. On which process technology is the Spartan-3 family built?

The Spartan-3 family is based on IBM and UMC advanced 90 nm, 8-layer process technology.

10. What is the operating voltage of the Spartan-3 family?

The Spartan-3 devices have a 1.2V core with 1.2/1.5/1.8/2.5/3.3V I/O voltage interfaces.

11. What are the advantages of the advanced 90nm technology?

The Spartan-3 family is now driving technology at Xilinx, as it is the first product based on the 90nm technology. Using this advanced technology resulted in a 50% chip size reduction for Spartan-3 devices as compared to the 130nm technology. This represents a cost savings of up to 80% over

competitive offerings. Such significant price reduction is possible due to remarkable economies of scale involved with moving to next generation manufacturing processes at increasingly finer geometries to achieve greater device densities and higher yields. A dual manufacturing strategy with IBM and UMC has put Xilinx at the forefront of the semiconductor industry's race to 90 nm and 300 mm wafers.

12. How did we use the staggered I/O technology to pack so much I/O on the Spartan-3 devices?

Unique to the Spartan-3 family architecture, a user has more I/O pins to design with. This is enabled by having two rows of I/O on each edge of the chip versus one found in all other FPGAs; hence the name staggered pad technology. This gives the maximum number of I/Os per dollar. Due to this feature, we are able to offer up to 784 I/O pins in Spartan-3 devices which is 50% more than in Spartan-IIE devices.

The Figure 1 shows the migration from 130 nm to 90 nm technology. The first part of the picture shows migration without staggered pads and the second with staggered pads. The latter represents the Spartan-3 solution approach.

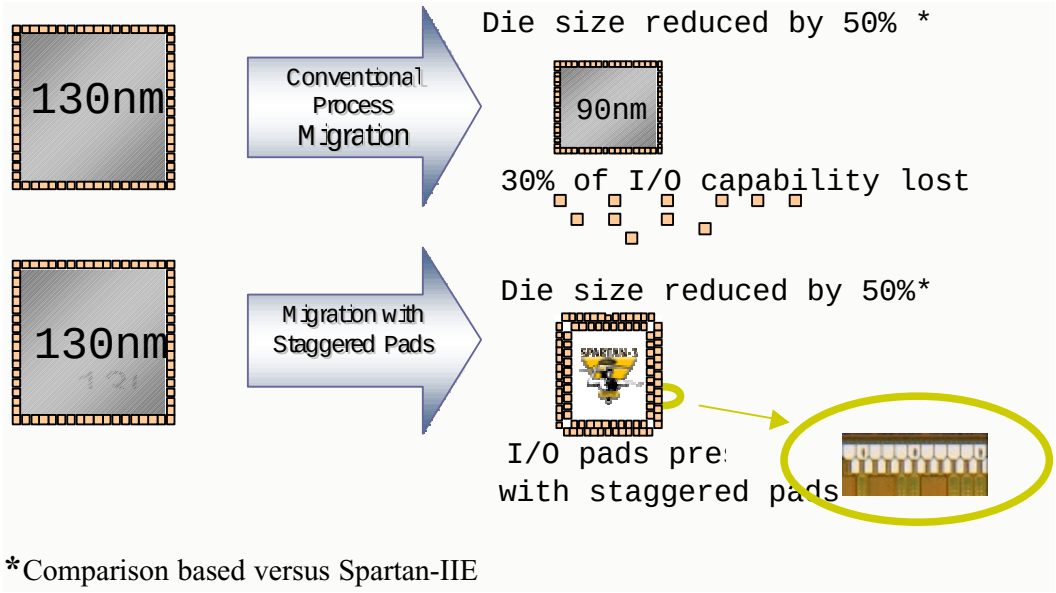

Figure 1: **130 nm to 90 nm Technology Migration**

Availability and Pricing

13. When will Spartan-3 devices be available?

Spartan-3 samples began shipping in March. First available devices are the XC3S1000 and XC3S50.

14. How much will Spartan-3 devices cost?

Volume pricing at the end of 2004 will be under $3.50 for the XC3S50 and under $20 for the XC3S1000, and under $100 for the XCS4000 (based on 250K unit quantities).

15. How does Spartan-3 family pricing compare to competitor products?

The Spartan-3 family advanced process technology is optimized for low cost. Xilinx is using 90 nm manufacturing technology to enable pricing under $20 (250K units, end-2004) for a one-million-gate FPGA (approximately 17,000 logic cells), which represents savings of up to 80 % compared to competitive solutions.

DSP

16. What makes the Spartan-3 solution good for DSP applications?

The Spartan-3 solution brings new low price points for high-performance DSP includes many features that enable designers to build highly efficient DSP systems at prices competitive to many DSP processors. Examples include:

- Up to 104 18x18 embedded multipliers. These can be used to implement compact DSP structures such as MAC engines, and Distributed Arithmetic (DA) or fully parallel FIR filters.
- SRL16 shift register logic and distributed memory for building compact DSP structures such as filters
- Block RAM for storing partial products and coefficients - A large library of DSP IP cores to allow designers to implement complex DSP algorithms such as Forward Error Correction (FEC) codecs, filters, for digital communications and imaging applications

17. What is the DSP design flow for the Spartan-3 solution?

The DSP design flow for the Spartan-3 solution remains the same as for all other DSP solutions from Xilinx. As you are aware, Xilinx offers many design flows for DSP design allowing designers to implement systems using familiar environments.

- The Xilinx System Generator for DSP bridges the gap between MathWorks' Simulink tool and the Xilinx ISE implementation tool. System Generator is the industry's only tool to support advanced capabilities such as hardware-in-the-loop and HDL co-simulation. These features make the Spartan-3 solution design flow

akin to that of DSP processors.

- The Cadence Signal Processing Worksystem (SPW) design flow is also supported.

Memory

18. What type of embedded memory features do Spartan-3 devices have?

Spartan-3 devices feature block RAM (BRAM) and distributed RAM. Every other slice on the Spartan-3 die has LUTs that can be used for distributed RAM. The total amount of distributed RAM depends on device density but the range is from 12Kbits in the XC3S50 to 520 Kbits in the XC3S5000.

Block RAM comes in 18K blocks arranged in two columns on the die. This is the same block size as the BRAM found in Virtex-II and Virtex-II Pro devices. The number of blocks goes up with density but the range is from four blocks in the XC3S50 to 104 blocks in the XC3S5000. On the XC3S5000, the total amount of BRAM is 1872K.

System Clock Management

19. How many global clocks are there per device?

Spartan-3 devices have eight global clocks that can run anywhere in the device.

20. What is the Digital Clock Manager (DCM) block found in the Spartan-3 devices and how does it work?

DCMs provide phase locking, phase shifting, and synthesizing precise frequencies. Multiple outputs from a single DCM can be used for efficient clock control while using a single resource. For deep submicron process technologies, the digital implementation of these systems provides a higher level of stability compared with analog implementations and also eliminates the need for specialized analog power supplies. This enhanced clocking not only provides greater flexibility but also eliminates external clock management chips. This lowers overall system cost and provides higher reliability.

21. How many DCMs are there in the Spartan-3 devices?

The Spartan-3 family provides up to four Digital Clock Managers (DCMs) within a single device, extending the functionality of the Delaye Locked Loops (DLLs) found in Spartan-IIE devices.

22. Can you describe the clocking support in the Spartan-3 solution?

Spartan-3 devices have eight global clock buffers, which is twice as many as offered in Spartan-IIE devices. These truly global clocks provide a cost optimized scheme for the Spartan-3 device array sizes to get you anywhere on the chip efficiently. Additional clocking is possible in the software via long lines. We have also expanded the capability of the DLL found in Spartan-IIE devices to include DCMs in the Spartan-3 solution. The Spartan-3 family contains four Digital Clock Managers (DCMs) within a single device, except the XC3S50, which contains two DCMs. The DCM operates at a minimum frequency of 25 MHz and a maximum of 325 MHz.

System Interfacing

23. What are the I/O advantages associated with Spartan-3 FPGAs?

The Spartan-3 family showcases the industry's premier I/O interface technology, to fully address all aspects of system connectivity in high-performance designs. System connectivity consists of the physical interface and the protocols required offering higher bandwidth. The Spartan-3 technology uses SelectIO™-Ultra to provide the fastest and most flexible electrical interfaces. All Spartan-3 device I/O pins support full SelectIO-Ultra functionality, to increase design flexibility.

The Spartan-3 family also supports XCITE Digitally Controlled Impedance (DCI) technology on selected I/O standards. The XCITE option is available on each user output, whereby the output impedance is matched to external reference impedance dedicated to one of eight 8 I/O banks within each device. This capability eliminates the need for most external termination resistors and allows high-precision impedance matching required for high speed. This provides a unique capability within the Spartan-3 family that is unavailable in ASICs, whereby Spartan-3 designs may be used in different electrical environments by matching local impedance requirements. In contrast, ASICs designed for one particular board impedance spec may not be able to work in a different board environment and cannot be tuned for adjustment.

Staggered Pad Technology Gives You More I/O

Unique to the Spartan-3 family architecture, a user has more I/O pins to design with. This is enabled by having two rows of I/O on each edge of the chip versus one found in all other FPGAs; hence the name staggered pad technology. This gives the maximum number of I/Os per dollar. Due to this feature, Xilinx is able to offer up to 784 I/O pins in Spartan-3 devices which is 50% more than in the Spartan-IIE family.

24. What are the single ended, differential, and DCI I/O standards supported by the Spartan-3 family?

Single Eended I/O	Differential I/O	Impedance Matching I/O
LVTTL, LVCMOS, SSTL2 I&II, SSTL18 I, HSTL18 I,II&III, GTL, GTL+, PCI33	LVDS, LVDS EXT, LDT, ULVDS, BLVDS, RSDS	DCI for LVCMOS, DCI for LVDS & LVDS-EXT, DCI for HSTL, DCI for SSTL, DCI for GTL & GTL+

25. What packages will be available for the Spartan-3 family?

The Spartan-3 family will be available in cost effective wire-bond packages for a total of eight package types with a range of 63 to 784 I/O. These include the previously available Spartan family package types of VQ100, TQ144, PQ208, FT256, and FG456. Xilinx has added three new packages to accommodate higher I/O counts: FG676, FG900, and FG1156.

	XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000
VQ100	63	63	-	-	-	-	-	-
TQ144	97	97	97	-	-	-	-	-
PQ208	124	141	141	-	-	-	-	-
FT256	-	173	173	173	-	-	-	-
FG456	-	-	264	333	333	-	-	-
FG676	-	-	-	391	487	489	-	-
FG900	-	-	-	-	-	565	633	633
FG1156	-	-	-	-	-		712	784

26. Are Spartan-3 devices pin-compatible with other devices?

Spartan-3 devices are pin-compatible inside of the Spartan-3 family.

27. Are different density device footprints compatible for the same package?

Yes, Spartan-3 devices are pin-compatible in the same package within the Spartan-3 family.

Device Configuration

28. What configuration devices support the Spartan-3 family?

Both legacy PROMs and Platform Flash PROMs from Xilinx can be used to configure Spartan-3 devices. However, Platform Flash PROMs, the latest PROM family from Xilinx, are the recommended solution for configuring Spartan-3 FPGAs. Platform Flash PROMs offer In-System Programmability (ISP), densities up to 32Mbits, and the lowest cost per megabit making it the premier choice for configuring Spartan-3 devices.

Spartan-3 FPGAs	Configuration Bits	Platform Flash PROM
XC3S50	326,784	XCF01S
XC3S200	1,047,616	XCF01S
XC3S400	1,669,136	XCF02S
XC3S1000	3,223,488	XCF04S
XC3S1500	5,214,784	XCF08P
XC3S2000	7,673,024	XCF08P
SC3S4000	10,397,824	XCF16P
XC3S5000	12,275,072	XCF16P

29. Which Xilinx download cables can be used to in-system configure Spartan-3 FPGAs?

There are multiple solutions available from Xilinx that support the Spartan-3 family including the MultiPRO Desktop Tool, Parallel Cable IV and MultiLINX™ Cable.

30. What software will support Platform Flash PROMs?

Platform Flash PROMs will require the iMPACT 5.2iSP2 or better. iMPACT is a new software tool from Xilinx that combines JTAG PROG, PC-ISP and HDWR DEBUG into one tool. The iMPACT software is available as part of the free WebPACK software.

Designers that do not currently have WebPACK can download it free from the xilinx.com web site at:
http://www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=ISE+WebPack.

Designers that already have WebPACK and iMPACT 5.2i can simply download the WebPACK Service Pack 2 or higher from the web at
http://www.support.xilinx.com/.

31. What is the pricing for Platform FLASH PROMs?

Platform Flash pricing is significantly less expensive than existing PROM families across the board. In terms of existing PROM families, Platform Flash is 40%+ lower than the XC17S00A Spartan OTP PROM family and 75%+ lower than the XC18V00 ISP PROM family.

Embedded Processing

32. What makes the Spartan-3 solution good for low cost processing solutions?

By utilizing the MicroBlaze 32-bit soft processor together with a Spartan-3 FPGA, the effective cost of the MicroBlaze core is under $1.50 per processor. Designers now have the ability to integrate the entire processing engine, control functions and additional supporting logic within a single cost-effective platform. Furthermore, Xilinx is able to leverage the same Embedded Design Kit (EDK) design tool suite that is available for the advanced Virtex-II Pro FPGA with PowerPC™ based designs.

33. What is the performance of the MicroBlaze 32-bit soft processor core within a Spartan-3 device?

- 1050 logic cells
- 68 D-MIPs at 85 MHz

34. What embedded system tool support is available for the Spartan-3 solution?

The Embedded Development Kit (EDK) includes the following Embedded System Tools (EST) support for Spartan-3 FPGAs:

- Xilinx Platform Studio (XPS)
- An IDE for hardware and software development
- Graphical assembly of MicroBlaze hardware systems
- Tools for editing software; creating hardware and software platforms
- GNU Software Development Tools
- C/C++ compilers for MicroBlaze
- Debuggers for MicroBlaze
- Other GNU utilities
- Software Libraries
- Xilinx Libc – optimized versions for MicroBlaze
- Hardware/Software Development Tools
- XMD – Xilinx Microprocessor Debug engine for MicroBlaze
- MicroBlaze Softcore 32-Bit RISC Microprocessor
- Runs on Spartan-IIE and Spartan-3 FPGAs
- MicroBlaze Infrastructure and Peripheral IP Cores
- CoreConnect On-Chip Peripheral Bus (OPB) infrastructure cores
- Evaluation versions of other CoreConnect cores

35. What is the CoreConnect Bus technology?

CoreConnect is the interconnect bus technology from IBM that is used for the soft and hard processor offerings from Xilinx. The CoreConnect architecture was developed to ease the integration and reuse of system and peripheral cores. It comprises of the Processor Local Bus (PLB) for high-speed data transfer, On-Chip Peripheral Bus (OPB) for general purpose, and Device Control Register (DCR) bus from system control. Peripherals that are used with MicroBlaze use the OPB interface to communicate with the soft processor core.

Software and IP Solutions

http://www.xilinx.com/ise/design_tools/index.htm

36. What software packages support Spartan-3 devices?

All ISE 5.2i configurations of Xilinx design software offer support for various Spartan-3 devices, this includes ISE WebPACK™, ISE BaseX, ISE Alliance Series™ and ISE Foundation™.

ISE 5.2i Configurations	Spartan-3 Device Support
ISE *Foundation*	XC3S50, XC3S200, XC3S400, XC3S1000, XC3S1500, XC3S2000
ISE *Alliance*	XC3S50, XC3S200, XC3S400, XC3S1000, XC3S1500, XC3S2000
ISE *BaseX*	XC3S50 and XC3S200
ISE *WebPACK*	XC3S50

Note: The CORE Generator™ System (included in all ISE configurations except ISE WebPACK) offers Spartan-3 device support.

Support for the XC3S4000 and XC3S5000 devices will be added with the ISE 6.1i release in September 2003.

37. Where do I get the latest speed files?

Spartan-3 device speed files will be updated with each service pack release following ISE 5.2i throughout the year. If the latest speed files for a Spartan-3 device are needed, please make to have the most recent service pack for ISE installed. The service packs for software are available from the ISE 5.2i Software Update Center at
http://www.xilinx.com/support/software/install_info.htm

38. What advantages does ISE deliver to Spartan-3 solutions?

ISE 5.2i lowers design costs. ISE 5.2i adds performance and ease-of-use to Spartan-3 designs that isn't possible with competing solutions.

ISE 5.2i accelerates Spartan-3 designs. ISE 5.2i is fully equipped to make the greatest use of the Spartan-3 family. Since the Spartan-3 solution is based on the world-leading Virtex-II architecture, many of the advantages already employed in Virtex-II device support are ready to be utilized to the advantage in Spartan-3 designs.

ISE 5.2i comes with a number of design productivity options. These development_options can_be plugged into existing design methodologies, and lower Spartan-3 design costs. With ProActive Timing Closure technology, ISE delivers up to 20% better performance than the nearest FPGA competitor, giving an extra “virtual speed grade” due to software performance.

39. Do ISE Development Options such as ChipScope Pro and ModelSim Xilinx Edition II (MXE-II) support the Spartan-3 family?

Yes, both ChipScope Pro and MXE-II support Spartan-3 devices.

ChipScope Pro delivers real-time debugging with shorter verification cycles and lower project costs. By inserting special low-impact IP debugging cores

directly into the HDL code or design netlist, designers can debug and verify logic, system bus, and internal processor bus activity, capturing signals at or near system operating speeds. And trace points can easily be changed without having to recompile the design.

ModelSim XE II (MXE-II) is a complete PC HDL simulation environment that enables verification of the HDL source code and functional and timing models of the designs.

40. What 3rd party software is available now and in the future?

Synplicity Synplify™ and Synplify Pro™, and Mentor Graphics LeonardoSpectrum fully support Spartan-3 devices. Model*Sim* Xilinx Edition-II (MXE-II) and all the Model*Sim* verification products support the Spartan-3 device family.

Third Party Software	Spartan-3 Device Support
Synthesis	
Synplicity	Synplify 7.2 overlay on FTP site
Mentor	LeonardoSpectrum LS2002e_16 overlay on FTP site
Synopsys	Design Compiler now, FPGA Compiler II in June, 2003
Simulation	
All Existing Third Parties	Now Available

41. What Intellectual Property (IP) cores will be available for Spartan-3 devices?

Due to the fact that the Spartan-3 family is based on the same architecture as the Virtex-II Series products, Xilinx was able to leverage over five years of IP already developed and in use for other Xilinx products. Various IP cores from Xilinx and AllianceCORE partners provide a broad selection of industry-standard solutions dedicated for use in Spartan-3 devices.

There are over 200 IP available for Spartan-3 devices including the popular cores such as**:**

- 10 Gbit Ethernet MAC
- 1 Gbit Ethernet MAC
- 10/100 Ethernet MAC
- MicroBlaze soft RISC processor
- PCI32/33 & PCI64/33
- SPI 3.1 (POSPHY Level 3)
- SPI 4.1

For the most up-to-date list visit the IP Center at http://www.xilinx.com/ipcenter

42. Do Spartan-3 devices support PCI?

Yes, at launch time, the PCI 32-bit / 33MHz and 64-bit / 33MHz implementations of the core are supported in the Spartan-3 family.

Services and Support

43. Is there any new Spartan-3 FPGA customer training available?

Yes. There is a new, FREE Recorded E-Learning (REL) module containing an overview of the new Spartan-3 architecture.

There are also three FREE Recorded E-Learning (REL) modules targeting the ASIC designer.

- Module 1: FPGA and ASIC Technology Comparison
- Module 2: ASIC versus FPGA Design Flow
- Module 3: ASIC to FPGA Coding Conversion

These modules are available FREE, 24 hours a day, 7 days a week, worldwide. Please visit http://www.support.xilinx.com/support/education-home.htm for access.

44. Are there customer education courses available for designers new to Spartan FPGAs?

Yes, and they have been updated to reflect the new Spartan-3 architecture. Book now to be sure to take advantage of the new promotional pricing offered below. Promotional pricing offered through June 2003.

Courses updated to reflect the Spartan-3 architecture

Fundamentals of FPGA Design	1 day
Designing for Performance for FPGA Users	2 days
Designing for Performance for ASIC Users	3 days
Advanced FPGA Design	2 days

Special Costs Savings "FPGA Essentials" Promotional package available now

Purchase 3 days of training and save $200 off of list price.

Fundamentals of FPGA Design	1 day	$ 500
Designing for Performance	2 days	$1000
List price		$1500
Special Promotion		$1300 (or 13 training credits)

See the ASIC Designer Curriculum path containing a recommendation of courses and sequences specifically designed for the ASIC designer.

http://www.support.xilinx.com/support/training/cur_paths/asic.htm

45. What support and services are available for designers?

- **Titanium Technical Service**
  - Dedicated onsite engineers w/S-3 and Xilinx tools expertise
- **Platinum Technical Service**
  - Premium priority hot line support

- **Design Services**
  - Designers w/expertise in ASIC conversion, logic and embedded software design
- **Support Web Site**
  - **Forum for S-3 discussion groups**
- **MySupport**
  - Provides automatic ALERTS on S-3 datasheets and other technical information
- **Answers database**

46. What application notes will be available at launch time?

For the latest, most complete listing of application notes for the Spartan-3 family visit the Web at xilinx.com/apps/sp3app.htm.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/03	1.0	Initial Xilinx release.
04/29/03	1.1	Updated Device Configuration FAQs.
06/05/03	1.2	Updated XC3S50 specs on Question 2.
07/22/03	1.3	Updated Question 2, Table 1, Logic Cells for XC3S5000 from 74,880 to 74,480.