DC Electrical Characteristics

In this section, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

All specifications are representative of worst-case supply voltage and junction temperature conditions. All specifications are subject to change without notice.

DC and AC characteristics are specified using the same numbers for both commercial and industrial grades unless otherwise noted.

Table 1: **Absolute Maximum Ratings(1, 2)**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.00	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to bidirectional I/O pins as well as unidirectional input and output pins.(3) If present, driver is put in a high-impedance state.	$V_{CCO} \leq 3.0V$(4)	–0.5	V_{CCO} + 0.5	V
		$V_{CCO} > 3.0V$	–0.3	3.75	V
T_J	Operating junction temperature	$V_{CCO} \leq 3.0V$(4)	-	125	°C
		$V_{CCO} > 3.0V$	-	105	°C
T_{SOL}(5)	Soldering temperature		-	220	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings will cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. This specification applies to all User I/O, Multi-Function, and Dedicated pins.
4. When V_{CCO} is 3.0 V or less, V_{IN} overshoot may go as high as V_{CCO} + 1.0 V for up to 11 ns provided that the current entering the I/O pin is limited to 10 mA. Also, when V_{CCO} is 3.0 V or less, V_{IN} undershoot may go as low as –1.0 V for up to 11 ns provided that the current entering the I/O pin is limited to 10 mA.
5. For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at www.xilinx.com.

Table 2: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:
1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. During power-on, when the V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} voltages are rising, none may dip at any point within their respective threshold-voltage ranges.
3. All parameters representing voltages are measured with respect to GND unless otherwise specified.

Table 3: **Power Voltage Levels Necessary for Preserving RAM Contents(1)**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:
1. RAM contents include configuration data.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. The level of the V_{CCO} supply has no effect on data retention.

Table 4: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	-	85	°C
		Industrial	–40	-	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage		1.140	-	3.450	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V

Notes:
1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 7, and that specific to the differential standards is given in Table 9.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.

Table 5: **General DC Characteristics of User I/O, Multi-Function, and Dedicated Pins**

Symbol	Description	Test Conditions		Min	Nom	Max	Units
I_L	Leakage current at User I/O, Multi-Function, and Dedicated pins	Driver is in a high-impedance state		–10	-	+10	µA
I_{RPU}	Current through pull-up resistor at User I/O, Multi-Function, and Dedicated pins	V_{IN} = 0V	V_{CCO} = 3.3V	500	1000	2000	µA
			V_{CCO} = 3.0V	400	800	1600	µA
			V_{CCO} = 2.5V	250	530	1100	µA
			V_{CCO} = 1.8V	120	270	770	µA
			V_{CCO} = 1.5V	70	180	440	µA
			V_{CCO} = 1.2V	40	100	300	µA
I_{RPD}	Current through pull-down resistor at User I/O, Multi-Function, and Dedicated pins	V_{IN} = V_{CCO} = 3.3V		250	520	1100	µA
		V_{IN} = V_{CCO} = 3.0V		250	520	1100	µA
		V_{IN} = V_{CCO} = 2.5V		250	520	1100	µA
		V_{IN} = V_{CCO} = 1.8V		250	520	1100	µA
		V_{IN} = V_{CCO} = 1.5V		240	510	1100	µA
		V_{IN} = V_{CCO} = 1.2V		230	480	1000	µA
I_{REF}	V_{REF} current per pin			–10	-	+10	µA
C_{IN}	Input capacitance			5	-	11	pF

Notes:
1. The numbers in this table are guaranteed over the conditions set forth in Table 4.

Table 6: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Commercial		Industrial		Units
			Typ	Max	Typ	Max	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	10				mA
		XC3S200					mA
		XC3S400					mA
		XC3S1000	40				mA
		XC3S1500					mA
		XC3S2000					mA
		XC3S4000					mA
		XC3S5000					mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5				mA
		XC3S200					mA
		XC3S400					mA
		XC3S1000	1.5				mA
		XC3S1500					mA
		XC3S2000					mA
		XC3S4000					mA
		XC3S5000					mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7.0				mA
		XC3S200					mA
		XC3S400					mA
		XC3S1000	25.0				mA
		XC3S1500					mA
		XC3S2000					mA
		XC3S4000					mA
		XC3S5000					mA

Notes:
1. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. For typical values, the ambient temperature (T_A) is 85 °C with V_{CCINT} = 1.2V, V_{CCO} = 2.5V, and V_{CCAUX} = 2.5V.
2. The numbers in this table are guaranteed over the conditions set forth in Table 4.

Table 7: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

Signal Standard	V_{CCO}			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
GTL	-	-	-	0.74	0.8	0.86	V_{REF} - 0.05	V_{REF} + 0.05
GTL_DCI(2)	-	1.2	-	0.74	0.8	0.86	V_{REF} - 0.05	V_{REF} + 0.05
GTLP	-	-	-	0.88	1	1.12	V_{REF} - 0.1	V_{REF} + 0.1
GTLP_DCI(2)	-	1.5	-	0.88	1	1.12	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_I, HSTL_I_DCI	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III, HSTL_III_DCI	1.4	1.5	1.6	0.68	0.9	0.9	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_I_18, HSTL_I_DCI_18	1.7	1.8	1.9	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_II_18, HSTL_II_DCI_18	1.7	1.8	1.9	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18, HSTL_III_DCI_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
LVCMOS12(3)	1.14	1.2	1.3	-	-	-	$0.20V_{CCO}$	$0.70V_{CCO}$
LVCMOS15, LVDCI_15(3)	1.4	1.5	1.6	-	-	-	$0.20V_{CCO}$	$0.70V_{CCO}$
LVCMOS18, LVDCI_18(3)	1.7	1.8	1.9	-	-	-	$0.20V_{CCO}$	$0.70V_{CCO}$
LVCMOS25(4), LVDCI_25(3)	2.3	2.5	2.7	-	-	-	0.7	1.7
LVCMOS33, LVDCI_33(3)	3.0	3.3	3.45	-	-	-	0.8	2.0
LVTTL	3.0	3.3	3.45	-	-	-	0.8	2.0
PCI33_3	3.0	3.0	3.0	-	-	-	$0.30V_{CCO}$	$0.50V_{CCO}$
SSTL18_I	1.65	1.8	1.95	0.825	0.9	0.975	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I, SSTL2_I_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.15	V_{REF} + 0.15
SSTL2_II, SSTL2_II_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.15	V_{REF} + 0.15

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} -- the supply voltage for the output drivers.
   V_{REF} -- the reference voltage for setting the input switching threshold.
   V_{IL} -- the input voltage that indicates a Low logic level
   V_{IH} -- the input voltage that indicates a High logic level
2. Because the GTL and GTLP standards employ open-drain output buffers, the V_{CCO} supply does not provide drive current. Nevertheless, the V_{CCO} level must always be at or above the termination voltage (V_{TT}) and I/O pad voltages.
3. There is approximately 100 mV of hysteresis on inputs using any LVCMOS standard.
4. In the standard case, all Dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, TMS) use the LVCMOS25 standard and are powered entirely by V_{CCAUX}. The Dual-Purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVCMOS25 standard during configuration. For information on how to program the FPGA using 3.3V signals and power, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**. The recommended V_{CCO} or V_{CCAUX} levels must be applied to the Global Clock Inputs (GCLK0 - GCLK7) according to the signal standards assigned to them—the same as for User Inputs.
5. All parameters representing voltages are measured with respect to GND unless otherwise specified.

Table 8: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL, GTL_DCI	32	-	0.4	-
GTLP, GTLP_DCI	36	-	0.6	-
HSTL_I, HSTL_I_DCI	8	–8	0.4	V_{CCO} - 0.4
HSTL_III, HSTL_III_DCI	24	–8	0.4	V_{CCO} - 0.4
HSTL_I_18, HSTL_I_DCI_18	8	–8	0.4	V_{CCO} - 0.4
HSTL_II_18, HSTL_II_DCI_18	16	–16	0.4	V_{CCO} - 0.4
HSTL_III_18, HSTL_III_DCI_18	24	–8	0.4	V_{CCO} - 0.4
LVCMOS12	6	–6	0.4	V_{CCO} - 0.4
LVCMOS15, LVDCI_15	12	–12	0.4	V_{CCO} - 0.4
LVCMOS18, LVDCI_18	16	–16	0.4	V_{CCO} - 0.4
LVCMOS25(2), LVDCI_25(3)	24	–24	0.4	V_{CCO} - 0.4
LVCMOS33, LVDCI_33	24	–24	0.4	V_{CCO} - 0.4
LVTTL	24	–24	0.4	2.4
PCI33_3	Note 5	Note 5	$0.10V_{CCO}$	$0.90V_{CCO}$
SSTL18_I	6.7	–6.7	V_{TT} - 0.475	V_{TT} + 0.475
SSTL2_I, SSTL2_I_DCI	7.5	–7.5	V_{TT} - 0.61	V_{TT} + 0.61
SSTL2_II, SSTL2_II_DCI	15	–15	V_{TT} - 0.80	V_{TT} + 0.80

Notes:

1. Descriptions of the symbols used in this table are as follows:
   I_{OL} -- the output current condition under which V_{OL} is tested
   I_{OH} -- the output current condition under which V_{OH} is tested
   V_{OL} -- the output voltage that indicates a Low logic level
   V_{OH} -- the output voltage that indicates a High logic level
   V_{IL} -- the input voltage that indicates a Low logic level
   V_{IH} -- the input voltage that indicates a High logic level
   V_{CCO} -- the supply voltage for the output drivers
   V_{REF} -- the reference voltage for setting the input switching threshold
   V_{TT} -- the termination voltage
2. In the standard case, all Dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, TMS) as well as the Dual-Purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) exhibit LVCMOS25 output characteristics. For information on how to program the FPGA using 3.3V signals and power, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
3. All parameters representing voltages are measured with respect to GND unless otherwise specified.
4. The numbers in this table are guaranteed over the conditions set forth in Table 4 and Table 7.
5. Tested according to relevant PCI specifications.

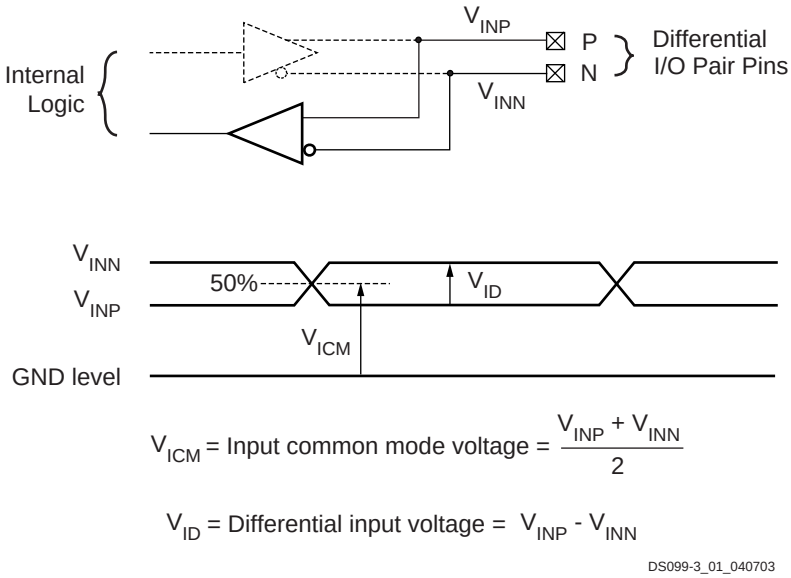


Figure 1: **Differential Input Voltages**

Table 9: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

	V_{CCO}			V_{ID}			V_{ICM}		
Signal Standard	**Min (V)**	**Nom (V)**	**Max (V)**	**Min (mV)**	**Nom (mV)**	**Max (mV)**	**Min (V)**	**Nom (V)**	**Max (V)**
LDT_25	2.38	2.50	2.63	200	600	1000	0.44	0.60	0.78
LVDS_25, LVDS_25_DCI	2.38	2.50	2.63	100	350	600	0.30	1.25	2.20
BLVDS_25	2.38	2.50	2.63	-	350	-	-	1.25	-
LVDSEXT_25, LVDSEXT_25_DCI	2.38	2.50	2.63	100	540	1000	0.30	1.20	2.20
ULVDS_25	2.38	2.50	2.63	200	600	1000	0.44	0.60	0.78
RSDS_25	2.38	2.50	2.63	100	200	-	-	1.30	-

Notes:
1. The V_{REF} input is not used for any of the differential I/O standards.
2. Of the parameters shown, only V_{CCO} represents a voltage measured with respect to GND. The remaining parameters are differential measurements. See Figure 1 for parameter definitions.

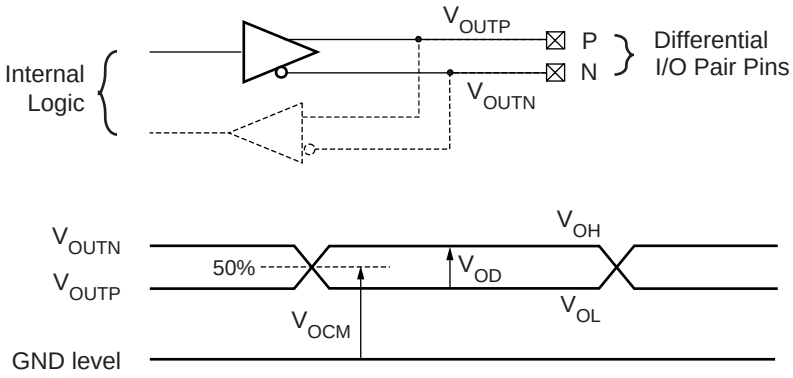


Figure 2: **Differential Output Voltages**

Table 10: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}		V_{OL}	
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Typ (V)	Max (V)	Min (V)	Typ (V)
LDT_25	430	600	670	–15	15	0.495	0.600	0.715	-15	15	-	-	-	-
LVDS_25, LVDS_25_DCI	250	325	400	-	-	1.125	1.20	1.375	-	-	-	1.475	0.925	-
BLVDS_25	250	350	450	-	-	-	1.20	-	-	-	-	-	-	-
LVDSEXT_25, LVDSEXT_25_DCI	330	540	700	-	-	1.125	1.20	1.375	-	-	-	1.700	0.705	-
ULVDS_25	430	600	670	-	-	0.495	0.600	0.715	-	-	-	-	-	-
RSDS_25	100	325	400	-	-	1.1	1.2	1.5	-	-	-	-	-	-

Notes:
1. Of the parameters shown, only V_{OH}, V_{OL}, and V_{OCM} represent voltages measured with respect to GND. The remaining parameters are differential measurements. See Figure 2 for parameter definitions.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
3. The numbers in this table are guaranteed over the conditions set forth in Table 4 and Table 9.

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

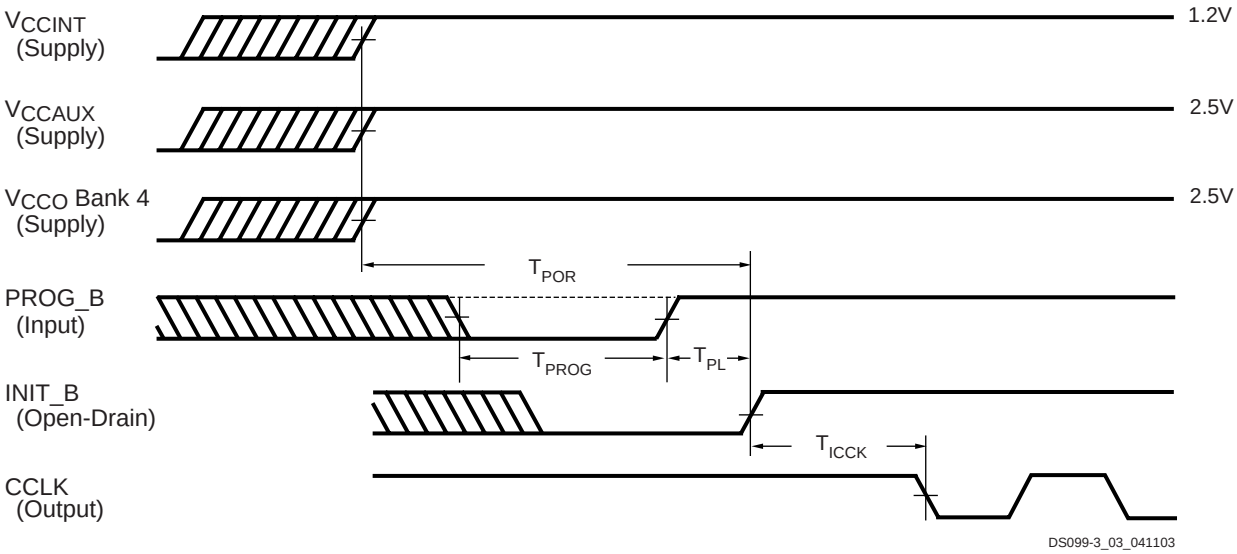
All specifications are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, values apply to all Spartan-3 devices.

Internal timing parameters are derived from measuring internal test patterns. Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. For more complete, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotate to the simulation net list.

Table 11: **DLL Timing**

Symbol	Description	Frequency Mode	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock Outputs							
F_{1XCO}	Frequency at the CLK0 and CLK180 pins	High			48	326	MHz
		Low			25	180	MHz
Clock Inputs							
F_{CLKIN}	Frequency at the CLKIN pin	High			48	326	MHz
		Low			25	180	MHz
T_{CLKINJ}	Allowable cycle-to-cycle jitter at the CLKIN pin	High			–100	+100	ps
		Low					ps

Notes:
1. For up-to-date information on DCM timing, see **http://www.xilinx.com/bvdocs/publications/ds099-3.pdf**.



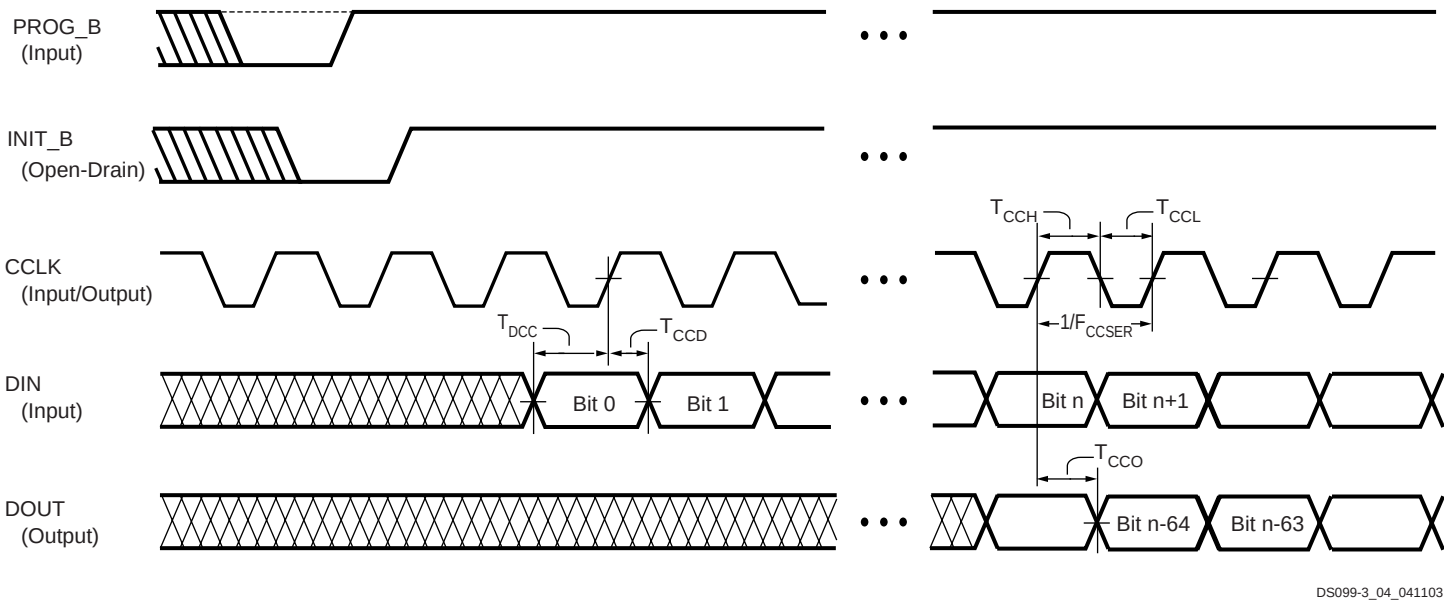
Notes:
1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 3: **Waveforms for Power-On and the Beginning of Configuration**

Table 12: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltages (whichever occurs last) to the rising transition of the INIT_B pin(1)	XC3S50	-	5	ms
		XC3S200	-	5	ms
		XC3S400	-	5	ms
		XC3S1000	-	5	ms
		XC3S1500	-	7	ms
		XC3S2000	-	7	ms
		XC3S4000	-	7	ms
		XC3S5000	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	-	µs
T_{PL}	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin(1)	XC3S50	-	2	ms
		XC3S200	-	2	ms
		XC3S400	-	2	ms
		XC3S1000	-	2	ms
		XC3S1500	-	3	ms
		XC3S2000	-	3	ms
		XC3S4000	-	3	ms
		XC3S5000	-	3	ms
T_{ICCK}	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin(2)	All	0.5	4.0	µs

Notes:
1. Power-on reset and the clearing of configuration memory occurs during this period.
2. This specification applies only for the Master Serial and Master Parallel modes.

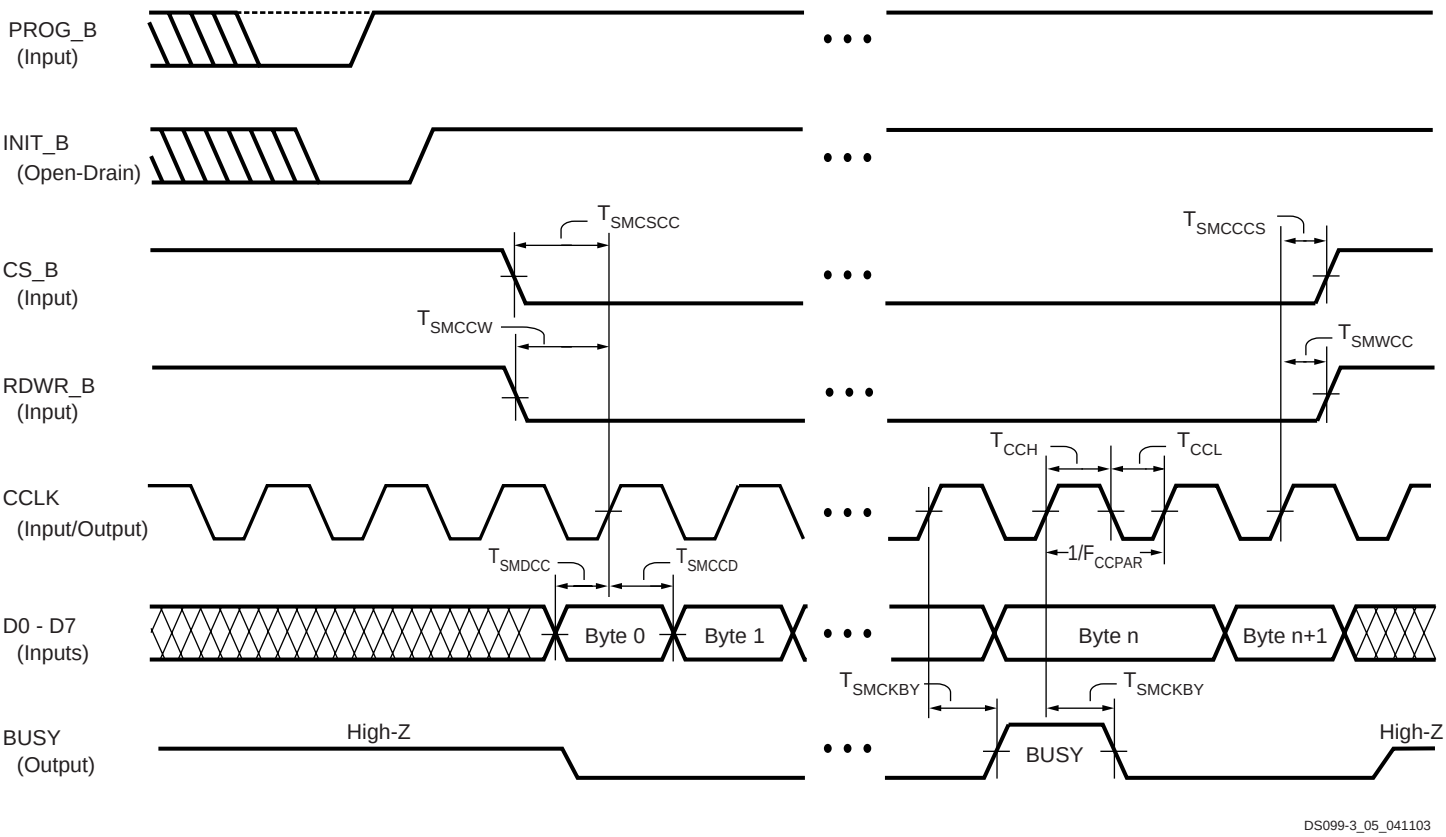


Notes:
1. The CS_B, WRITE_B, and BUSY signals are not used in the serial modes. Keep the CS_B and WRITE_B inputs inactive (i.e., both pins High).

Figure 4: **Waveforms for Master and Slave Serial Configuration**

Table 13: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description	Slave/Master	All Speed Grades		Units
			Min	Max	
Setup Times					
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin	Both	-	5.0	ns
Hold Times					
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin	Both	-	0	ns
Clock-to-Output Times					
T_{CCO}	The time from the rising transition on the CCLK pin to data appearing at the DOUT pin	Both	-	12.0	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin	Slave	5.0	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5.0	-	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin		-	66	MHz
ΔF_{CCSER}	Variation from the generated CCLK frequency set using the ConfigRate BitGen option	Master	–50%	+50%	-



Notes:
1. In a given CCLK cycle, when RDWR_B transitions High or Low while holding CS_B Low, the next rising edge on the CCLK pin will abort configuration.

Figure 5: **Waveforms for Master and Slave Parallel Configuration**

Table 14: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/Master	All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	5.0	-	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		7.0	-	ns
T_{SMCCW}	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin(1)		7.0	-	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins	Both	0	-	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin		0	-	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin(1) to the point when a logic level is last held at the RDWR_B pin(1)		0	-	ns

Table 14: **Timing for the Master and Slave Parallel Configuration Modes *(Continued)***

Symbol	Description		Slave/Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin		Slave	-	12.0	ns
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin		Slave	5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	Not using the BUSY pin(2)		-	66	MHz
		Using the BUSY pin		-	100	MHz
ΔF_{CCPAR}	Variation from the generated CCLK frequency set using the BitGen option ConfigRate		Master	–50%	+50%	-

Notes:

1. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.

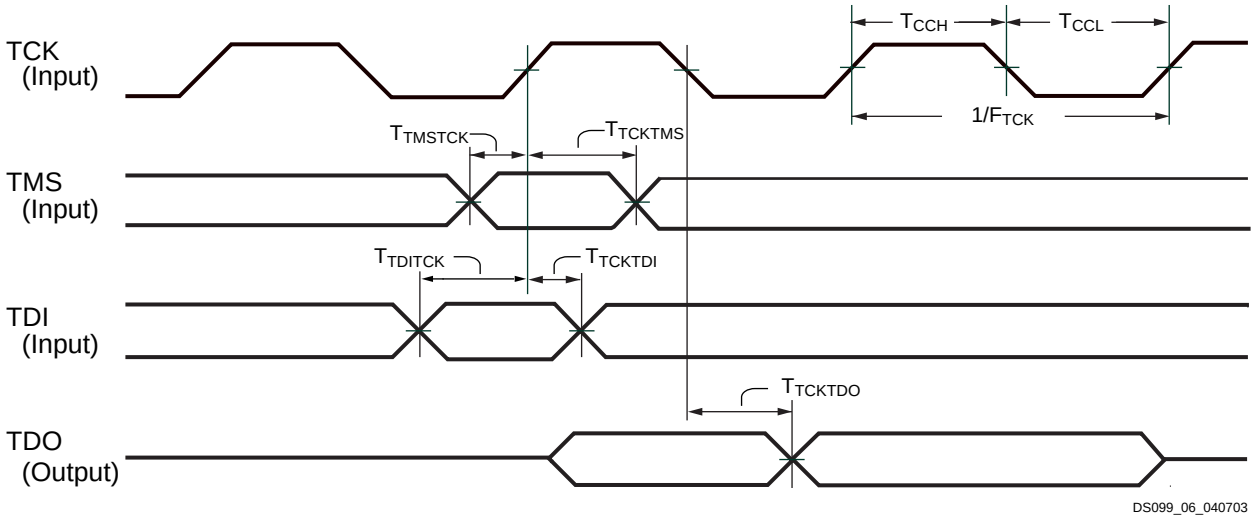


Figure 6: **JTAG Waveforms**

Table 15: **Timing for the JTAG Port**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	4.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	4.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns

Table 15: **Timing for the JTAG Port *(Continued)***

Symbol	Description	All Speed Grades		Units
		Min	Max	
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	-	11.0	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5.0	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5.0	-	ns
F_{TCK}	Frequency of the clock signal at the TCK pin	-	33	MHz

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 1. Added numbers for typical quiescent supply current (Table 6) and DLL timing (Table 11) .

The Spartan-3 Family Data Sheet

DS099-1, ***Spartan-3 1.2V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS099-2, *Spartan-3 1.2V FPGA Family: Functional Description* (Module 2)

DS099-3, *Spartan-3 1.2V FPGA Family: DC and Switching Characteristics* (Module 3)

DS099-4, ***Spartan-3 1.2V FPGA Family: Pinout Tables*** (Module 4)