Power-Assist Circuits for the Spartan-II and Spartan-IIE Families

XILINX®

XAPP451 (v1.0) November 15, 2001

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Summary

Spartan™-II and Spartan-IIE Field Programmable Gate Arrays require a minimum supply current in order to power on. For many applications, power supplies selected to cover operating current requirements can readily source enough instantaneous current to satisfy the power-on current requirement. For other applications, there may be a strict limit on the available supply current, such that the Power-On Surge (POS) current requirement is difficult to meet. In such cases, the addition of a large capacitor and a few other passive components permit Spartan-II and Spartan-IIE FPGAs to power-on with less supply current than the power-on specification requires. This application note presents a number of these "power-assist" solutions.

Introduction

Spartan-II and Spartan-IIE Field Programmable Gate Arrays require a minimum core supply current (I_{CCINT}) in order to power on successfully. This short-lived current is specified as I_{CCPO} min. in the DC Specifications section of Module 3 for both the Spartan-II and the Spartan-IIE data sheets. It is also known as the Power-On Surge (POS) current. For Spartan-II devices (both commercial and industrial), I_{CCPO} min. is 500 mA for junction temperatures above 0°C and 2A below 0°C. For Spartan-IIE devices, I_{CCPO} min. is 500 mA for commercial devices. The requirement is only in effect during FPGA power-on, before the core power voltage V_{CCINT} reaches its recommended operating level (2.5V for Spartan-II devices and 1.8V for Spartan-IIE devices). For more information on these specifications, see application note **XAPP450, "Power-On Requirements for the Spartan-II and Spartan-IIE Families"**.

When using the smaller Spartan-II and Spartan-IIE devices, it is possible that some designs will consume markedly less operating current than the minimum I_{CCPO} specification requires. For example, the Power Estimator Worksheet shows that an XC2S50 design with 64% of the logic toggling at 20 MHz and 16% of the logic toggling at 100 MHz consumes roughly 310 mA of power current. This is less than the 500 mA I_{CCPO} requirement for junction temperatures above 0°C.

When choosing a power supply to match an application's operating current needs, there is generally no issue meeting the higher I_{CCPO} requirement. This is true since many supplies can source more current to meet instantaneous demand than their continuous output rating would indicate. It is important to verify that the instantaneous capability of the desired supply will cover the I_{CCPO} min. requirement.

For some applications, a strict limit on the amount of available supply current may make meeting the I_{CCPO} min. requirement difficult. For example, the sole source for power may be a bus interface such as USB, which can only supply 250 mA. The recommended solution is to add a simple capacitor-based "power-assist" circuit that enables the FPGA to power-on with less supply current than the I_{CCPO} min. specification requires. This application note presents a number of different power-assist circuits.

The Power-Assist Circuit

The power-assist circuit is inserted between the power-supply and the FPGA. Figure 1 shows a two-port representation of the circuit. V_{SRC} and I_{SRC}, the respective supply voltage and current, enter through one port of the power assist circuit whereas V_{CCINT} and I_{CCINT} exit the

other port to power the FPGA. As a test criterion, the circuit's operation is considered successful if I_{SRC} is less than I_{CCINT}.
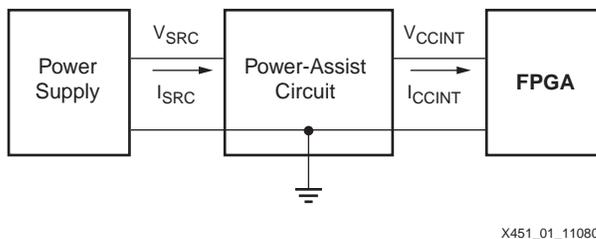

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Figure 1: **Two-Port Model of the Power-Assist Circuit**

A number of different elements, some optional, can combine to make power assist circuits that achieve different purposes. A large capacitor called C_0, connected from V_{SRC} to ground, is always part of the circuit. This capacitor is used for storing the charge necessary to produce the POS current. Some kind of switch is required to hold off power to the FPGA until the capacitor is completely charged. This switch may already be available on the board in the form of a regulator enable feature. A P-channel MOSFET can also be used to realize this function.

A limit circuit may optionally be used to control the amount of current available to the FPGA. This can serve two purposes: First, it helps keep the size of C_0 small. Second, it helps avoid inadvertently activating over current protection features (see "Using FPGAs with Over-Current Protection"). Frequently, the desired limiting effect will be the natural result of components already in the power path to the FPGA. For example, many regulators have a short circuit current characteristic that limits supply current. Alternatively, a P-channel MOSFET in saturation can be inserted into the power path to create a limit.

Power-Assist Circuit Using a Regulator

Many boards use a regulator to step the power voltage from a higher level (3.3V or 5.0V) down to the recommended operating V_{CCINT} level (2.5V for Spartan-II devices and 1.8V for Spartan-IIE devices). A power-assist circuit employing C_0 together with a regulator is explained at length in this section.

The presence of a regulator already on the board provides two important benefits: First, regulators with an enable (i.e., shutdown feature) are readily available. The enable feature can be used to delay turning on the FPGA until C_0 is completely charged. Second, the presence of a maximum short-circuit limit helps keep the size of C_0 at a reasonable value. Both these benefits reduce the cost of the power-assist circuit, since a dedicated switch is unnecessary and smaller capacitors are less expensive.

Because of the small voltage difference from input to output (commonly anywhere from 0.8V to 3.0V), the regulator will ordinarily be a Low Drop Out (LDO) type. In order to comply with the FPGA's power-on specifications, the regulator must have a short circuit current characteristic whose minimum limit exceeds I_{CCPO} min. If the short-circuit current is not specified in the regulator data sheet, use the minimum continuous output current instead. (This is a more conservative comparison. Preferably, the regulator will not have any over-current protection feature (e.g., foldback) that could turn off current to the FPGA during the POS period. See the "Regulator Selection" section in XAPP450 for more details.

A second capacitor C_{DLY} and a resistor R_{DLY} connected to the regulator's enable input are used to delay turning on the regulator.

Figure 2 shows the schematic. On the left-hand side is a power-supply that delivers a current I_{SRC} at a voltage V_{SRC}. For the following example, calculations will be made for two V_{SRC} values: 3.3V and 5.0V. Consider I_{SRC} to have the maximum possible value of 60 mA, an arbitrary value chosen so that it is well below the minimum commercial I_{CCPO} requirement (500 mA). Aside from supplying current to the regulator input, I_{SRC} also charges C_0 and the

$R_{DLY}C_{DLY}$ net. The node between R_{DLY} and C_{DLY} rises over time so that once C_0 has been charged the Enable input (EN) is High and the regulator turns on.
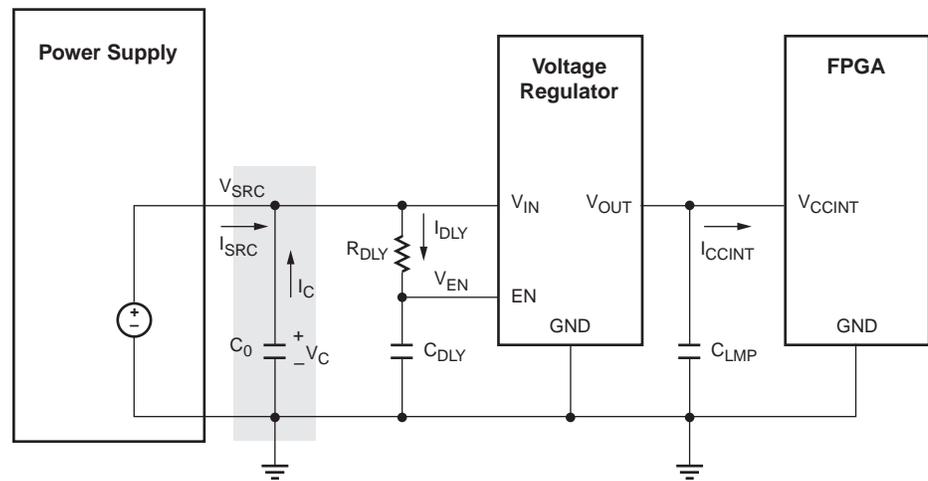

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Figure 2: **Schematic of a Regulator-Based Power-Assist Circuit**

The regulator output supplies the current labeled I_{CCINT} directly to the V_{CCINT} pins of the FPGA on the right-hand side. Also connected to the regulator output, C_{LMP}, lumps together three different kinds of capacitance: that required at the regulator output for stability, stray board capacitance and that used to decouple for the FPGA.

Figure 3 shows the waveforms one can expect from the regulator-based power-assist circuit. The nominal V_{CCINT} level is 2.5V for the Spartan-II family and 1.8V for the Spartan-IIE family. With the power-supply turned on, V_{SRC} ramps up, charging C_0 as well as C_{DLY}. As a result, the voltage on EN also rises, only at a slower rate, as determined by the $R_{DLY}C_{DLY}$ time constant. When the voltage crosses the switching threshold of EN, the regulator turns on and V_{CCINT} begins to ramp up. When V_{CCINT} reaches approximately 0.6V, the FPGA begins to draw the POS current. At this point, C_0 discharges, adding current to I_{SRC} for a peak I_{CCINT} power-on current that is equal to the maximum short-circuit current specified for the regulator. At the same time, V_{SRC} will dip by the amount ΔV_{SRC}. If the available supply current is limited to a relatively small amount, V_{CCINT} may flatten out to form a shelf.
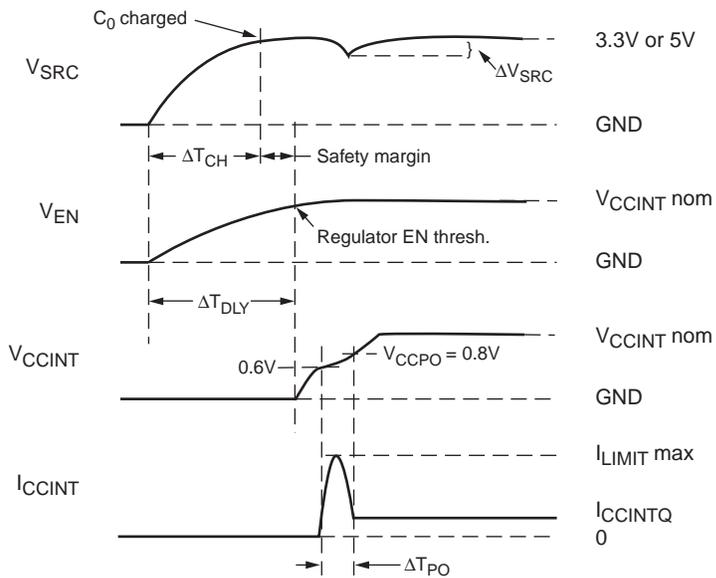
Figure 3: **Regulator-Based Power-Assist Waveform Drawings**

After the FPGA receives enough energy for power-on, V_{CCINT} will reach 0.8V, at which time the I_{CCINT} has now fallen to its standby level (I_{CCINTQ}). Finally, V_{CCINT} rises to its recommended nominal level, indicating a successful power-on.

Testing the Regulator-Based Power-Assist Circuit

A board was built to evaluate the regulator-based power-assist circuit as well as other related concepts. All tests described in this application note used this board, which consists of a few basic components: an XC2S150 FPGA, a Maxim MAX1818 2.5V 500 mA LDO regulator, and a large a capacitor (C_0), connected together as shown in Figure 2. All circuits and formulas presented in the examples that follow apply not only to Spartan-II devices, but also to Spartan-IIE devices. Furthermore, the results measured from the Spartan-II-test board are similar to what one would expect to see from a Spartan-IIE-based power assist circuit. Any pertinent differences between the power-on behavior of the two families will be pointed out.

In order to accurately measure the effectiveness of the power-assist circuit, a strict limit on the current from the power-supply to the FPGA is essential. In the present tests, an ordinary bench supply was used to provide power to the board; however, it was not possible to rely upon the supply's variable current limit feature. Such controls typically require hundreds of microseconds to take effect, by which time, the Power-On Surge (POS) period may already be over, in which case, the desired current limit would not have its intended effect. For this reason, the supply's limit feature was not used; rather, a special current limiting circuit, constructed out of two regulators, was placed between the bench supply and the power-assist circuit.

For the initial experiments described in the present section, this current-limiting circuit was arbitrarily set to 60 mA, ensuring that no more than that amount of current could ever reach the power-assist circuit. A C_0 value of 2600 µF was used for the initial measurements. All measurements were made at an ambient temperature of 25°C. Figure 4 shows a photograph of the test setup
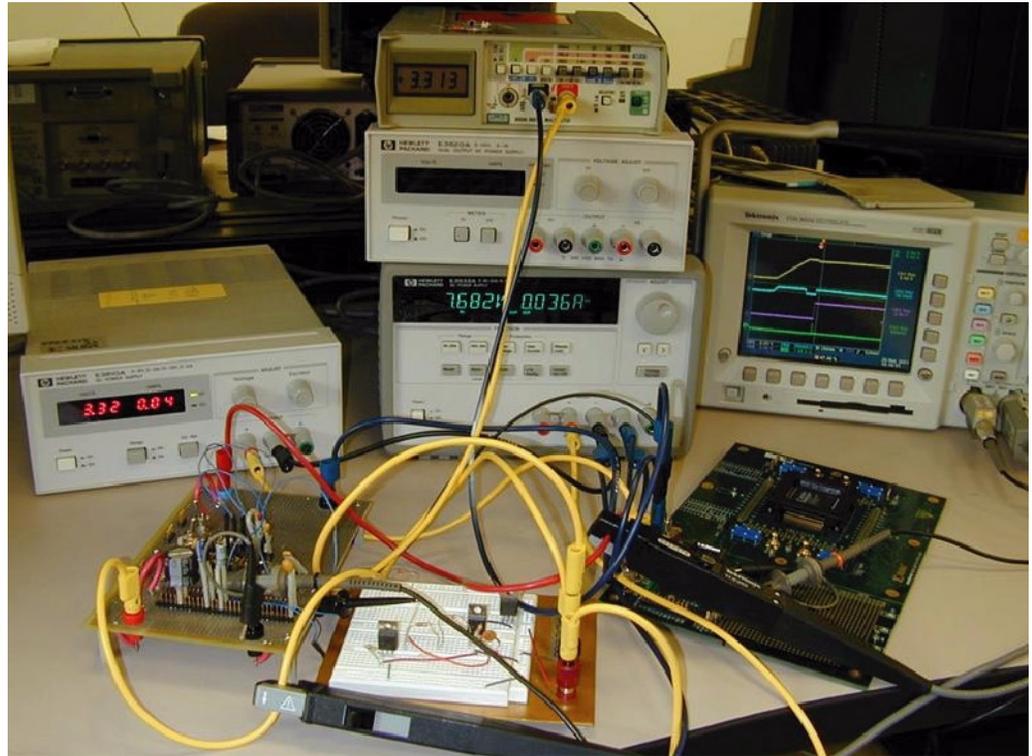
Figure 4: **Power-Assist Test Setup**

Figure 5 shows the waveforms captured from the test board. This oscilloscope picture attempts to duplicate the waveform drawings shown in Figure 3. The signals from the top down are V_{SRC}, V_{EN}, V_{CCINT}, and I_{CCINT}. The power-supply voltage V_{SRC} rises while charging C_0. V_{EN}, at the regulator enable pin, tracks V_{SRC}, only at a slower rate. Once V_{EN} is high enough (~1.6V) to turn on the regulator, V_{CCINT} begins rises and the FPGA draws a POS current. The surge on the I_{CCINT} trace is very narrow and is just obscured by the central vertical gridline
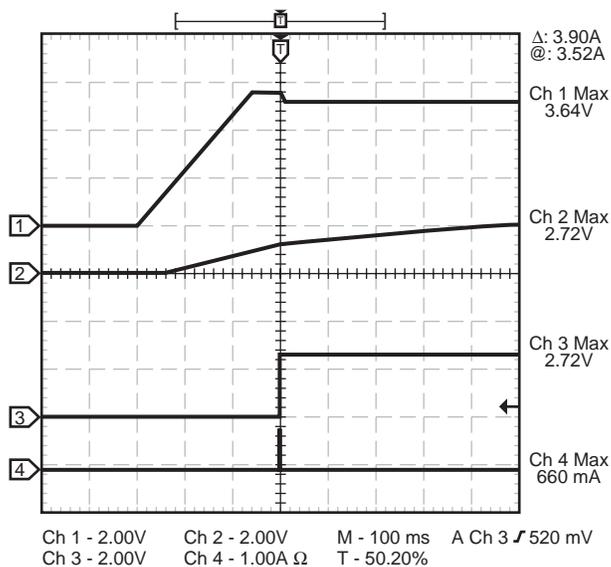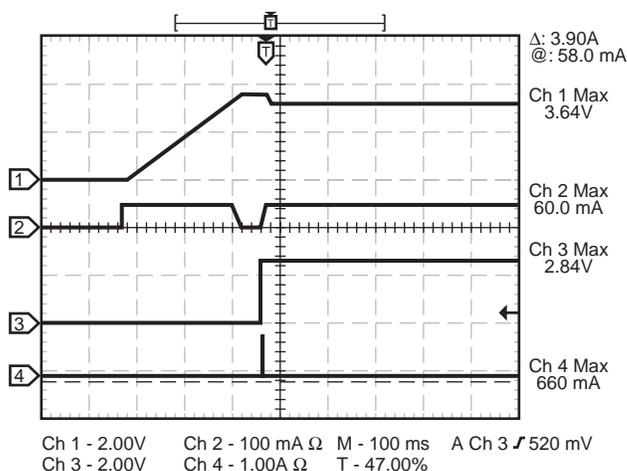
Device	T_A (°C)	Available Current (mA)	C_0 (μF)	Signals (Top Down)
XC2S150	25	60	2,600	V_{SRC}, V_{EN}. V_{CCINT}, I_{CCINT}

Figure 5: **Regulator-Based Power-Assist Oscilloscope Waveforms**

The waveforms shown in Figure 6 are identical to those of Figure 5, with the exception that I_{SRC} replaces V_{EN} (the second trace from the top). This oscilloscope picture shows the current and voltage at the input and output lines of the two-port model introduced in the **"The Power-Assist Circuit"**, page 1 section. As V_{SRC} ramps up, the power-supply provides an I_{SRC} current of 60 mA to charge C_0. This is the maximum possible current according to the operative limit.

Once V_{SRC} reaches 3.3V, C_0 is fully charged and I_{SRC} drops to 0. When the regulator turns on, the power-supply recommences providing 60 mA, this time to the FPGA.


Δ: 3.90A
@: 58.0 mA

Ch 1 Max
3.64V

Ch 2 Max
60.0 mA

Ch 3 Max
2.84V

Ch 4 Max
660 mA

Ch 1 - 2.00V   Ch 2 - 100 mA Ω   M - 100 ms   A Ch 3 ∫ 520 mV
Ch 3 - 2.00V   Ch 4 - 1.00A Ω   T - 47.00%

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Device	T_A (°C)	Available Current (mA)	C_0 (μF)	Signals (Top Down)
XC2S150	25	60	2,600	V_{SRC}, I_{SRC}. V_{CCINT}, I_{CCINT}

Figure 6: **Regulator-Based Power-Assist Two-Port Waveforms**

While only 60 mA of current were available from the power supply, the FPGA was able to draw approximately 660 mA during the POS period. The additional current drawn could only have come from C_0. The two current levels satisfy the criterion for successful operation of the power-assist circuit, that I_{SRC} be less than I_{CCINT}. Thus, the power-assist circuit works as expected. It is also worth pointing out that, V_{SRC} does not dip any more than 0.2V during the POS period, indicating that good results could have been achieved for a C_0 value much less than 2600 μF.

The next oscilloscope shot (Figure 7) shows a close-up view of the waveforms just discussed. The V_{CCINT} profile flattens out to form a "shelf" at about 0.6V. This is a result of the 60 mA

current limit. The POS current drawn by the FPGA only occurs during the shelf. The current drawn both before and after the shelf charges capacitance associated with the test fixture.
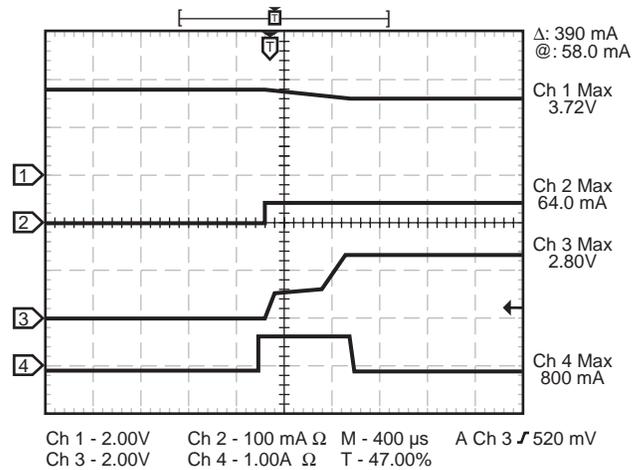
Device	T_A (°C)	Available Current (mA)	C_0 (µF)	Signals (Top Down)
XC2S150	25	60	2,600	V_{SRC}, I_{SRC}. V_{CCINT}, I_{CCINT}

Figure 7: **Regulator-Based Power-Assist Waveforms, Close-up View**

Calculating the Value for C_0

This section shows how to determine a value for C_0 such that the sum total of its discharge current plus the current available from the power supply will always be enough for successful FPGA power-on.

During the power-on period, the FPGA will take on a very low impedance value. As a result, it can draw a current as high as the regulator's maximum short-circuit current (I_{LIMIT}). There are two sources for this this: the current (I_{SRC}) from the power supply and the current (I_C) from C_0. This relationship can be expressed as follows:

$$I_{LIMIT} = I_C + I_{SRC} \qquad (1)$$

I_C is related to the change in the voltage (V_C) across C_0 that occurs during an infinitesimally small change in time, as shown below:

$$I_C = C_0(dV_C/dt) \qquad (2)$$

C_0 discharges its current during the POS period (ΔT_{PO}). Thus, ΔT_{PO} replaces dt and the equation becomes an approximation. According to Figure 2, V_C is the same as V_{SRC}. After substitutions, the new equation is:

$$I_C \approx C_0(\Delta V_{SRC}/\Delta T_{PO}) \qquad (3)$$

Next, equations 1 and 2 are combined.

$$I_{LIMIT} \approx C_0(\Delta V_{SRC}/\Delta T_{PO}) + I_{SRC} \qquad (4)$$

Solving for C_0 gives

$$C_0 \approx (I_{LIMIT} - I_{SRC})(\Delta T_{PO}/\Delta V_{SRC}) \qquad (5)$$

For the regulator-based power-assist circuit under consideration, input values for the variables are determined as follows:

   I_{LIMIT} is the maximum short circuit current specification from the regulator data sheet. I_{LIMIT} is 1.8A for the MAX1818, as shown in Table 1, which is reproduced from the MAX1818 data sheet.

I_{SRC} is the maximum power supply current, which is arbitrarily set to 60 mA for the present example.

ΔT_{PO} is the duration of the POS current. Because many regulators can supply high current to meet short-term demand means that V_{CCINT} commonly ramps up in less than two milliseconds. The present example assumes a ramp time of 2 ms. Since the POS current always lasts less than the ramp time, ΔT_{PO} is set to 2 ms, a conservative value.

ΔV_{SRC} is the most that V_{SRC} may dip when C_0 discharges. It is calculated using the following expression:

$$\Delta V_{SRC} = V_{SRC} - V_{OFFSET} - V_{CCPO} \qquad (6)$$

V_{OFFSET} is the voltage required across the switch (if any). Since a regulator is used to implement the switch in this example, V_{OFFSET} is the drop-out voltage, which is 360 mV for the MAX1818 (from Table 1).

V_{CCPO} is the V_{CCINT} level above which, I_{CCPO} goes away. This is set to 0.8V. Thus, the ΔV_{SRC} value calculated using equation 6 means that V_{SRC} can dip no further than V_{OFFSET} above V_{CCPO} for the C_0 value we derive from equation 5.

Table 1: **Selected MAX1818 LDO Regulator Specifications**

Description	Symbol	Parameters		Min	Typ	Max	Units
Guaranteed output current (RMS)	I_{OUT}	$V_{IN} \geq 2.7V$		500	-	-	mA
Short-circuit current limit	I_{LIMIT}	$V_{OUT} = 0V, V_{IN} \geq 2.7V$		**0.55**	0.8	**1.8**	A
In-regulation current limit		$V_{OUT} > 96\%$ of nominal value, $V_{IN} \geq 2.7V$		-	1.6	-	A
Dropout voltage	$V_{IN} - V_{OUT}$	$I_{OUT} = 500$ mA	$V_{OUT} = 5V$	-	100	220	mV
			$V_{OUT} = 3.3V$	-	120	215	
			$V_{OUT} = 2.5V$	-	210	**360**	
$\overline{SHDN}$ input threshold	V_{IH}	$2.5V < V_{IN} < 5.5V$		**1.6**	-	-	V
	V_{IL}	$2.5V < V_{IN} < 5.5V$		-	-	0.6	V

Below, equations 5 and 6 are evaluated for two power supply voltages, 3.3V and 5.0V, at 25°C:

When $V_{SRC} = 3.3V$ and $T_A = 25°C$,

$\Delta V_{SRC} = 3.3V - 0.8V - 0.36V = 2.14V$

$C_0 \approx (1.8A - 60 \text{ mA})(2.0 \text{ ms})/ 2.14V \approx 1626 \text{ μF}$

When $V_{SRC} = 5.0V$ and $T_A = 25°C$

$\Delta V_{SRC} = 5.0V - 0.8V - 0.36V = 3.84V$

$C_0 \approx (1.8A - 60 \text{ mA})(2.0 \text{ ms})/ 3.84V \approx 906 \text{ μF}$

When $V_{SRC} = 5.0V$, a larger ΔV_{SRC} value in the denominator of equation 5 yields a smaller value for C_0 (906 μF) than the case when $V_{SRC} = 3.3V$ (1626 μF). This makes sense, since the higher V_{SRC} level permits a greater drop in voltage across the capacitor; hence, the smaller capacitor is sufficient to discharge the required power-on current. The above calculations are valid for operation at an ambient temperature of 25°C; however, they do not account for loss of capacitance at cold temperatures. This matter will be addressed in the section **"Power-Assist Operation Over Temperature"**, page 10".

Calculating the Values for C_{DLY} and R_{DLY}

C_{DLY} and R_{DLY} are used to delay the assertion of the regulator enable input until C_0 is fully charged. The power supply, once on, charges C_{DLY} through R_{DLY}. The voltage V_{EN} across C_{DLY} increases over time, approaching the turn-on threshold of the enable input. Values must be assigned to C_{DLY} and R_{DLY} such that V_{EN} only reaches the V_{IH} max. threshold of the enable input when C_0 is completely charged. The following example assumes that V_{SRC} is 3.3V.

The first step is to calculate the charge time ΔT_{CH} for C_0. A variant of equation 2 from the preceding section is used:

$$\Delta T_{CH} \approx C_0 \Delta V_{SRC}/I_{SRC} \qquad (7)$$

Substituting values from the present example, this equation 7 yields the following result:

$$\Delta T_{CH} \approx (1626~\mu F)(3.3V)/60~mA \approx 90~ms$$

Because the actual switching threshold of EN is not specified, a safety factor, T_{SAFE}, is added to the charge time for T_{DLY}, the delay that the RC net must produce. The safety factor ensures that C_0 will be fully charged before the regulator turns on.

$$T_{DLY} = \Delta T_{CH} + T_{SAFE} \qquad (8)$$

For the sake of this example, T_{SAFE} is 10 ms, then

$$T_{DLY} = 90~ms + 10~ms = 100~ms$$

With the adjusted charge time in hand, it is now possible to determine values for C_{DLY} and R_{DLY} using an equation that describes how the voltage across a capacitor, charged by a current through a resistor, varies with time:

$$V_{EN} = V_{SRC}(1 - e^{-T_{DLY}/(R_{DLY}*C_{DLY})}) \qquad (9)$$

Solving for R_{DLY} gives

$$R_{DLY} = -(T_{DLY}/C_{DLY})(1/\ln(1 - V_{EN}/V_{SRC})) \qquad (10)$$

Choosing an arbitrary value of 4.7 μF for C_{DLY} and making the appropriate substitutions yields the following resistor value:

$$R_{DLY} = -(100~ms/4.7~\mu F)(1/\ln(1 - 1.6V/3.3V)) = 33~K\Omega$$

At T_A = 25°C, a C_{DLY} value of 4.7 μF and an R_{DLY} value of 33 KΩ means there will be a delay of 100 ms from the time the power supply turns on to the enabling of the MAX1818 regulator, ensuring that C_0 is fully charged before the POS occurs. However, these values do not take into account the loss of capacitance at cold temperature effects. This will be addressed in the next section.

Power-Assist Operation Over Temperature

Capacitance decreases with colder temperatures. Thus, it is necessary to increase the C_0 and C_{DLY} capacitor values just calculated to make up for the loss that occurs at the coldest temperatures of operation.

First, consider the adjustment to C_0. This is accomplished by multiplying the C_0 value from equation 5 by

$$1/(1 - \%C_0/100) \qquad (11)$$

where $\%C_0$ is defined as the percent decrease in C_0 when going from room temperature down to the coldest operating ambient temperature.

On account of its large size, C_0 will probably be an aluminum electrolytic capacitor. For the commercial temperature range (down to 0°C), $\%C_0$ for such capacitors is commonly around 50%. Continuing with the original example, the C_0 value when V_{SRC} = 3.3V as calculated from equation 4 is 1626 μF (T_A = 25°C assumed). The following calculation gives a C_0 value good across the commercial temperature range:

$$[1/(1 - 50/100)]*1626~\mu F = 3252~\mu F$$

An adjustment is also required to compensate for the temperature sensitivity of C_{DLY}. Because C_{DLY} is an input to previous calculations, it will be easier to keep it a constant 4.7 μF and adjust

R_{DLY} instead. Recall that the delay the two components create is a function of the RC time constant, thus adjusting R_{DLY} achieves the same basic effect as adjusting C_{DLY}.

First, since C_0 has changed to 3252 µF, it is necessary to calculate a new value for R_{DLY}. Equations 7 and 8 provide an updated T_{DLY} value of 0.189s. Using this result to evaluate equation 10 gives a value of 60.6 KΩ for R_{DLY}.

Use an adjustment factor similar to the one described for C_0, only %C_0 is now replaced with %C_{DLY}, which is defined as the percent decrease in C_{DLY} when going from room temperature to the coldest ambient operating temperature. The factor is

$$1/(1-\%C_{DLY}/100) \qquad (12)$$

C_{DLY} is assumed to be a tantalum type, which is less sensitive to temperature than the aluminum electrolytic type. The %C_{DLY} value for the commercial temperature range is assumed to be 20%. It follows that the adjusted R_{DLY} value for the commercial temperature range is

$$[1/(1 - 20/100)]*60.6 \text{ KΩ} = 76 \text{ KΩ}$$

Values for %C_0 and %C_{DLY} are readily available from capacitor data sheets.

Power-Assist Spreadsheets

Equations 5, 6, and 10 were incorporated into a spreadsheet to facilitate calculating values for C_0, C_{DLY}, and R_{DLY} under various conditions. Figure 8 shows a view of the spreadsheet that models power operation over the commercial temperature range. The input fields are shaded. They include T_{PO}, V_{CCPO}, I_{LIMIT}, V_{OFFSET}, V_{EN}, C_{DLY}, T_{SAFE}, V_{SRC}, %C_0, and %C_{DLY}, as previously introduced. These are all set to the values used in the present example.

FPGA Characteristics				Capacitance Decrease	
ΔTpo (ms)	Vccpo (V)			% Co	% Cdly
2	0.8			50	20
Supply/Regulator Characteristics					
Ilimit (mA)	Voffset (mV)	Ven (V)	Cdly (uF)	Tsafe (s)	
1800	360	1.6	4.7	0.01	
Vsrc (V)	ΔVsrc (V)	Isrc (mA)	Co (uF)	Tch (s)	Rdly (KOhms)
3.3	2.14	100	3178	0.105	46
		200	2991	0.049	24
		300	2804	0.031	16
		400	2617	0.022	13
		500	N/A	N/A	N/A
5	3.84	100	1771	0.089	68
		200	1667	0.042	36
		300	1563	0.026	25
		400	1458	0.018	19
		500	N/A	N/A	N/A

Figure 8: **Spreadsheet Calculating Commercial Component Values**

The output fields are white and include ΔV_{SRC}, I_{SRC}, C_0, T_{CH}, and R_{DLY}. When V_{SRC} is 3.3V, C_0 ranges from 2,617 µF to 3,178 µF, all are reasonable values. When V_{SRC} is 5.0V, C_0 has lower values, ranging from 1,458 µF to 1,771 µF.

Figure 9 shows a view of the spreadsheet that calculates the component values for industrial operation. For FPGA power-on down to –40°C, the min. I_{CCPO} requirement is 2A. The MAX1818 cannot provide this much current. It is necessary to choose a regulator rated for industrial operation. One that is capable of supplying 2A short-term. The Texas Instruments TPS75225Q regulator meets these requirements. The values chosen for the I_{LIMIT}, V_{OFFSET}, and V_{EN} fields reflect the TPS75225Q specifications. %C_0 is now at 67% because of the lower

minimum operating temperature. The remaining input fields have the same values as in the commercial spreadsheet.

FPGA Characteristics				Capacitance Decrease	
ΔTpo (ms)	Vcppo (V)			% Co	% Cdly
2	0.8			67	20

Supply/Regulator Characteristics					
Ilimit (mA)	Voffset (mV)	Ven (V)	Cdly (uF)	Tsafe (s)	
4500	275	2	4.7	0.01	

Vsrc (V)	ΔVsrc (V)	Isrc (mA)	Co (uF)	Tch (s)	Rdly (KOhms)
3.3	2.225	330	11359	0.114	35
		660	10460	0.052	18
		990	9561	0.032	12
		1320	8662	0.022	9
		1650	7763	0.016	7
		2000	N/A	N/A	N/A
5	3.925	330	6439	0.098	56
		660	5929	0.045	29
		990	5420	0.027	19
		1320	4910	0.019	15
		1650	4401	0.013	12
		2000	N/A	N/A	N/A

Figure 9: **Spreadsheet Calculating Industrial Component Values**

Figure 9 shows that when V_{SRC} is 3.3V, C_0 ranges from 7,763 µF to 11,359 µF. When V_{SRC} is 5.0V, C_0 has somewhat lower values, ranging from 4401 µF to 6439 µF. The industrial ranges are altogether higher than those predicted by the commercial spreadsheet. The difference is due principally to the industrial regulator having a higher maximum short-circuit current than the commercial regulator: 4.5A for the TPS75225Q compared to 1.8A for the MAX1818.

The spreadsheet is available for downloading from the **www.xilinx.com/apps/sp2eapp.htm** web page listing application notes. The spreadsheet calculates suggested power-assist component values for any FPGA that requires a minimum POS current. A V_{CCPO} value of 0.8V or higher is generally appropriate for both Spartan-II and Spartan-IIE devices. The effectiveness of the suggested component values should be verified over the operating temperature range on a prototype board that models power supply characteristics as well as loading effects. As part of this prototype test, it is also important to verify the input value used for the spreadsheet's ΔT_{PO} field. Furthermore, one should check that the V_{CCINT} ramp time when recharging the desired C_{DLY} value does not exceed the 50 ms max specification (T_{CCPO} from the data sheet). Finally, make sure R_{DLY} is not so small that the regulator enable will be de-asserted during the discharge of C_0.

Most FPGA Applications Do Not Need Power-Assist Circuits

Many power supplies can provide more current to meet the short-term I_{CCPO} requirement than their guaranteed continuous output rating would indicate. The power-on current is usually not more than a millisecond or two.

As a case in point, consider plug-in-the-wall AC-to-DC adapters which are used to power many consumer-oriented electronic products. The next experiment used such an adapter to power a Spartan-II FPGA . The setup used the same board (MAX1818-based power-assist circuit plus XC2S150) as the previous experiment; only, a Coby 3V adapter replaced the laboratory power supply and the current-limiting circuit. The adapter was rated for a 300 mA of continuous current output. C_0 was 320 µF and all measurements were made at an ambient temperature of 25°C.

Figure 10 shows an oscilloscope shot of waveforms during the POS period. The signal order from the top down is V_{SRC}, I_{SRC}, V_{CCINT}, and I_{CCINT}. Immediately upon the application of power, V_{SRC} ramps up and an I_{SRC} surge of 5A is drawn through the adaptor. This large current charges C_0. (It does not go to the FPGA since the regulator is disabled at this time. Only after V_{CCINT} begins to rise does the FPGA draw a POS current.) These waveforms show that the Coby adapter, presented with a short-term demand, can provide 17 times the continuous output current rating . In conclusion, the adapter alone can easily meet the FPGA's minimum I_{CCPO} requirement and the power-assist circuit is not necessary.
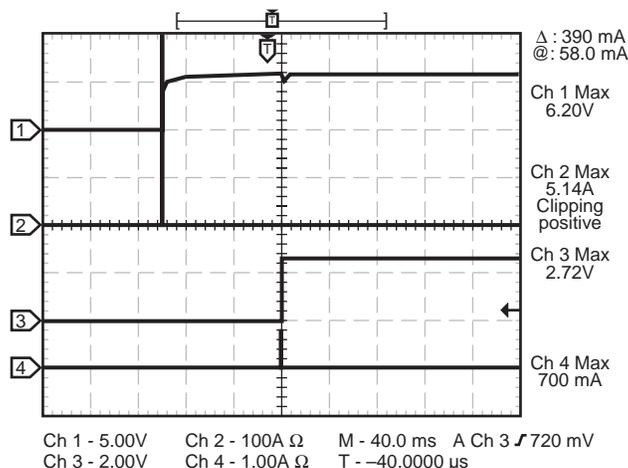
Device	T_A (°C)	Available Current (mA)	C_0 (µF)	Signals (Top Down)
XC2S150	25	800	320	V_{SRC}, I_{SRC}. V_{CCINT}, I_{CCINT}

Figure 10: **Regulator-Based Power-Assist Circuit Powered by AC-to-DC Adapter**

Power-Assist Circuit with P-Channel MOSFET

All power-assist circuit address the same need, enabling the FPGA to turn on when the power supply's maximum rated output is less than I_{CCPO} min. These circuits all employ a large capacitor (C_0) to store the power-on current as well as a switch to hold off turning-on the FPGA until C_0 is charged. The switch can be implemented in different ways. The previous section used a regulator with an enable feature. This section uses a P-Channel MOSFET and the next section, a Silicon-Controlled Rectifier.

There are a number of reasons for using a PFET-based power-assist circuit:

First, if the power voltage that the FPGA needs (2.5V for Spartan-II and 1.8V for Spartan-IIE) goes directly to the board, a regulator is not needed for the purpose of DC-to-DC conversion. Then the PFET should be used as a way of implementing a power switching function.

Second, the PFET can be used to set a current limit close to (but not below) the I_{CCPO} min. specification and the maximum operating current requirement. This helps keep the size of C_0 small. Furthermore, if an over-current protection circuit is present on the board, it avoids the risk of a supply shutdown when encountering a large POS current.

Third, it is possible to slow the V_{CCINT} ramp using a PFET with a resistor-capacitor net connected to its gate. This benefit proves helpful when powering Spartan-IIE devices, which require a V_{CCINT} ramp no faster than 2 ms. (Spartan-II devices have no such requirement.)

Of the various kinds of transistors available, the PFET is particularly well suited to power-assist applications. First, PFETs are readily available that can handle the largest POS currents. Second, it has a low on resistance (around 0.05Ω), which minimizes the voltage drop on the supply line. Third, it turns on with a gate volltage (V_G) that is lower than the source voltage (V_S). Thus, switching the transistor does not require a voltage higher than V_{CCINT}.

Figure 11 shows the schematic of a power-assist circuit that uses a PFET to implement the switch function. As before, C_0 stores the charge needed to produce the POS current. The PFET is placed with its source lead connected to the power supply output (the voltage of which is V_{SRC}) and its drain lead connected to the V_{CCINT} pins of the FPGA. The gate lead is tied to C_{TIME} and R_1, which determine the time it takes to turn on the PFET as well as the V_{CCINT} ramp rate.
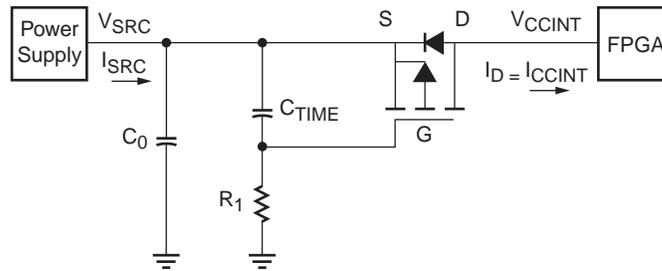
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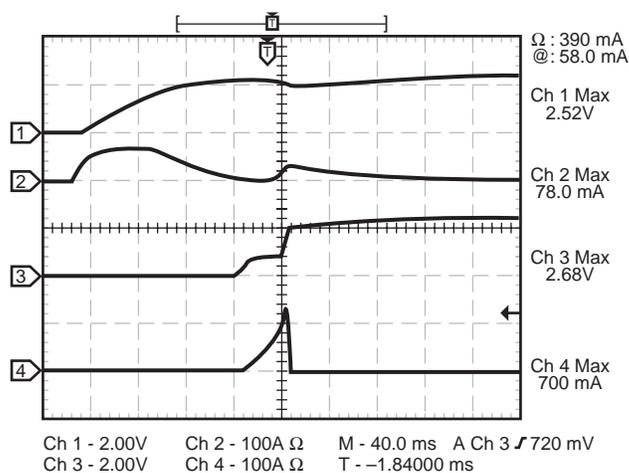*Figure 11:* **PFET-Based Power-Assist Circuit Schematic**

The circuit operates as follows. Once turned on, the power supply charges C_0 and V_{CCINT} begins to rise from the ground potential. At first, most of the V_{SRC} voltage falls across R_1, with very little across C_{TIME}. This means that the gate voltage (V_G) is close to V_{SRC} and the PFET is off. As C_{TIME} charges, an increasing proportion of V_{SRC} falls across C_{TIME}, driving down V_G. When V_{GS} reaches the turn-on threshold, the PFET turns on, permitting C_0 to discharge. Upon receiving the resulting current the FPGA powers on.

C_0, C_{TIME}, and R_1 are calculated using much the same equations presented earlier for the regulator-based power-assist circuit. C_{TIME} and R_1 correspond to C_{DLY} and R_{DLY}, respectively. I_{LIMIT} from the regulator example becomes the effective current limit of the PFET during the power-on period. V_{OFFSET} becomes the voltage across the PFET, which is determined by the on resistance times I_{LIMIT}. The excel file discussed in the **"Power-Assist Spreadsheets"**, page 11 section can be used to estimate the component values under various conditions. The PFET must be able to carry a current at least the size of I_{CCPO} min.

This PFET-based power-assist circuit was built and tested using an XC2S150 FPGA and a Siliconix Si3445DV PFET with a gate-to-source turn-on voltage ($V_{GS(th)}$) of –0.45V. V_{SRC} is at the nominal operating V_{CCINT} level. For the Spartan-II device, it is 2.5V. The maximum current available from the supply was 100 mA. C_0 was 3200 µF. C_{TIME} and R_1 were 0.69 µF and 100 KΩ, respectively. All measurements were made at an ambient temperature of 25°C.

The waveforms representing the two-port model of the PFET-based power-assist circuit are shown Figure 12. From top to bottom, the traces are V_{SRC}, I_{SRC}, V_{CCINT}, and I_{CCINT}. Starting in the upper left-hand corner, the power supply turns on and V_{SRC} begins to rise. The leftmost pulse of I_{SRC}, representing a current of 78 mA, charges C_0 and C_{TIME}. When these capacitors are charged, I_{SRC} drops back to 0. V_{SRC} increases as V_G falls, so magnitude of V_{GS} increases over time. Once that magnitude has reached about 0.8V, the PFET turns on and V_{CCINT} begins to rise. When V_{CCINT} is between 0.6V and 0.8V, the I_{CCINT} trace shows a POS current of

114 mA. Because the POS current is larger than I_{SRC}, the criterion for successful power-assist operation is met.

Device	T_A (°C)	Available Current (mA)	C_0 (μF)	Signals (Top Down)
XC2S150	25	100	3,200	V_{SRC}, I_{SRC}. V_{CCINT}, I_{CCINT}

Figure 12: **PFET-Based Power-Assist Circuit Two-Port Waveforms**

Using the PFET to Control the V_{CCINT} Ramp

The PFET circuit just discussed also controls the V_{CCINT} ramp rate. This function is useful for Spartan-IIE devices, which have a minimum V_{CCINT} ramp time requirement of 2 ms. (Spartan-II devices do not have this requirement.) For many power supplies, V_{CCINT} will rise quickly such that the ramp time requirement is not met. It is possible to slow down the ramp by inserting the PFET (drain-to-source) in the power path between the supply and the FPGA (as was shown in Figure 11). By increasing the value of C_{TIME}, the PFET can be made to produce a V_{CCINT} ramp time of 2 ms or slower. For the test results of the regulator-based power-assist circuit shown in Figure 7, the V_{CCINT} ramp time was 640 μs (which is acceptable for a Spartan-II device). After inserting a PFET source-to-drain between the regulator output and the FPGA's V_{CCINT} pins (C_{TIME} = 0.69 μF and R_1 = 100 KΩ), the V_{CCINT} ramp time increased to 10 ms.

Using the PFET to Set a Current Limit

The PFET can also be used to implement a current limit. For the power-assist circuit shown in Figure 11, this helps keep C_0 small. It can also be used to set a maximum limit on the size of the POS current, which becomes important when over-current circuit protection is present on the board. In this case, it is possible to avoid an inadvertent shutdown of the supply line by setting a current limit below the foldback trip point. This approach is described at length in **XAPP450**, in the section called "Using FPGAs with Over-Current Protection".

The output characteristics of the Si3445DV PFET are graphed in Figure 13. The absolute values of V_{GS} are shown so that these curves resemble the more familiar NFET curves. The V_{GS} values ranging from 1V to 2.5V are actually negative since V_G is lower than V_S when the transistor is on. The PFET provides current-limiting behavior when it is in saturation. In this case, the drain current (I_D) is independent of the voltage from the drain to the source (V_{DS}). The PFET is in saturation when the following condition is met:
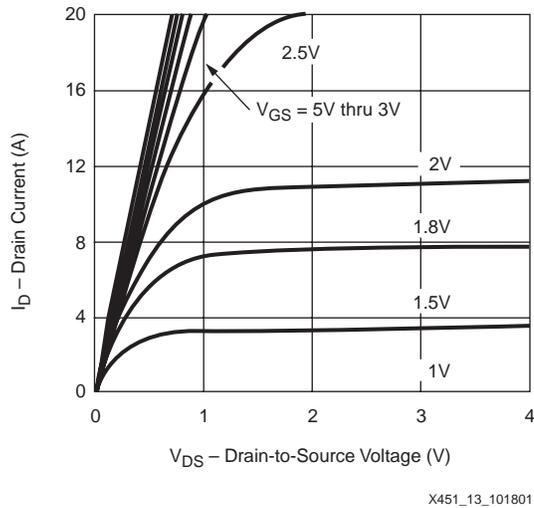
$$V_{DS} < V_{GS} - V_T$$

Figure 13: **Si3445DV Output Characteristics**

Power-Assist Circuit with SCR

Another variant of the power-assist circuit combines uses a Silicon-Controlled Rectifier (SCR) to perform the switch function that holds off powering the FPGA until C_0 is completely charged. The SCR is a three-junction device that is created by stacking four doped semiconductor layers in the order PNPN. The SCR has three terminals: The anode connects to the p layer that terminates the stack. The cathode is tied to the n layer at the other end of the stack. The gate connects to the inner p layer. By toggling a signal applied to the gate lead, this device is capable of switching large currents flowing from the anode to the cathode very quickly.

There are a number of distinct benefits arising from the use of the SCR-based power-assist circuit:

First, when the SCR is conducting, it exhibits a 0.8V drop from anode to cathode. It follows that the SCR can be used to convert the power voltage from 3.3V down to the 2.5V-level that Spartan-II devices need at the V_{CCINT} lines. In this case, a regulator for the purposes of DC-to-DC conversion is unnecessary. Similarly, an SCR plus in series with a silicon diode produces a total voltage drop of 1.5V, which can serve as a level conversion from 3.3V down to 1.8V, the nominal power voltage for Spartan-IIE.

Second, by adding a resistor in series with C_0, it is possible to slow the V_{CCINT} ramp, which helps meet the 2 ms minimum V_{CCINT} ramp time requirement of Spartan-IIE devices.

Other advantages specific to the SCR include the following: The SCR can carry short-lived current surge many times its continuous current rating. Also, the SCR turns on with a gate voltage (V_G) that is lower than the anode voltage (V_A). Thus, the power-assist circuit will not need any voltage higher than V_{SRC}.

Figure 14 shows the schematic of an SCR-based power-assist circuit. C_0 stores the charge needed for the POS current. R_2 (optional) slows the V_{CCINT} ramp by limiting the current discharged from C_0. The SCR has its anode connected to the power supply's output (the voltage of which is V_{SRC}) and its cathode connected to the FPGA's V_{CCINT} pins. The gate is tied to R_1 and C_{TIME}, which delay turning on the SCR.

The circuit operates in the following way. Once on, the power supply charges C_0 and V_{CCINT} starts to rise. At first, nearly all of the V_{SRC} voltage falls across R_1, with only a little across C_{TIME}. This means that the gate voltage (V_G) is close to ground potential and the SCR is off. As C_{TIME} charges, an increasing proportion of V_{SRC} falls across C_{TIME}, causing V_G to rise. When V_{GS} reaches the turn-on threshold, the SCR turns on, allowing C_0 to discharge. The resulting current powers on the FPGA.
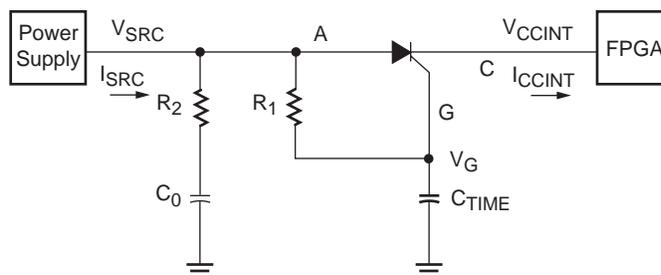
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Figure 14: **SCR-Based Power-Assist Circuit Schematic**

C_0, C_{TIME}, and R_1 are calculated using equations similar to those originally presented for the regulator-based power-assist circuit. C_{TIME} and R_1 perform the same function as C_{DLY} and R_{DLY}. V_{OFFSET} is measured across the SCR FROM anode to cathode. As mentioned earlier, this voltage drop is around 0.8V. The file discussed in the **"Power-Assist Spreadsheets"**, page 11 section can be used to estimate the component values under various conditions.

An alternative version of the circuit constructs an SCR out of bipolar transistors, an NPN and a PNP. The two-transistor version functions exactly the same way as the integral SCR component, only it is likely to be less expensive. The schematic shown in Figure 15, employing a 2N2222 for the NPN and a 2N2907 for the PNP, was built and evaluated in the lab. The measured gate turn-on threshold was 0.6V. As in previous examples, the FPGA on the board was an XC2S150. V_{SRC} was set to 3.3V. The maximum current available from the supply was 100 mA. C_0 was 2600 μF. C_{TIME}, R_1, and R_2 were 10 μF, 100 KΩ and 3.9Ω, respectively. All measurements were made at an ambient temperature of 25°C.
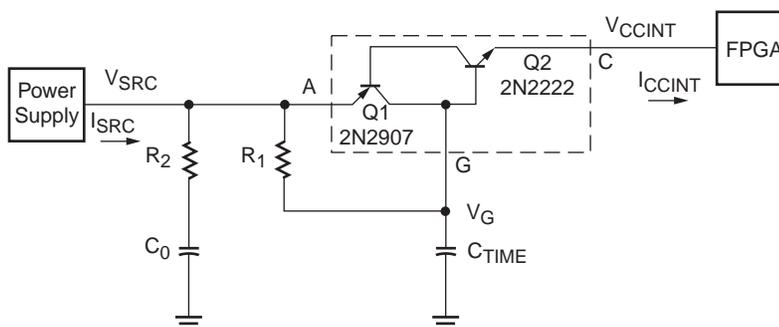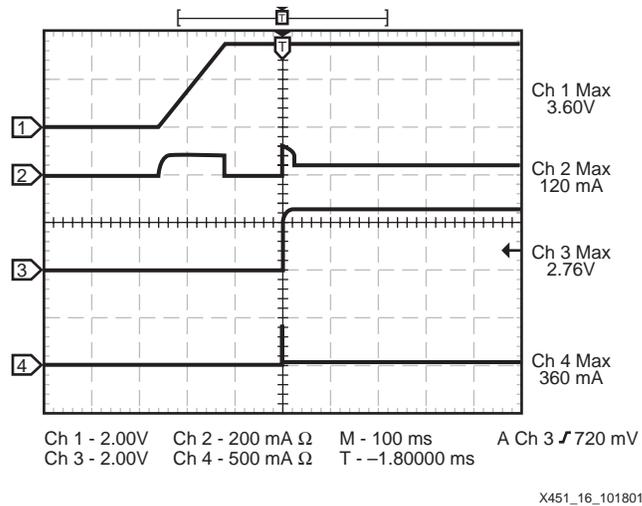

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Figure 15: **Power-Assist Using an SCR Made Up of Two Bipolar Transistors**

The waveforms representing the two-port model of the SCR-based power-assist circuit are shown Figure 16. From top to bottom, the traces are V_{SRC}, I_{SRC}, V_{CCINT}, and I_{CCINT}. Starting in the upper left-hand corner, the power supply turns on and V_{SRC} begins to rise. The leftmost pulse of I_{SRC}, representing a current of about 100 mA, charges C_0 and C_{TIME}. When these capacitors are charged, I_{SRC} drops back to 0. As V_{SRC} rises, V_G also rises, only at a slower rate. Once V_G has reached about 0.6V, the SCR turns on and V_{CCINT} begins to rise. When

V_{CCINT} is between 0.6V and 0.8V, the I_{CCINT} trace shows a POS current of 400 mA. Because the POS current is larger than I_{SRC}, the criterion for successful power-assist operation is met.

| Ch 1 - 2.00V | Ch 2 - 200 mA Ω | M - 100 ms | A Ch 3 ∫ 720 mV |
| Ch 3 - 2.00V | Ch 4 - 500 mA Ω | T - –1.80000 ms | |

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Device	T_A (°C)	Available Current (mA)	C_0 (μF)	Signals (Top Down)
XC2S150	25	100	2,600	V_{SRC}, I_{SRC}, V_{CCINT}, I_{CCINT}

Figure 16: **SCR-Based Power-Assist Circuit Two-Port Waveforms**

Controlling the V_{CCINT} Ramp with the SCR-Based Power-Assist Circuit

The addition of a small resistor in series with C_0 can be used to slow the V_{CCINT} ramp. This optional resistor, called R_2, is shown in Figure 14 and Figure 15. This function can facilitate meeting the 2 ms minimum V_{CCINT} ramp time requirement that applies to Spartan-IIE devices. The tests in this section used an R_2 value of 3.9Ω, which produced a V_{CCINT} ramp time of 4 ms.
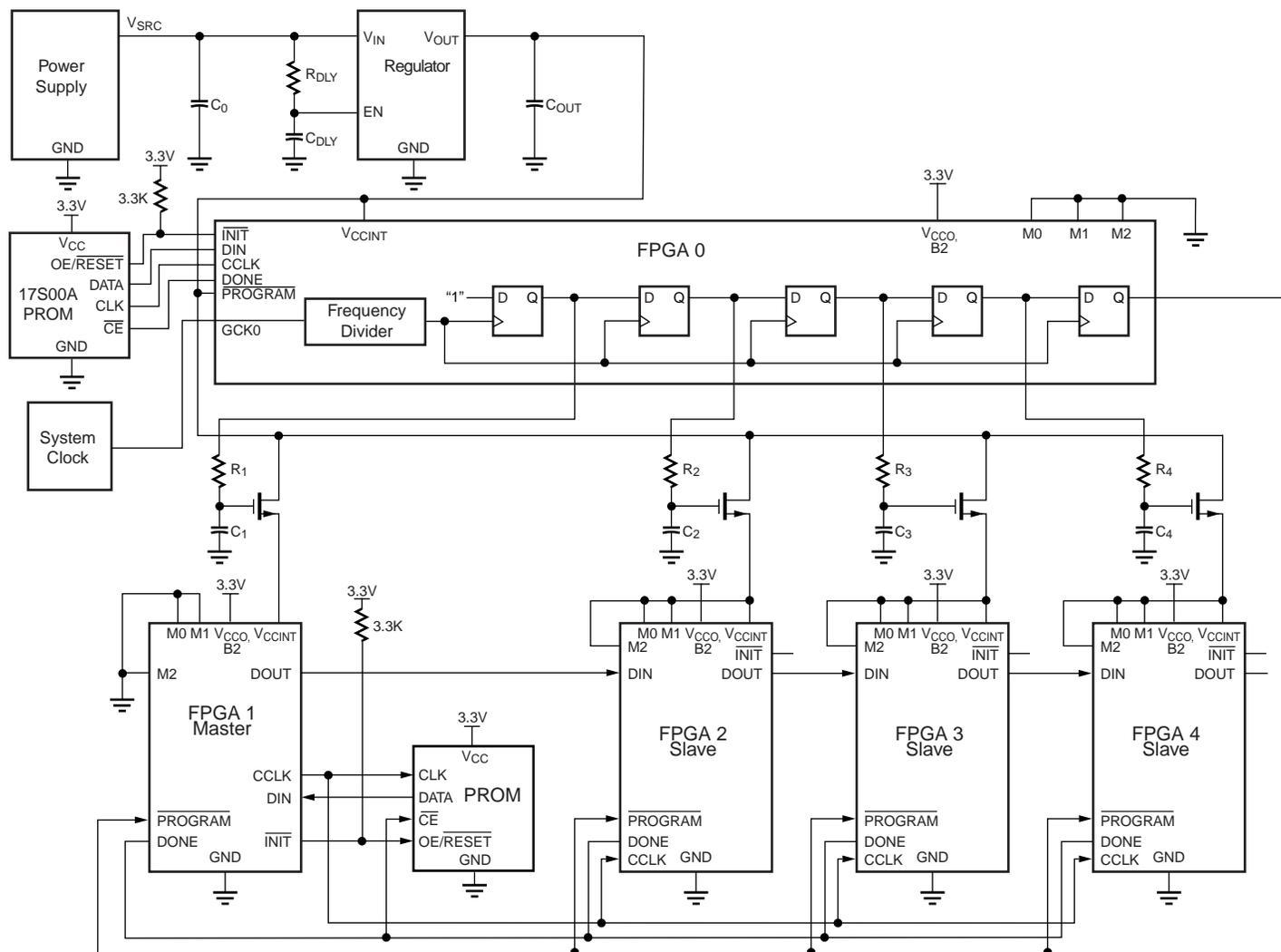
Powering up Multiple FPGAs

Designing a supply for powering on multiple FPGAs deserves special attention. The power-on behavior of multiple FPGAs is described in the "Board Power Considerations" section of **XAPP450**. The power supply must be able to source the sum total of the POS current requirements for all FPGAs turning on simultaneously. This total current can be quite large. Designs that must operate at very cold temperatures (e.g., close to –40°C) will encounter the largest current levels. In this case, the minimum POS current for each FPGA is 2A and the board may require as much as several Amperes to power-on all the FPGAs at once.

Two approaches can be taken to minimize the total POS current requirement: First, the FPGAs can be turned on in sequence, one after the other (known as staggering power-on). Second, a power-assist circuit with a large capacitor can be used. It is possible to implement these approaches either independently or together.

One possible implementation of the combined approach is shown in Figure 17. The schematic shows five FPGAs that are numbered according to the order in which they power-on: FPGA 0 turns-on first, followed by FPGA 1, then FPGA 2, etc. One 17S00A series PROM configures FPGA 0 and a 1700 PROM configures the remaining FPGAs. The mode pins are set to select master serial configuration for FPGAs 0 and 1 and slave serial configuration for FPGAs 2 through 4. In the upper right-hand corner is the power supply for the board. Without a power-assist capacitor, 2A per FPGA would be necessary for operating at cold temperatures (e.g., Spartan-II devices below 0°C or Spartan-IIE industrial devices). Just to the right, an optional power-assist circuit is shown that makes use of a large capacitor (C_0) and a regulator's enable feature. This will be described at the end of the section.

The resources of all five FPGAs taken together make up the logic fabric of a particular product's design. A little spare logic from FPGA 0 is used to construct a frequency divider and five registers. The frequency divider accepts the system clock signal and generates a reduced-frequency clock signal, such that one clock period covers the time necessary to power-on a single FPGA.

Note: If the bitstream generator option "DriveDone" in the Xilinx development software is not selected, add a 330Ω pull-up resistor to the DONE line.

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Figure 17: **Schematic for Powering On Multiple FPGAs in Sequence**

The reduced-frequency signal clocks a string of five registers connected D-to-Q. The Q signals of the first four registers (from the left) exit the FPGA. Each connects to the gate of an N-channel transistor. Each transistor is placed drain-to-source in the path from the power supply to one of the FPGAs labeled 1 through 4. The transistors are designed to carry large currents (on the order of Amperes). Their low on resistance means that the voltage drop from the drain to the source will be small. In order to turn on, the NFET needs a gate-to-source voltage greater than a certain positive threshold (say 0.8V). Thus, the gate voltage has to be higher than V_{CCINT}. This is accomplished by powering the IOBs of FPGA 0 with a V_{CCO} supply of 3.3V. The Q signal of the last (rightmost) register also exits FPGA 0 and connects to the $\overline{PROGRAM}$ input of FPGAs 1 through 4.

FPGAs 1 through 4 are connected to form a standard daisy chain for serial configuration from a second PROM. See Module 2 of the Spartan-II and Spartan-IIE data sheets for information

on daisy-chain operation. The DONE lines of FPGAs 1 through 4 are tied together. The "DriveDone" bitgen option in the Xilinx development software is set to "no" (open drain operation) for the FPGAs 1 through 3. The option is set to "yes" for the last FPGA in the chain, FPGA 4.

Passing over the effect of C_0 for the moment, the circuit operates as follows: Once the power supply is turned on, FPGA 0 configures itself from the dedicated 17S00A PROM. As soon as FPGA 0 enters user mode, the five internal registers are reset and the frequency divider begins to clock them. A logic level High (signified by "1" in Figure 17) is passed from register to register. When the High level appears on the Q output of the first register (on the left), the associated NFET turns on, conducting power to the VCCINT pins of FPGA 1. Configuration is held off, since the Q output of the right-most register drives the $\overline{PROGRAM}$ input of FPGAs 0 through 4 Low. When the power-on of FPGA 1 is complete, the High logic level is passed from the first register inside FPGA 0 to the Q output of the next register in line. The associated NFET turns on, powering FPGA 2. Clocking continues until the remaining FPGAs power on and the High logic level reaches the Q output of the right-most register, de-asserting $\overline{PROGRAM}$ for FPGAs 1 through 4. At this point, FPGA 1 first configures itself from the second PROM and then passes the bit-stream on to FPGAs 2 through 4. When configuration is complete for all devices, DONE goes High, marking the transition to user mode.

If the five-FPGA application operates at temperatures below 0°C, the power supply would never have to provide more than 2A. With the addition of the power-assist capacitor (C_0), still less supply current is possible. Power-assist design considerations include the following:

C_0 charges and discharges for the power-on of each FPGA. Thus, the clock signal coming out of the frequency divider must have a period that covers the capacitor recharge time as well as the FPGA power-on time.

The variable V_{CCPO}, introduced in the **"Calculating the Value for C_0"**, page 8 section, is the lowest voltage to which V_{CCINT} may dip during FPGA power-on. When staggering power-on, once an FPGA is turned on, V_{CCINT} must not dip below its minimum specified nominal voltage. Thus, V_{CCPO} is set to 2.5V – 5% for Spartan-IIE devices and 1.8V – 5% for Spartan-IIE devices (These numbers come from the respective data sheets). Because V_{CCPO} is higher than the value used for the single FPGA case, the C_0 value will be larger.

Conclusion

The Spartan-II and Spartan-IIE families require a minimum supply current (I_{CCPO}) to guarantee successful power-on. The requirement only applies during the power-on period (typically, a few milliseconds). For designs using the smaller members of the Spartan-II and Spartan-IIE families, the I_{CCPO} min. number may be larger than the operating current. This situation is unlikely to require a larger supply than would otherwise be necessary, since many supplies can source more current to meet short-term demand than their continuous output rating would indicate. For such a supply, it is appropriate to match the continuous output current capability with the design's operating current requirements and the instantaneous output current capability with I_{CCPO} min. These designs would not need any additional components to facilitate power-on.

Other designs with stringent power current budgets (e.g., those powered from a data bus or interface) can benefit from a variety of simple, low cost power-assist solutions that permit

supply current levels less than I_{CCPO} min. to successfully power on Spartan-II and Spartan-IIE devices. The solutions discussed in this application note are summarized in Table 2.

Table 2: **Summary of Power-Assist Circuits**

Power-Assist Circuit	Switch Implementation	When to Use
Regulator-based	LDO Regulator • Must have enable port • Avoid foldback feature	• Stepping from supply voltage down to the FPGAs nominal V_{CCINT} voltage • Regulator is already present on board
PFET-based	P-channel MOSFET • Low on-resistance • Must be able to handle power current	• FPGAs V_{CCINT} voltage is directly available from supply (no step-down necessary) • Use to slow V_{CCINT} ramp time (to comply with Spartan-IIE minimum requirement) • Set a current limit to avoid tripping over-current protection circuit
SCR-based	Silicon-Controlled Rectifier • Construction of NPN and NPN transistors • Must be able to handle power current	• Stepping from 3.3V supply down to the FPGA's nominal V_{CCINT} voltage. (Spartan-IIE uses an additional diode for a larger step.) • Use to slow V_{CCINT} ramp time (for compliance with Spartan-IIE minimum requirement).

References

Power-On Requirements for the Spartan-II and Spartan-IIE Families (**XAPP450**)

Powering Xilinx Spartan-II FPGAs (**XAPP189**)

Spartan-II 2.5V FPGA Family: DC and Switching Characteristics (**Module 3 of the Spartan-II Data Sheet**)

Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics (**Module 3 of the Spartan-IIE Data Sheet**)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/15/01	1.0	Initial Xilinx release.