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DDR SDRAM DIMM Interface for Virtex-II Devices

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Summary

This application note describes the Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) Dual In-line Memory Module (DIMM) controller. This controller is implemented in a Virtex™-II device and is part of a system design with the Universal Serial Bus (USB 2.0) as the user interface. The DDR SDRAM DIMM used in this reference design is the Micron, Inc., 256-MB MT16VDDT3264A.

Introduction

DDR SDRAM DIMM memories are generally used on Personal Computer (PC) motherboards as main memory. The DDR SDRAM DIMM in this application is used for collecting and analyzing large numbers of data samples in real time. This aids the development of RAM intensive Digital Signal Processing (DSP) algorithms in Virtex-II devices. The MT16VDDT3264A is a 184-pin module using eight 100 MHz or 133 MHz DDR SDRAM MT46V16M8 type components. The I/O standard required by the DDR SDRAM DIMM is SSTL_2, Class II with a $V_{DD} = V_{DDQ} = 2.5V$, $V_{REF} = V_{DDQ}/2$, and $V_{TT} \sim V_{REF}$.

A brief overview of the DDR SDRAM DIMM is presented followed by a detailed description of the controller design.

DDR SDRAM DIMM Overview

The MT16VDDT3264A module is internally configured with four banks of DDR SDRAM components. The DDR SDRAM components use double data rate architecture to achieve high speed. These components have a bidirectional data strobe signal (DQS) that is transmitted along with data to enable data capture at the receiver. DQS is transmitted by the DDR SDRAM during read operations and is edge-aligned with the data being read. The memory interface controller during write operations transmits DQS, and it is center-aligned with data being written to the DDR SDRAM.

The DDR SDRAM requires differential clocks (CK and $\overline{CK}$), and the positive edge of the clock is defined as the crossing of CK transitioning High and $\overline{CK}$ transitioning Low. All the commands are registered at the positive edge of CK. Input data is registered on both the edges of DQS, and the output data is referenced to both edges of DQS as well as to both edges of CK.

Data accesses to and from the DDR SDRAM components are burst oriented starting at a selected location. Programmable burst lengths of 2, 4, or 8 are provided. Note that the minimum burst length is 2. The data bus is 64-bits wide. Read or write accesses begin with an ACTIVE command followed by the READ or WRITE command. The ACTIVE command is used to activate a row for a subsequent read or write access. The address provided with the ACTIVE command selects the bank and the row address. The address provided with the READ or WRITE command selects the bank and the starting column address. The memory controller can issue consecutive READ or WRITE commands (without an ACTIVE command) when all the data to be accessed is from the same row address until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank. The PRECHARGE command deactivates the open row in a particular bank or in all banks (PRECHARGE ALL) determined by the A10 bit (A10 = 0, PRECHARGE).

The memory controller needs to issue an AUTO REFRESH command to the DDR SDRAM every 15.6 µs. When the AUTO REFRESH command needs to be issued during a read or write access, the memory controller will not issue this command as long as the time between two consecutive AUTO REFRESH commands is not more than 140.6 µs.

Initialization

After the DDR SDRAM DIMM module is powered up, a 200 µs delay is required prior to issuing an executable command. After the 200 µs delay, the DDR SDRAM components have to be initialized in a predefined sequence as listed below. At the end of this sequence of commands, the DDR SDRAM component is ready for normal operation.

Predefined Sequence of Commands:

1. DESELECT or NOP command
2. PRECHARGE ALL
3. LOAD MODE REGISTER
4. LOAD MODE REGISTER
5. PRECHARGE ALL
6. AUTO REFRESH
7. AUTO REFRESH
8. LOAD MODE REGISTER

Mode Register

The mode register is used to define the burst type, burst length, Column Address Strobe ($\overline{CAS}$) latency, and operating mode of the DDR SDRAM component. The mode register can be accessed during the LOAD MODE REGISTER command by setting BA0 = 0 and BA1 = 0. Figure 1 shows the different fields in the mode register. The mode register is loaded using the address bits (A0-A11) and the bank address bits (BA0-BA1).

Burst type can be set to either sequential or interleaved.

Burst length can be set to 2, 4, or 8. A burst length of 4 indicates that four 64 bits of data will be available on the data bus at a rate of 200 Mb/s (both edges of 100 MHz clock).

Read latency or CAS latency is defined as the delay in clock cycles between the registration of a READ command and the availability of the first bit of output data on the bus. CAS latency can be set to 2 or 2.5 clock cycles.

Operating mode can be set to either normal operation or Delay Locked Loop (DLL) reset.

Extended Mode Register

The extended mode register can be accessed by setting BA0 = 1 and BA1 = 0. The extended mode register controls functions such as DLL enable/disable, output drive strength, and $\overline{QFC}$ function (used to control isolation switches on modules).

Notes:

1. The reduced drive strength option is not supported for the DDR SDRAM component being used in this application.
2. This $\overline{QFC}$ function is not supported for the DDR SDRAM component being used in this application.

Read Operation

The READ command is used to initiate a burst read access to an activated row in a bank selected by BA0-BA1 and the starting column address selected by A0-A9. The value of A10 determines whether or not auto precharge is required. In this memory controller design, the AUTO PRECHARGE command is not used due to the requirement for consecutive read or write accesses and the BURST TERMINATE option during READ.

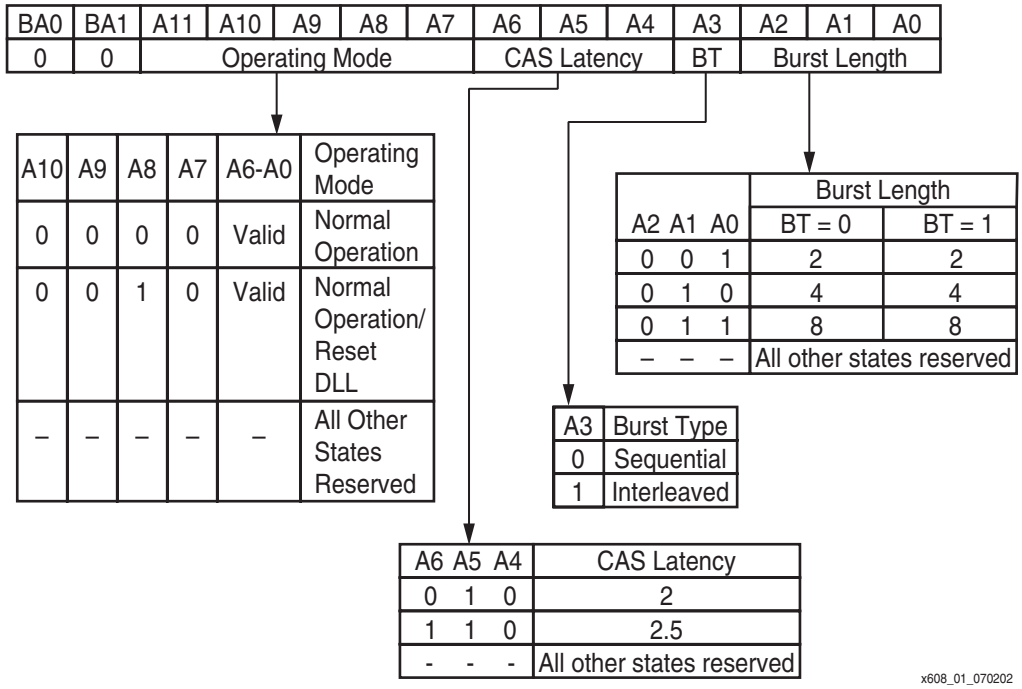

Figure 1: **Mode Register Definition**

Figure 2 shows the waveform of a READ command with a Burst size of 4 and a CAS Latency of 2. Note that the address during the READ command is that of the column to be accessed (A0-A9). The row address (A0-A11) is given during an ACTIVATE command issued just before the READ command.

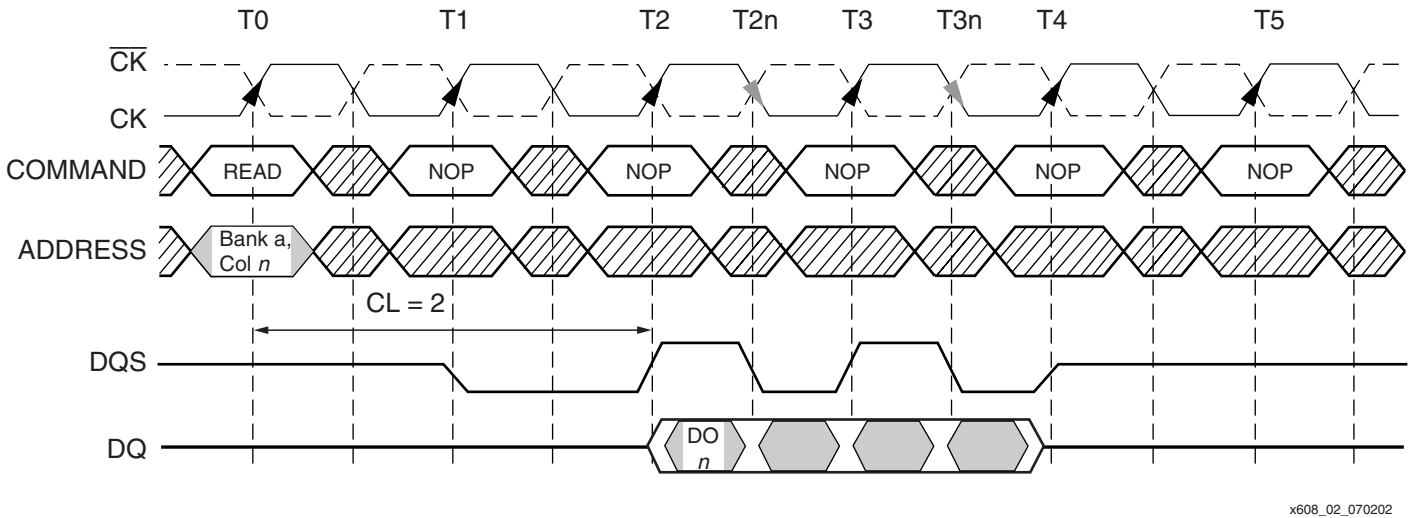

Figure 2: **READ Burst 4 with CAS Latency 2**

Write Operation

The WRITE command is used to initiate a burst write access to an activated row in a bank selected by BA0-BA1 and the starting column address selected by A0-A9. Input data is written to the memory array depending on the Data Mask (DM) input logic level coincident with the data. If DM signal is Low, then the corresponding data will be written to the addressed memory location, or else the corresponding data will be ignored and will not be written to the addressed column location.

Figure 3 shows the waveform of a WRITE command with a Burst size of 4 and a nominal t_{DQSS} of one clock cycle. The address during the WRITE command is that of the column to be accessed (A0-A9). The row address (A0-A11) is given during an ACTIVATE command issued just before the WRITE command.

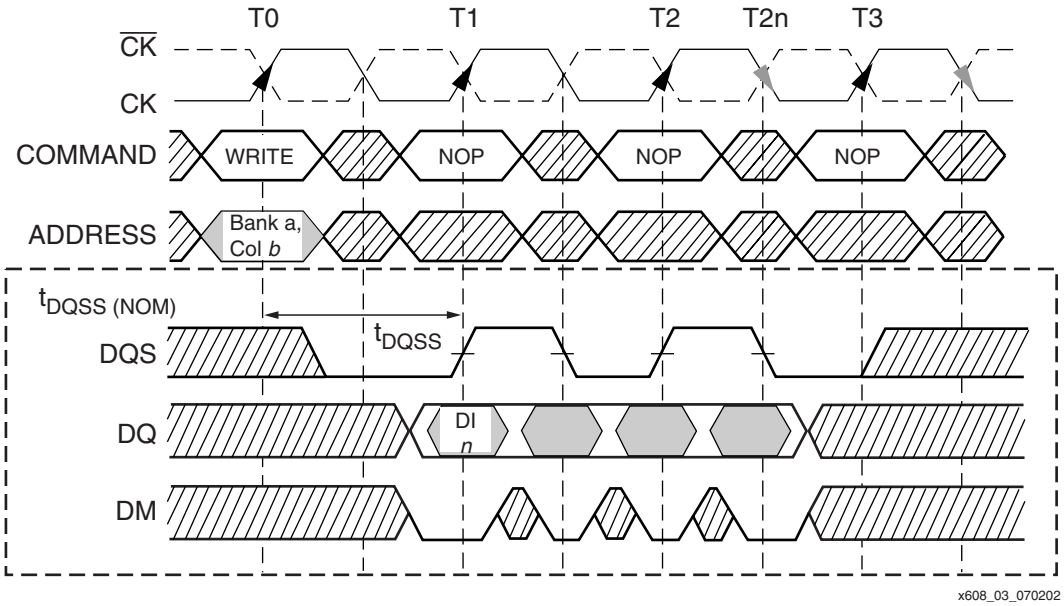

Figure 3: **WRITE Burst 4 with Nominal t_{DQSS} of One Clock Cycle**

DESELECT/No Operation (NOP)

The DESELECT command requires a logic High on the Chip Select ($\overline{CS}$) input. The $\overline{CS}$ input is logic Low for the NOP command. Both these commands prevent the DDR SDRAM component from executing unwanted commands during idle or wait states.

Burst Terminate

The BURST TERMINATE command is used to truncate read bursts.

Table 1: **Burst Terminate Command Truth Table**

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
DESELECT (NOP)	H	X	X	X	X
No Operation (NOP)	L	H	H	H	X
ACTIVE (Select Bank and Activate Row)	L	L	H	H	BA0-BA1 A0-A11
READ (Select Bank and Column and Start READ Burst)	L	H	L	H	BA0-BA1 A0-A9
WRITE (Select Bank and Column and Start WRITE Burst)	L	H	L	L	BA0-BA1 A0-A9
BURST TERMINATE	L	H	H	L	X
PRECHARGE (Deactivate Row in Bank or Banks)	L	L	H	L	A10 = H All Banks
AUTO REFRESH or SELF REFRESH	L	L	L	H	X
LOAD MODE REGISTER	L	L	L	L	BA0-BA1 A0-A11

Notes:

1. During a LOAD MODE REGISTER command, BA0-BA1 selects either the mode register or the extended mode register. BA0=0, BA1=0 selects the mode register, and BA0=1, BA1=0 selects the extended mode register. A0-A11 provides the data to be written to the selected mode register.
2. CKE (Clock Enable) is High for all commands except SELF REFRESH.
3. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are Active Low signals.

Notes:

1. Most of the text from the previous section was taken from Micron Technology, Inc. product data sheets for MT16VDDT3264A and MT46V16M8. For a detailed functional and timing specification, refer to their web site at: www.micron.com

DDR SDRAM DIMM Interface Controller

Figure 4 shows the top-level bock diagram with the user interface and the DDR SDRAM DIMM signals. The DDR SDRAM DIMM controller block diagram in Figure 5 shows the major modules in this design. There are three state machines in this design namely, the main state machine, the read state machine, and the write state machine. The main state machine comprises the following states: IDLE or NOP, LOAD MODE REGISTER, PRECHARGE, AUTO REFRESH, and ACTIVE. The read state machine comprises the following states: READ_WAIT or NOP, BURST_READ, and BURST_STOP or BURST_TERMINATE. The write state machine comprises the following: WRITE_WAIT and BURST_WRITE states. Flags are used to jump from one state machine to the other and they are mutually exclusive, that is, when one state machine is in operation the other two are in the IDLE or NOP states.

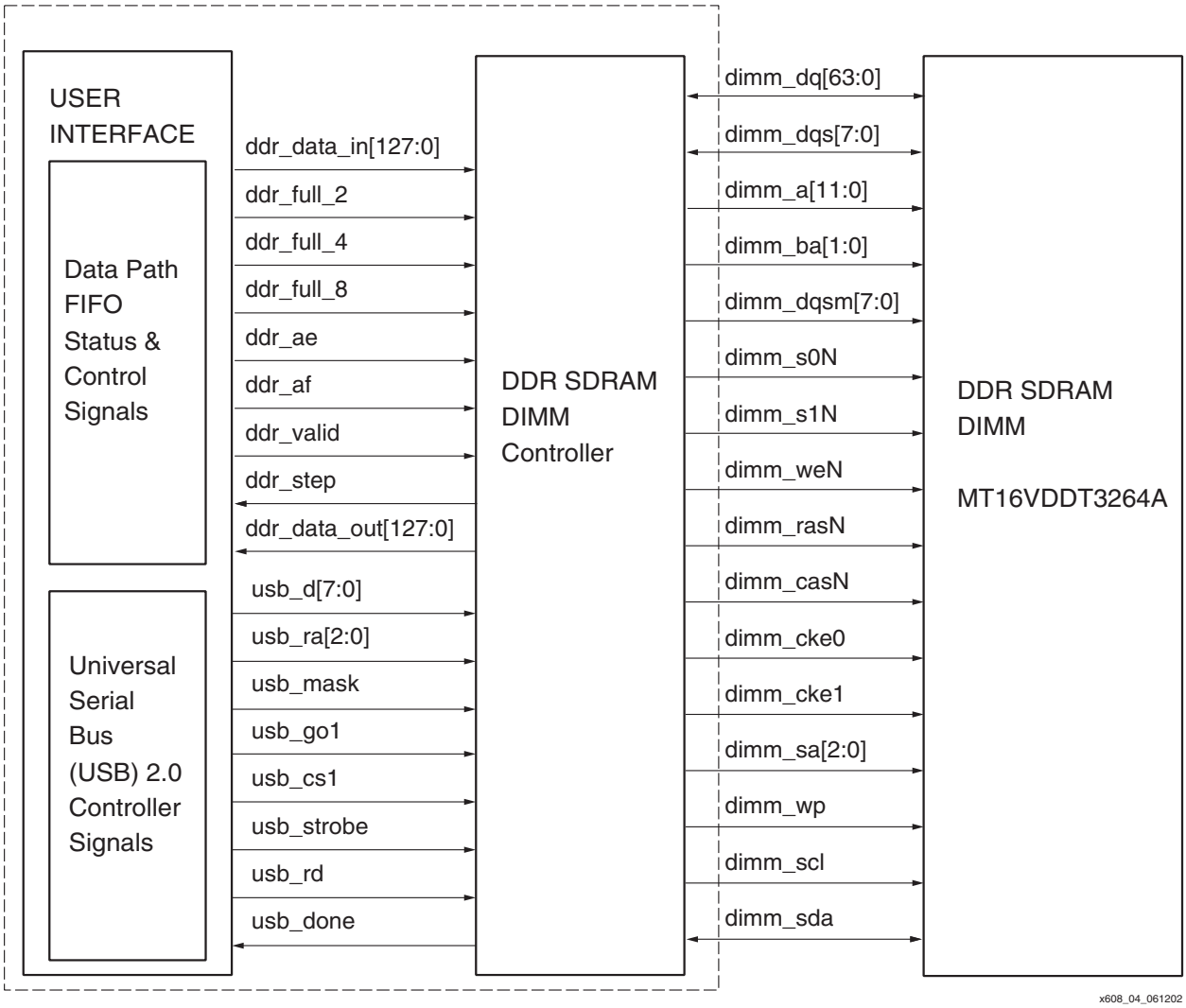

Figure 4: **DDR SDRAM DIMM Interface Top-Level Block Diagram**

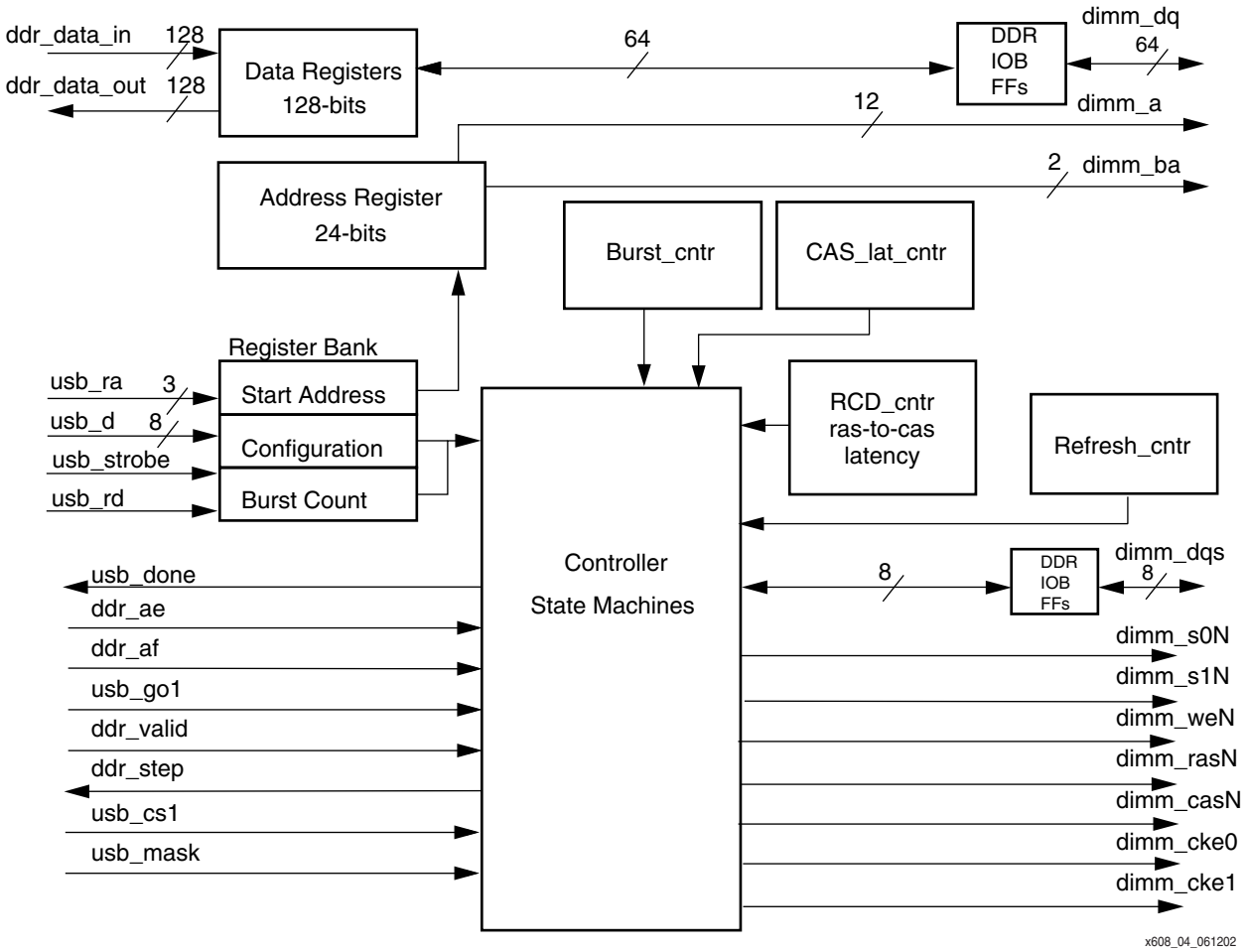

Figure 5: **DDR SDRAM DIMM Interface Controller Block Diagram**

Main State Machine

The details of the main state machine are shown in Figure 6. On reset, the state machine transitions to the IDLE or NOP state. Once the reset is de-asserted for a READ command to be executed, the following sequence of commands need to be executed: LOAD MODE REGISTER, ACTIVE, BURST_READ, and PRECHARGE All (address A[10] = 1) in that order. After the LOAD MODE REGISTER command, the read flag is set when the usb_go1 signal is asserted by the USB controller, and the ddr_ae (FIFO almost empty) is asserted. The setting of the read flag indicates that an ACTIVE command should be issued. After a delay of t_{RCD}, a BURST_READ command is executed followed by the PRECHARGE All (address A[10] = 1) command.

Similarly for a WRITE command to be executed, the following sequence of commands need to be executed: LOAD MODE REGISTER, ACTIVE, BURST_WRITE, and PRECHARGE All (address A[10] = 1) in that order. At the end of the LOAD MODE REGISTER command, the write flag is set when the usb_go1 signal is asserted, and either the ddr_full_2, ddr_full_4, or ddr_full_8 signal is asserted. The setting of the write flag indicates that an ACTIVE command should be issued. After a delay of t_{RCD}, a BURST_WRITE command is executed followed by the PRECHARGE All (address A[10] = 1) command.

Note that for consecutive read and write accesses to the same row and same burst size, a burst FULL option is provided in this design. The burst FULL option saves the user the overhead of the following commands: LOAD MODE REGISTER, ACTIVE, and PRECHARGE All (address A[10] = 1). The LOAD MODE REGISTER command must be executed each time a new start

address must be provided or the burst size must be changed. This design does not support the interleaved burst type, only sequential. The CAS latency is set to two clock cycles. However, the user has the option to change it to 2.5 clock cycles with some modification to the code.

The PRECHARGE All command is issued at the end of a READ or WRITE command, or at the end of a row during a FULL, or in order to terminate a write burst access. The AUTO PRECHARGE command is not used in this design in order to support the consecutive read and write accesses (burst FULL option).

There is one counter in this design to handle auto refresh. The counter (AUTO_REF_CNT) is dedicated to count 15.6 µs and is clocked by a 6.25 MHz clock. An Auto_Refresh flag is set when AUTO_REF_CNT reaches 15.6 µs. If no other commands (READ or WRITE) are being executed when Auto_Refresh flag is set, then an AUTO REFRESH command is executed. An AUTO REFRESH command is only executed after the completion of a READ or WRITE command in progress.

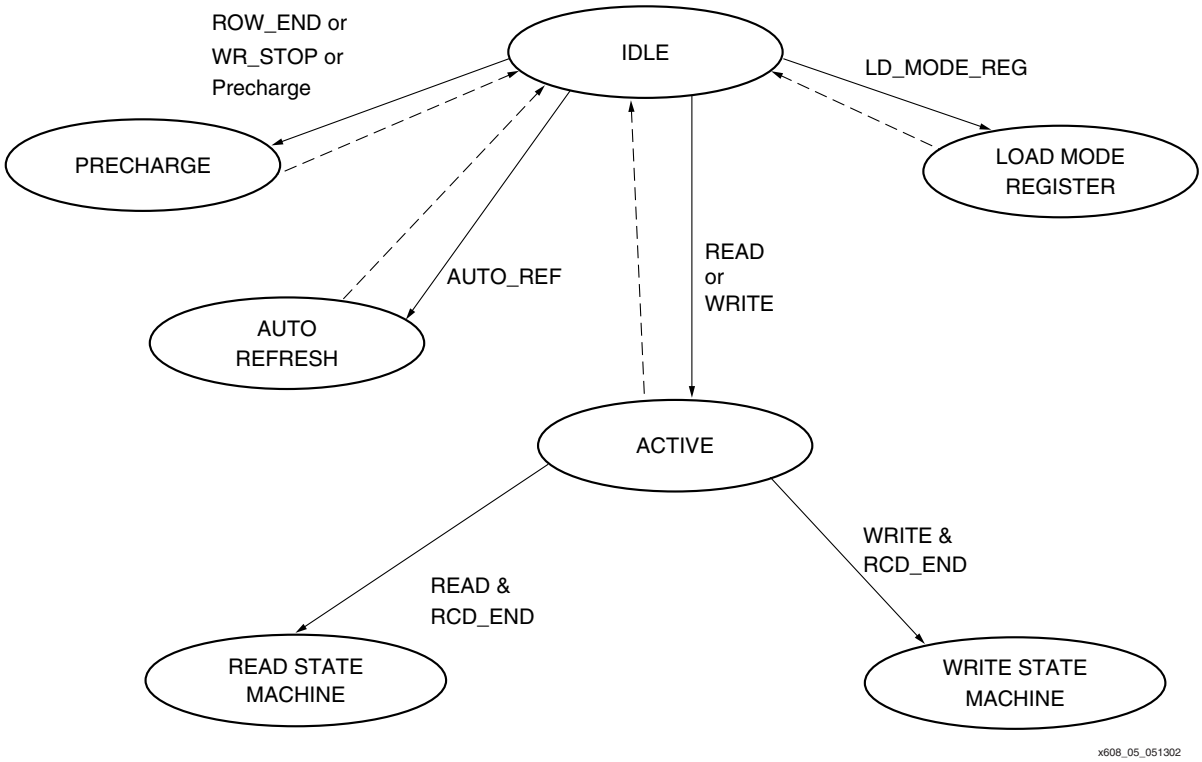

Figure 6: **Main State Machine**

Read State Machine

The details of the read state machine are shown in Figure 7. The three states in this state machine are READ_WAIT/NOP, BURST_READ, and BURST_STOP. On reset, this state machine transitions to the READ_WAIT state. In the BURST_READ state, the READ command is executed. The state machine stays in the BURST_READ state for exactly one 100 MHz clock cycle and subsequently transitions to the READ_WAIT state. As shown in the read waveform in Figure 7, the read data appears on the DQ bus two clock cycles later (CAS latency). During a read access, the DQS is provided by the DDR SDRAM DIMM and is edge aligned with the data. Since DQS is an intermittent signal, it cannot be input to the Digital Clock Manager (DCM) and, hence, cannot be used to clock registers in the FPGA. To capture this data, the memory controller Read Enable (RD_EN) signal transitions High at the first rising edge of clock CAS Latency later. RD_EN stays High for two clock cycles for a burst 2, five clock cycles for a burst 4, and nine clock cycles for a burst 8. The RD_EN signal is Low at all other times. The data is captured on the positive edges of CLK90 and CLK270 (90° and 270° phase shifted versions of the 100 MHz clock) to ensure adequate setup and hold times with respect to the incoming data.

The DDR flip-flops in the Input Output Block (IOB) of the Virtex-II device are used for this purpose.

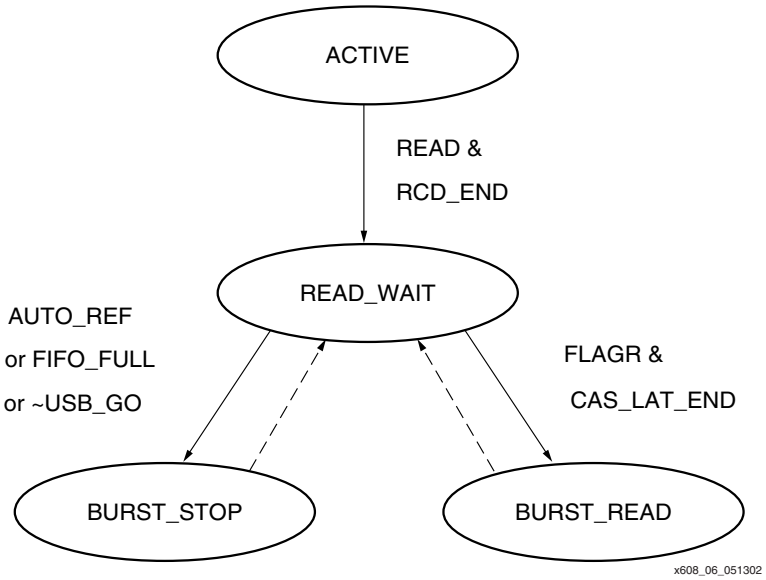

Figure 7: **Read State Machine**

Read Timing

During a READ, the DDR SDRAM DIMM module sends DQS and DQ edge aligned with respect to each other. DQS is in phase with CK, the clock provided to the DDR SDRAM DIMM module, which in turn is in phase with CLK0 (with some finite skew). To capture the read data, a 90° phase shifted clock (CLK90) is used for the input DDR IOB flip-flops to center the clock edge with respect to data. To determine whether the setup time of the input DDR IOB FF is being met, the phase relationship between CK and CLK90 and the data valid window must be computed.

To compute the phase relationship, it is important to note that a DCM in the FPGA provides the clock to the DDR SDRAM DIMM modules. The DCM for the clock used internally in the FPGA and the DCM used to forward the clock to the DDR SDRAM DIMM module have the same input source clock. Therefore, a phase relationship exists between the clock used internally in the FPGA and the clock forwarded to the DDR SDRAM DIMM module.

Figure 8 shows the relationship between CLK90 (used for read data capture) and CK at the DDR SDRAM DIMM. The board trace length of the feedback to the external DCM and the trace length of CK and $\overline{CK}$ from FPGA to DDR SDRAM DIMM must be the same.

The worst case phase relationship is computed by adding CLKIN_CLKFB_PHASE for the external DCM, CLKIN_CLKFB_PHASE for the internal DCM, CLKOUT_PHASE between CLK0 and CLK90, clock tree skew, and clock period jitter. Assume a phase offset between CLKIN (input) and CLKFB (feedback) of –50 ps for the external DCM, and a phase offset between CLKIN (input) and CLKFB (feedback) of +50 ps for the internal DCM, and the phase offset between the DCM outputs of the internal DCM of 140 ps. The clock tree skew is 500 ps and the clock period jitter is ±150 ps.

Worst case phase relationship = (CLKIN_CLKFB_PHASE for External DCM)
+ (CLKIN_CLKFB_PHASE for Internal DCM)
+ (CLKOUT_PHASE between DCM outputs of Internal DCM)
+ clock tree skew + clock period jitter

Worst case phase relationship = 50 ps + 50 ps + 140 ps + 500 ps + 300 ps = 1040 ps

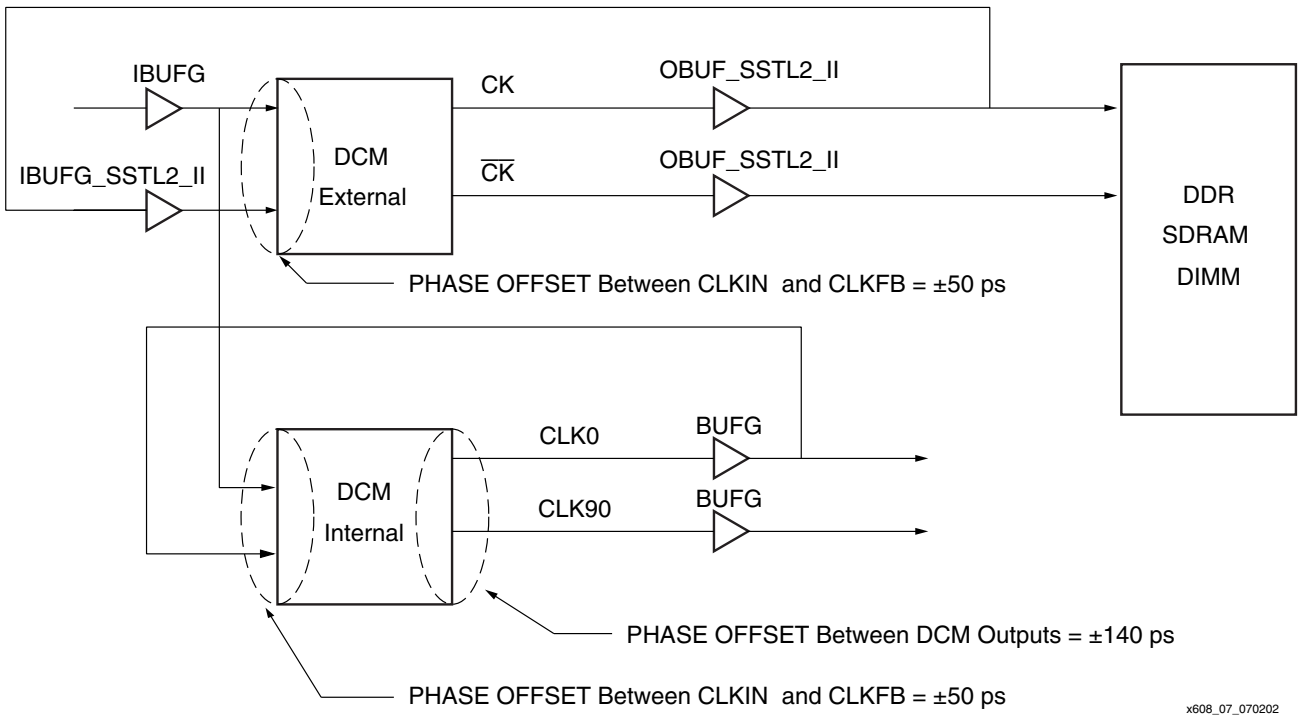

Figure 8: **Clock Skew Between CK at the DDR SDRAM DIMM and CLK90 in FPGA**

The other parameters to be considered to compute the data valid window are the duty cycle distortion, board trace delay (propagation delay of data on the board), package skew, and t_{AC} the access window of data (DQs) from CK/$\overline{CK}$ given by the memory vendor. The duty cycle distortion must be considered since CLK90 and the inverse of CLK90 are used to clock input DDR IOB flip-flops to capture read data and the inverse of CLK90 is generated by inverting CLK90.

Duty cycle distortion = 140 ps

Board trace delay = 600 ps

Package skew = 90 ps

t_{AC} = ±0.8 ns

Data valid window at DIMM = (clock period/2) – t_{AC} = 5 ns – 1.6 ns = 3.4 ns

This data valid window further reduces at the input DDR IOB flip-flops due to board trace delay, phase difference between CK and CLK90, package skew, and duty cycle distortion.

Data valid window at input DDR IOB FF = 3.4 ns – (1.04 ns + 0.14 ns + 0.6 ns + 0.09 ns)

= 1.53 ns

The margin available on the data valid window is very small.

1.53 ns – 0.8 ns [setup (T_{PSDCM}) and hold (T_{PHDCM}) of input DDR IOB flip-flops] = 0.73 ns

To improve the margin, the internal DCM clock outputs were phase shifted by 1 ns to the right. A fixed phase shift factor of 25 for a 100 MHz clock input was used to achieve this phase shift. The 1 ns phase shift compensates for the clock skew between CK and CLK90. The resulting margin is 1.73 ns.

Figure 9 shows the timing details of the read data capture.

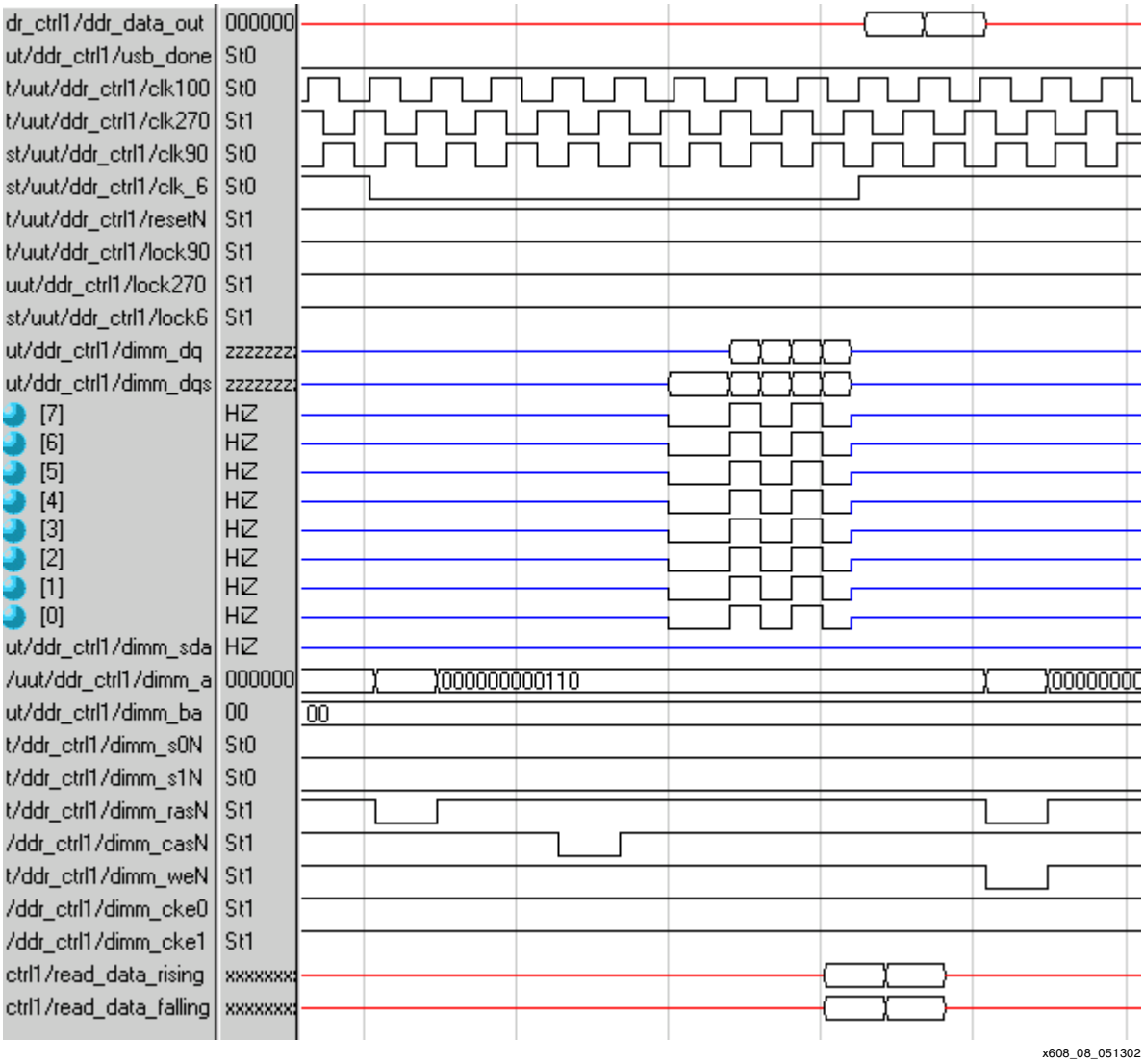

Figure 9: **Read Burst Size 4**

Write State Machine

The details of the Write state machine are shown in Figure 10. The two states are WRITE_WAIT or NOP and BURST_WRITE. On reset, the state machine transitions to the WRITE_WAIT state. There is no Write Terminate state. To terminate a write burst access, a PRECHARGE command has to be executed. In the BURST_WRITE state, the WRITE command is executed. The state machine stays in the BURST_WRITE state for exactly one 100 MHz clock cycle and subsequently transitions to the WRITE_WAIT state.

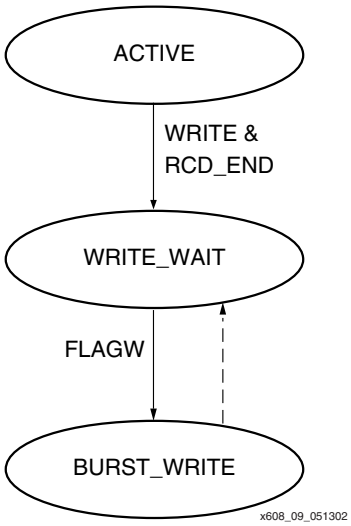

Figure 10: **Write State Machine**

Write Timing

During a WRITE, the DQS signal is output by the DDR SDRAM DIMM memory controller. As shown in the write waveform in Figure 11, DQS must be center aligned with write data to be sent on the DQ bus. DQS is a 100 MHz clock that is provided through a DDR IOB flip-flop clocked by CLK270 and CLK90 only during a write access. Data (DQ) to be written to memory is sent out through the output DDR flip-flops that are being clocked at CLK0 and the inverse of CLK0, thereby, achieving the 90° phase shift required between DQS and data (DQ). The 90° phase shift between DQS and DQ is mostly maintained at the DDR SDRAM DIMM, because the board trace delays for DQS and DQ are matched and both signals have the same clock-to-out through DDR IOB output FFs. The phase difference between DQS and DQ will not be exactly 90° due to the package skew (90 ps) and board trace inaccuracies. The data valid window calculation (at the FPGA) for a WRITE is shown below. The phase relationship parameter is the skew between CK at the DDR SDRAM DIMM and CLK90.

Worst case phase relationship:

= (CLKIN_CLKFB_PHASE for Internal DCM) + (CLKIN_CLKFB_PHASE for External DCM)
+ (CLKOUT_PHASE between DCM outputs of Internal DCM) + clock tree skew + clock period jitter

Worst case phase relationship = 50 ps + 50 ps +140 ps + 500 ps + 300 ps = 1040 ps

Data valid window at FPGA = (clock period/2) – (clock skew + package skew + duty cycle distortion)

Data valid window at FPGA = 5 – (1.04 + 0.09 + 0.14) = 5 – 1.27 = 3.73 ns

This data valid window is further reduced at the DDR SDRAM DIMM due to board trace delay of 600 ps.

Data valid window at DDR SDRAM DIMM = 3.73 – 0.6 = 3.13 ns

The phase shift of 1 ns on the clock outputs from the DCM and the clock-to-out delay of the IOB flip-flops cause the t_{DQSS} to be a nominal of one clock cycle.

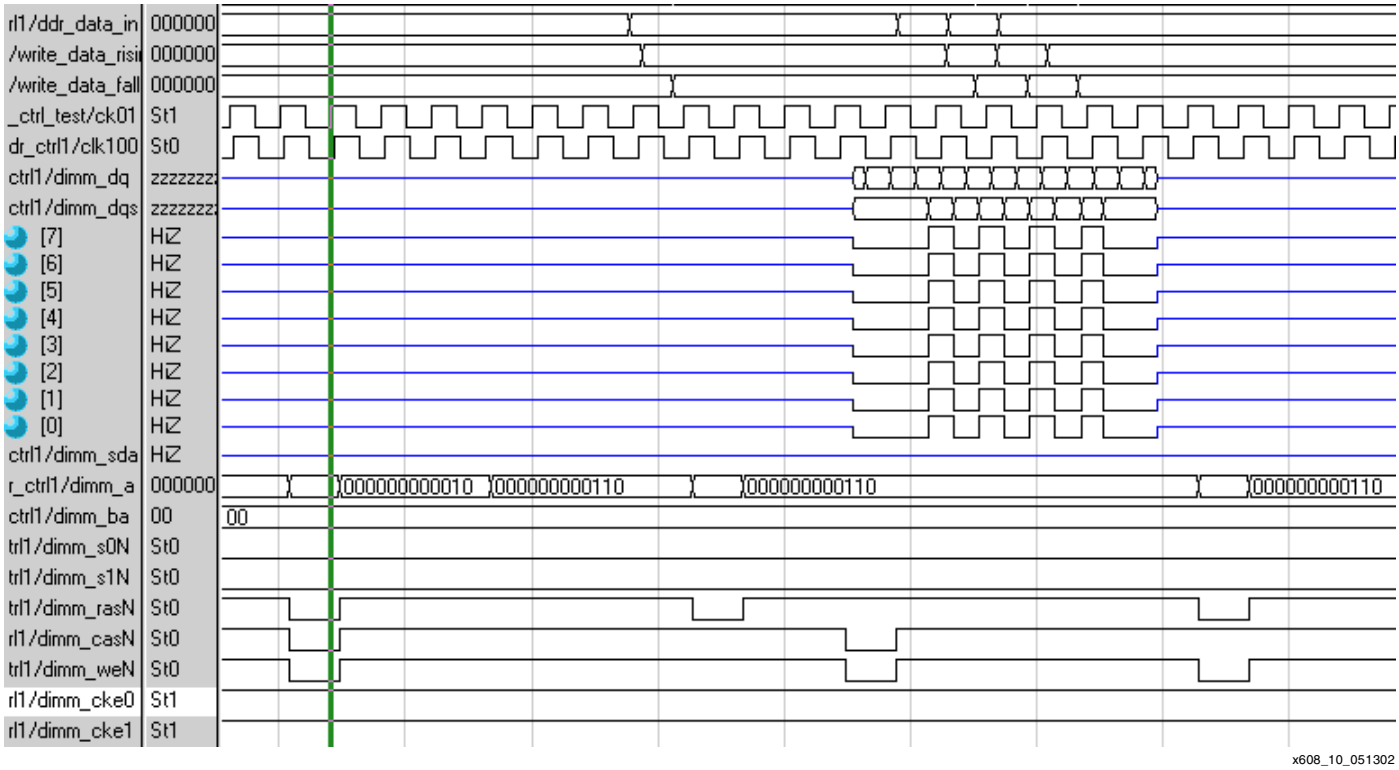

Figure 11: **Write Burst Size 8**

User Interface

The user interface in this application is Cypress USB 2.0. The USB controller sends control signals via a set of six 8-bit registers. Table 2 describes the functions of each register and the details of each bit in the configuration register.

Table 2: **8-Bit DDR SDRAM Register Address**

Register Address (RA)	Register Name	Description	Initial Values
000	CONFIGURATION	[0, 0, cas_lat, init_mem, full, mode2, mode1, read/write]	00000000
001	STATUS	Not used in the current design	00000000
010	START_ADDR_1	LSB 8 bits of starting address	00000000
011	START_ADDR_2	Next 8 bits of starting address	00000000
100	START_ADDR_3	MSB 8 bits of starting address	00000000
101	BURST_COUNT_1	LSB 8 bits of burst count	00000000
110	BURST_COUNT_2	LSB 8 bits of burst count	00000000
111	N/A	N/A	N/A

Configuration

The DDR SDRAM controller uses the Configuration register to set the direction and burst type of a transaction. The read/write bit sets the direction of DDR SDRAM transactions. When asserted, the read/write bit sets the DDR SDRAM controller to write to the DDR SDRAM and reads from the DDR SDRAM when de-asserted. The mode bits set the type of transaction according to the mapping in Table 3.

Table 3: **Mode Bits in the Configuration Register**

Mode 2, Mode 1	DDR SDRAM DIMM Mode
00	Burst 2: 64-bit Words
01	Burst 4: 64-bit Words
10	Burst 8: 64-bit Words
11	Not Used

The full bit is used to indicate that the transaction will be bursting many rows. If full is de-asserted, then the SDRAM controller will only perform one burst transfer. When full is asserted, the DDR SDRAM controller will conduct burst transfers until the burst count is reached. The DDR SDRAM controller uses the init_mem bit to initialize DDR SDRAM DIMM memory 200 µs after power up. The cas_lat bit sets the CAS latency for the DDR SDRAM device. When cas_lat bit is asserted, the CAS latency is set to 2.5 clock cycles (100 MHz) and CAS latency is two clock cycles when de-asserted. There should be a 202 µs delay between power-up and a READ transaction.

Start Address

A total of 24 bits are required to address the DDR SDRAM DIMM. The sum of Bank Address (2 bits), Row Address (12 bits), and Column Address (10 bits) equates to 24 bits. The USB data bus is only 8-bits wide; hence, the need for three Start Address registers as shown in the Table 3 above.

Burst Count

During a full burst, multiple rows can be accessed for read or write. The user needs to specify the number of rows using these registers. The starting column address for full bursts must be either zero or some multiple of eight, because multiple burst 8s are issued during a full burst. The maximum number of rows in the DDR SDRAM DIMM requires 12 bits to be represented; therefore, two 8-bit Burst Count registers are required.

USB Control Signals

The control signals from the USB to the DDR SDRAM controller are usb_go1, usb_strobe, usb_rd, usb_cs1, and usb_ra. All these signals are registered within the DDR SDRAM controller. The usb_done signal is a status from the DDR SDRAM controller to the USB indicating the end of an uninterrupted transaction. The usb_strobe signal is used in conjunction with the 8-bit data bus, usb_d, being input from the USB. When usb_strobe is asserted, data on usb_d is input to the DDR SDRAM controller register addressed by usb_ra independent of the logic level on the usb_go1 signal. When usb_go1 is asserted, the data from the configuration register is read and given to the relevant counters and state machines to start a transaction (READ or WRITE). A READ or WRITE transaction is started by setting the read or write flag. An ACTIVE command is issued on assertion of the flag, followed by a READ or WRITE command.

Also the 64-bit data is registered in the data register depending on the flags status (ddr_full_2, ddr_full_4, ddr_full_8, ddr_ae, ddr_af, ddr_valid, ddr_step) from the data path FIFO. These flags are further explained in the data path section. At the negative edge of usb_go1, the current transaction must be terminated and the DDR SDRAM controller state machine must go to the IDLE state. The usb_done signal will not be asserted if usb_go1 was de-asserted in the

middle of a transaction. Usb_ra is the register address from the USB. Table 2 indicates the register addresses for the different registers in the DDR SDRAM controller (for example, Configuration register [000]). Usb_rd is a read signal enabling the USB to read from the STATUS register.

Data Path

The 64-bit data to and from the DDR SDRAM controller is supplied through a FIFO. The FIFO status flags input to the SDRAM controller are ddr_full_2 (two 64 bits of data in FIFO), ddr_full_4 (four 64 bits of data in FIFO), ddr_full_8 (eight 64 bits of data in FIFO), ddr_ae (Almost Empty), ddr_af (Almost Full), ddr_step, and ddr_valid. The Step (ddr_step) output from the SDRAM controller is used to increment/decrement the write/read pointers in the FIFO.

Table 4 shows the delay parameters for the DDR SDRAM. The turn around time for a Read command between consecutive rows is the sum of the following parameters: $t_{RP} + t_{RCD} + CL$ (2 or 2.5 clock cycles for 100 MHz). The turn around time for a write operation between consecutive rows is the sum of the following parameters: $t_{RP} + t_{RCD} + t_{DQSS}$ (5 clock cycles for 100 MHz nominal case).

Table 4: **DDR SDRAM Delay Parameters**

Parameter	Symbol	-262/-265 (Speed Grade)	Units
Precharge Command Period	t_{RP}	20 (Min)	ns
Active to Read/Write Delay ($\overline{RAS}$ to $\overline{CAS}$)	t_{RCD}	20 (Min)	ns
CAS Latency	CL	2.0 or 2.5	Clock Cycles (100 MHz)
Read to Precharge Command	RDP	1 for burst 2 2 for burst 4 4 for burst 8	Clock Cycles (100 MHz)
Active to Precharge Command	t_{RAS}	45 (Min)	ns
Active Bank A to Active Bank B Command	t_{RRD}	15 (Min)	ns
Write Command to First DQS Latching Transition	t_{DQSS}	0.75 (Min) 1.0 (Nom) 1.25 (Max)	Times Clock Period
Auto Refresh Command Period	t_{RFC}	75	ns
Refresh to Refresh Command Interval	t_{REFC}	15.6	µs

The 64-bit data to be written to the DDR DIMM is provided through a shift register and a FIFO. The user data is 16-bits wide and its frequency is 100 MHz. The shift register constructs a 128-bit memory data with eight 16-bit wide user data and sends it into the FIFO at 100 MHz. Data from the FIFO is registered in the controller at 100 MHz and then sent out to DDR DIMM through DDR IOB flip-flops. The controller starts reading from the FIFO only when usb_go1 is asserted, ddr_valid signal is asserted (indicating valid data in the FIFO), and the FIFO has the required number of 64-bit data. For example, two 64-bit data for a burst 2, four 64-bit data for burst 4, eight 64 bit data for burst 8, and ddr_af is asserted for burst full. The full status of the FIFO is provided to the controller via the full2 (ddr_full_2), full4 (ddr_full_4), full8 (ddr_full_8), and almost full (ddr_af) flags. The controller sends a Step (ddr_step) signal to the FIFO in order to increment its read pointer. The ddr_step signal is asserted for one clock cycle for a burst 2, two clock cycles for burst 4, four clock cycles for burst 8, and four clock cycles for full bursts, since a full burst is a series of burst 8s. The write data is center aligned with respect to DQS signal. The first positive edge of the DQS signal appears 3/4 of a clock cycle after the WRITE

command was issued. However, the delay t_{DQSS} is a nominal value of one clock cycle at the DDR SDRAM DIMM due to clock-to-out of DDR IOB flip-flop and the board trace delay.

The 64-bit data being read from the DDR SDRAM DIMM is registered at input DDR flip-flops (clocked at 100 MHz) in the IOB. Valid read data is available on the DQ bus two 100 MHz clock cycles (CAS latency) after READ command was issued. This data is edge aligned with DQS. Read data is captured using read enable signal in the IOB input DDR flip-flops. The FIFO flags, ddr_af and ddr_ae must be checked before read data is written to the FIFO. The ddr_ae (almost empty) flag must be asserted before the FIFO can be written to and data can only be written to FIFO until the ddr_af flag is asserted. The write pointer of the FIFO into which this data is written to increments using the Step (ddr_step) signal. The ddr_step signal is asserted for one clock cycle for a burst 2; two clock cycles for burst 4; four clock cycles for burst 8, and four clock cycles for full bursts, since a full burst is a series of burst 8s.

Implementation and Performance

This design targets an XC2V6000 -5, FF1152 package. Two DCMs are required, one for clocking the logic inside the FPGA and the other to provide the clock externally to the DDR SDRAM DIMM. Both the DCMs receive the same system clock input of 100 MHz. The DCM for external clocking requires an external feedback and the outputs being used are the CLK0 (clock) and CLK180 (inverted clock). This design uses four outputs of the DCM providing clocks for internal logic. The four outputs are CLK0 (100 MHz clock), CLK90 (90° phase shifted version of the 100 MHz clock), CLK270 (270° phase shifted version of the 100 MHz clock) and CLKDV (100 MHz/16 = 6.25 MHz clock). The 6.25 MHz clock is for the auto-refresh counter.

The performance of this controller (100 MHz) is limited by the set-up time window for this system synchronous design. The digital phase shift factor was computed based on the board trace delay for this system. The phase shift was essential to meet the setup time requirement for the IOB DDR flip-flop during a READ command. See Table 5.

Table 5: **Performance and Utilization**

Location Constrained IOBs	Slices	BUFMUXs	DCMs	Performance
110	645	4	2	100 MHz

Notes:

1. The user interface signals and data path signals (e.g., the FIFO control and status) are not added to the number of IOBs. These signals are not external inputs/outputs in a real system.

Conclusion

This design was implemented as part of a larger system and the features of the DDR SDRAM DIMM best suited for this system application were selected and implemented. For example, a CAS Latency of 2 is fixed and the auto-precharge option is not being used since consecutive read and write commands are crucial to this application.

The DDR flip-flops in the IOB of Virtex-II devices are being used both for the data as well as the DQS during a WRITE command.

Note that this design provides little setup time and data valid window margin during a read data capture. Therefore, this design should only be used for performances up to 100 MHz. Beyond 100 MHz, the method using local clock routing for DQS is recommended as shown in **XAPP266** and **XAPP253**.

Reference Design Files

The VHDL and Verilog reference design files are posted on the Xilinx FTP site.

ftp://ftp.xilinx.com/pub/applications/xapp/xapp608.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/02/02	1.0	Xilinx Initial Release
11/05/02	1.1	Revised Read and Write Timing sections.
01/15/03	1.2	More revisions to Read and Write Timing sections.