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SONET Rate Conversion in Virtex-II Pro Devices

Author: Nick Sawyer and Francesco Contu

Summary

This application note targets Virtex-II Pro™ designs where there is a requirement to directly use the Rocket I/O™ transceivers in 16-bit mode. Use this reference design when 8b/10b data encoding is not required and the output frequency needs to be 16 times the system frequency. This design has been successfully simulated and an update will be available when actually implemented in Virtex-II Pro silicon.

Introduction

The Rocket I/O transceivers have several modes of operation, but all modes rely on the internal transmitter clock being multiplied by 20 for data transmission. For example, a 20-bit data stream passed to the unit at 125 MHz is serialized and retransmitted at 2.5 Gb/s. At a 156.25 MHz input, the output is at its maximum speed of 3.125 Gb/s. The parallel data stream applied to the Rocket I/O transceiver can either be 20 bits direct, or it can be written as 16 bits, to which 8b/10b coding is applied to generate the 20 bits required.

However, there is a class of applications, typically in SONET processing systems, where the data path is 16 bits wide, running at 155.52 MHz. The designer would ideally apply the data directly to the Rocket I/O transceiver for onward transmission at 155.52 x 16 = 2.48832 Gb/s. Since this can not be done in Virtex-II Pro devices, this application note describes the logic necessary to perform this function.

This application note is divided into two sections, the first is the logic necessary for the data width conversion, and the second describes the clocking characteristics required by the Rocket I/O transceiver.

Logic Description

The logic required for the rate converter is very simple. The input from the system to the transmitter logic (Figure 1 and Figure 2) is 16-bits wide, running at typically 155.52 MHz. The output to the Rocket I/O transceiver is 20-bits wide and typically running at 124.416 MHz. The absolute frequencies can be varied, but the ratio is fixed at 5:4. Sonet systems transmit data with the most-significant bit (MSB) first. Since the Rocket I/O transceiver also uses this bit ordering, no bit, byte, or word swapping is necessary.

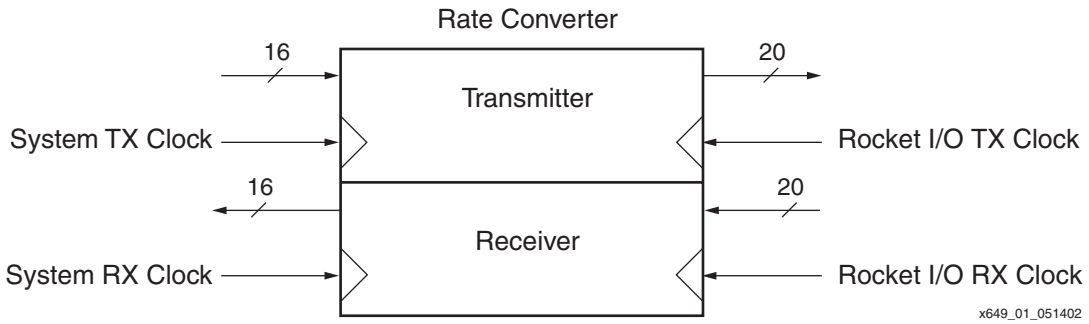

Figure 1: **Rate Converter Logic Block Diagram**

The reverse path is very similar as 20-bit wide data at 124.416 MHz arrives from the Rocket I/O transceiver and is converted by the receiver logic into 16-bit wide data at 155.52 MHz for forwarding into the system.

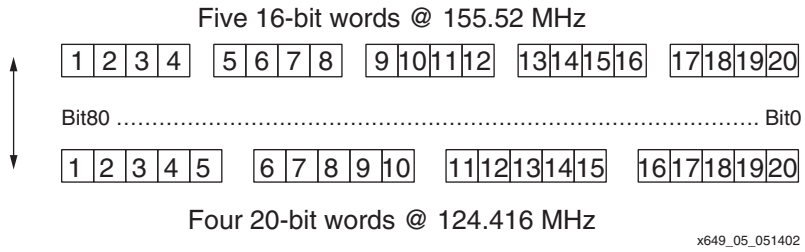

Figure 2: **Data Rate/Width Conversion**

Transmitter

This unit consists of an 80-bit register and two counters. Following a reset, the first 16 bits of data to arrive from the system are written into registers 15 down to 0; the second word is written into registers 31 down to 16, and so on. The sixth word received is again written into registers 15 down to 0. Each time a word is written, a write counter increments by one, synchronous to the system clock, and is programmed to count from 0 to 4 before repeating. When the write counter reaches the value 001 or 010, the read counter is enabled. Two possible values are required as the Rocket I/O transceiver and system clocks are totally asynchronous. Data is first read 20 bits wide from registers 19 down to 0, then from registers 39 down to 20, and so on. After four reads, it returns to registers 19 down to 0. The read counter counts from 0 to 3 synchronous to the Rocket I/O transceiver clock, and is used to control the data output multiplexer. The circuit is now synchronized and will continue operating as described.

Receiver

This unit also consists of an 80-bit register and two counters. Following a reset, the first 20 bits of data to arrive from the Rocket I/O transceiver are written into registers 19 down to 0; the second word is written into registers 39 down to 20, and so on. The fifth word received is again written into registers 19 down to 0. Each time a word is written, a write counter increments by one, synchronous to the Rocket I/O transceiver clock, and is programmed to count from 0 to 3 before repeating. When the write counter reaches the value `001` or `010`, the read counter is enabled. Two possible values are required as the Rocket I/O transceiver and system clocks are totally asynchronous. Data is first read 16 bits wide from registers 15 down to 0, then from registers 31 down to 16, and so on. After five reads, it returns to registers 15 down to 0. The read counter counts from 0 to 4, synchronous to the system clock, and is used to control the data output multiplexer. The circuit is now synchronized and will continue operating as described.

Clock Considerations

For the circuit to work correctly, the Rocket I/O transceiver clock needs to be exactly 0.8 times the system clock. This is easily achieved using the frequency synthesizer module (DFS) in the Virtex-II Pro Digital Clock Manager unit (DCM). However, the jitter added by the DFS will be more than is required for the Rocket I/O transceiver REFCLK input to work properly. In order to generate a clock with the right jitter number (max 40 ps, peak-to-peak), it is necessary to use an external component. Two possible solutions are proposed.

PLL Based Clock Generator

Figure 3 shows the solution using an external monolithic PLL. A possible device is ICS8430-11 (see **www.icst.com** for details). Because this is a fully integrated device, no external components are necessary to generate the clock. It has a maximum output jitter of 30 ps.

The SONET clock (155.52 MHz) is divided by 10 inside the Virtex-II Pro FPGA, to obtain a frequency (15.552 MHz) that can be accepted by the external PLL. This divided clock is then multiplied by 8 by the PLL resulting in the desired 124.416 MHz clock.

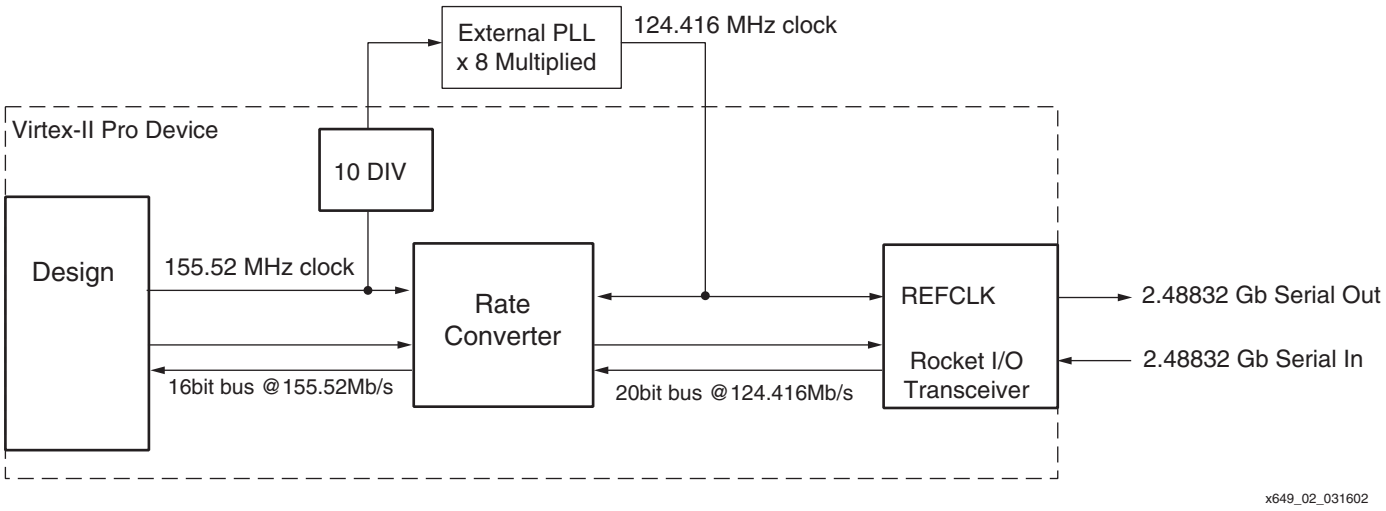

Figure 3: **PLL Based Clock Generation**

VCXO Based Clock Generator

Figure 4 shows the solution using an external VCXO. The VCXO is a custom component available from several different vendors. Champion Technologies has already implemented a device with a maximum output jitter of 15 ps (www.champtech.com).

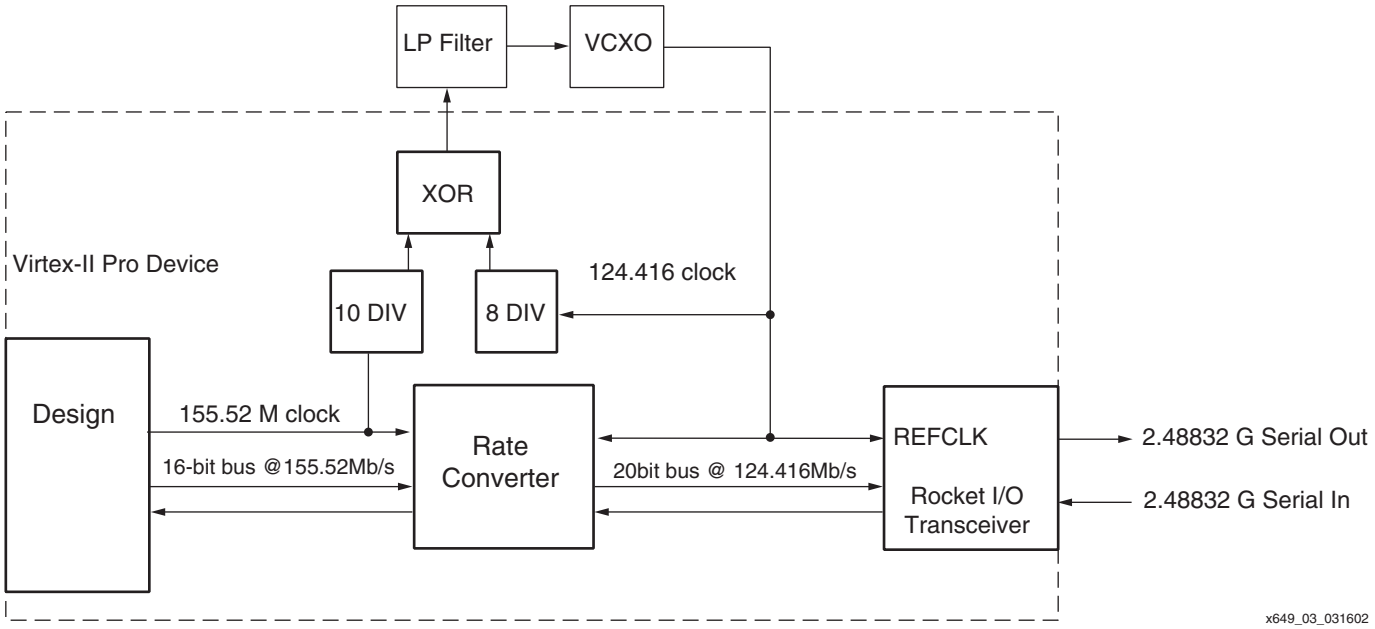

Figure 4: **VCXO Based Clock Generation**

Using this VCXO, a classic PLL circuit can be realized. The SONET clock (155.52 MHz) is divided by 10 internally in the Virtex-II Pro FPGA, while the VCXO generated clock (the desired 124.416 MHz) is divided by 8. Both these dividers should generate a frequency of 15.552 MHz. These two divided clocks are used to feed a phase comparator, implemented by a simple XOR gate. The XOR output feeds an external low-pass filter (a simple RC circuit) generating the control voltage for the VCXO. A clock generated by the VCXO is exactly 80% of the SONET system clock frequency.

Reference Design

The reference design files described in this application note are written in both Verilog and VHDL and are available from the Xilinx FTP site (**xapp649.zip**).

The best way to implement the design is to connect the rate converter to a Rocket I/O CUSTOM_GT primitive configured in 2-byte mode (shown in Figure 5). For full details consult the **Rocket I/O Transceiver User Guide**.

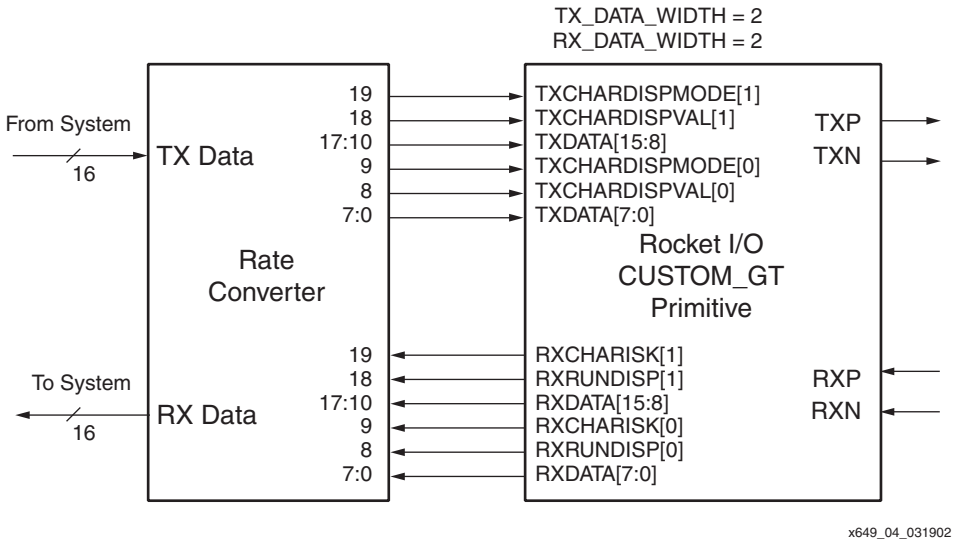

Figure 5: **Using the Rate Converter with the 20-bit Rocket I/O Transceiver**

Conclusion

Virtex-II Pro Rocket I/O transceivers can be used directly in SONET systems for board-to-board and chip-to-chip connections, processing 16-bit wide data with the addition of the logic and clocking schemes described in this application note.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/18/02	1.0	Initial Xilinx release.
05/14/02	1.1	Changed name of application note, updated Figure 1.