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SONET and OTN Scramblers/Descramblers

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Summary

This application note examines the design of scramblers for use with Synchronous Optical NETworks (SONET) and Optical Transport Unit (OTN) designs using the Virtex™ series of FPGAs. The scrambler function for Synchronous Digital Hierarchy (SDH) is the same as that for SONET.

Introduction

Both SONET and OTN are standards for data transmission over fibre optic links. This implies a need for clock recovery at the receiver, which in turn requires a guaranteed minimum number of transitions in the incoming serial data stream. The mechanism to achieve this transition density, similar for both SONET and OTN, is known as scrambling. The scrambling (and descrambling) function is independent of the serial data rate used.

Serial data for transmission is added to the output of a pseudo-random number generator, running at the same clock frequency. The same circuit is used in the receiver to recover the original data transmitted. Obviously, the pseudo-random number generators at each end of the link must be in phase. This is achieved using a known pattern of framing information (which is actually transmitted unscrambled). This is covered in more detail in **XAPP652**.

Circuit Description

The scrambler polynomial for SONET is 7 bits, and so repeats every $2^n - 1 = 127$ clock cycles (see Figure 1). The polynomial for OTN is 16 bits (repeats every 65,535 cycles) and is shown in Figure 2. Note that the scrambler polynomial does not depend on the serial data. It is reset to a known value "1111111" or "1111111111111111" on the most significant bit of the first byte transmitted following the framing sequence transmission. The initialization of the scrambler is performed using the signal INIT as shown in the timing diagram Figure 3.

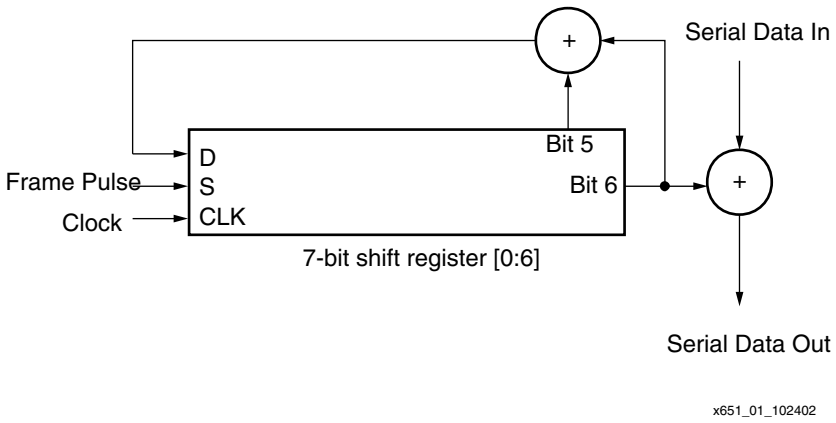

Figure 1: **SONET Scrambler/Descrambler**

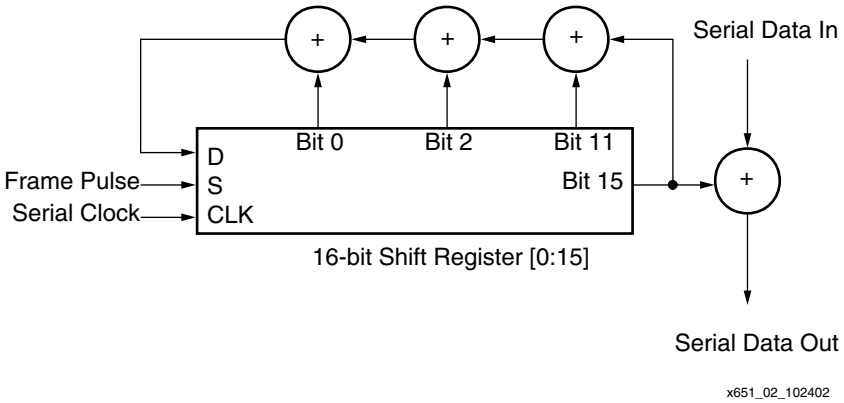

Figure 2: **OTN Scrambler/Descrambler**

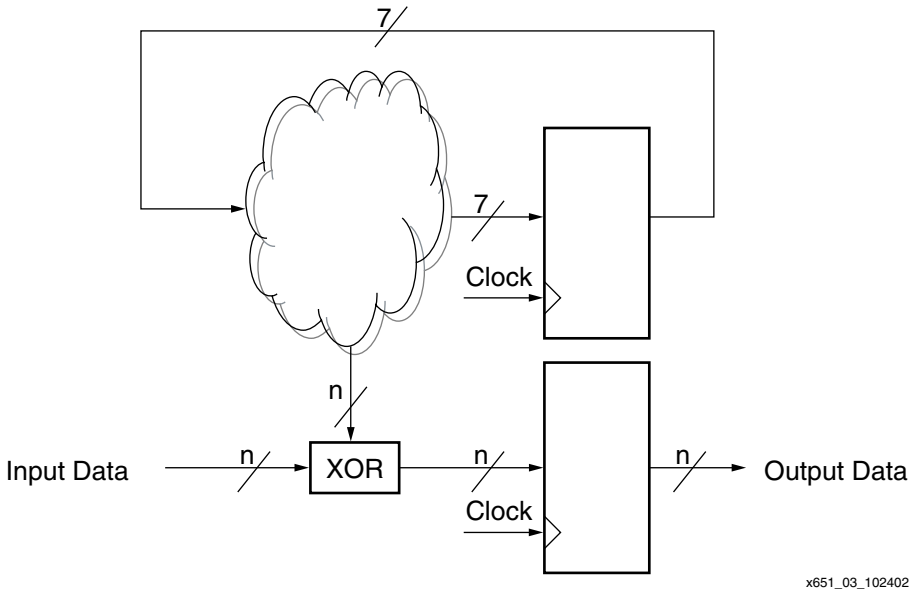

Figure 3: **Logic Mechanism to Generate Scrambled *n*-bit Wide SONET Data**

Both Figure 1 and Figure 2 represent the modification done on a serial bitstream, but typically the design is processing words of data per clock cycle. For instance, SONET OC48 (2.48 Gb/s) can be processed 16 bits wide at 155 MHz, and OC192 (10 Gb/s) can be processed 64 bits wide at 155 MHz, or 128 bits wide at 78 MHz. The scrambler/descrambler circuit, therefore, needs to perform the polynomial multiple times (*n* times for *n*-bit wide data) in one clock period. For SONET scrambling, this is shown in Figure 4. For OTN, the algorithm needs to generate the same *n* bits of output data, but the feedback register is 16 bits, not 7, as the OTN algorithm is a 16-bit shift register.

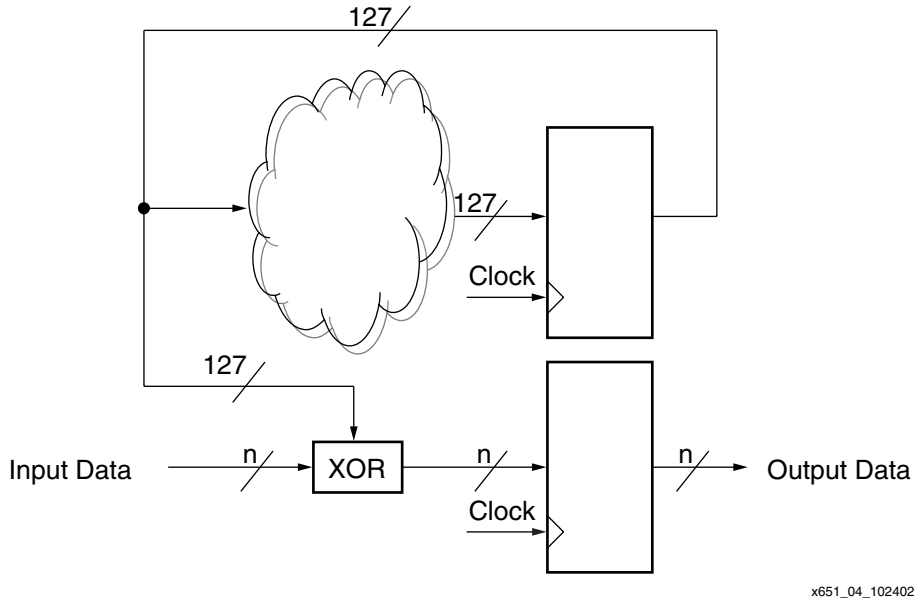

Figure 4: **Shifter Mechanism to Generate Scrambled *n*-bit Wide SONET Data**

This mechanism for implementing an *n*-bit algorithm works well for *n* = 8-, 16-, 32-, and 64-bit SONET data. However, for 128-bit wide and above SONET data, the fact that the entire scrambler shift sequence is only 127 bits can be used to advantage. This sequence can be used to initialize a 127-bit shifter, which is then shifted backwards one position for 128-bit data, twice for 256-bit data, and so on. The tradeoff is that there are extra flip-flops, but less levels of logic and, hence, more speed (see Figure 5). This method is not applicable to OTN data, as the scrambler length is 65,535 cycles, an excessive number of flip-flops.

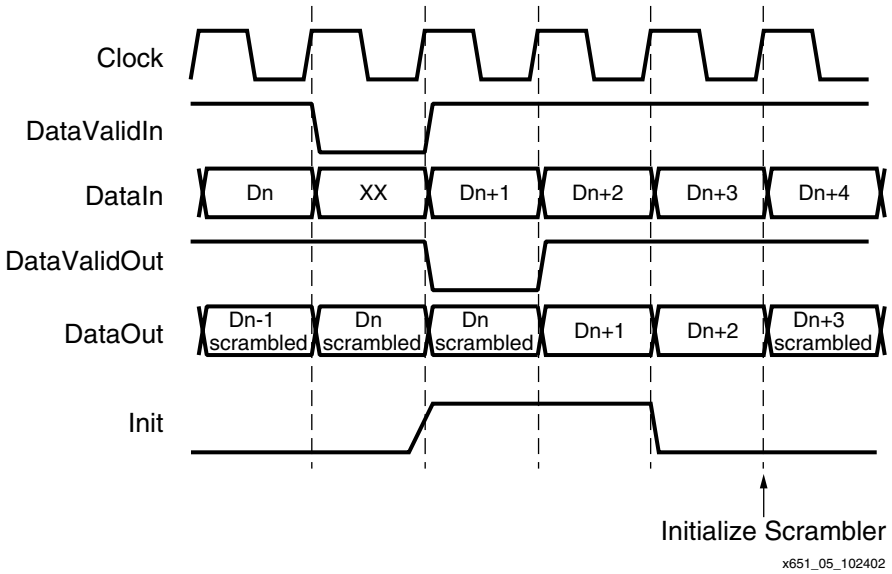

Figure 5: **Data Flow Timing Diagram**

Performance

Clock speed and logic size depend on the data width being used. Below are some examples of what can be achieved using a Virtex-II -5 speed grade device.

Table 1: **Performance Examples**

Data Path	Flip-Flops	Look-Up Tables	Clock MHz	Bandwidth
8-bit SONET	16	15	>400	>3.2 Gb/s
16-bit SONET	24	25	>360	>5.7 Gb/s
32-bit SONET	40	50	>360	>11.5 Gb/s
64-bit SONET	72	87	>320	>20 Gb/s
128-bit SONET	256	261	>320	>40 Gb/s
256-bit SONET	384	391	>320	>80 Gb/s
512-bit SONET	640	653	>320(1)	>160 Gb/s
8-bit OTN	25	35	>350	>2.8 Gb/s
16-bit OTN	34	56	>175	>2.8 Gb/s
32-bit OTN	55	124	>85	>2.7 Gb/s

Notes:
1. Requires a -6 speed grade.

The timing diagram for the data flow is very simple for all mechanisms and is shown in Figure 3. A clock enable input and output are provided for systems where data has been buffered using a FIFO. That is, the processing is not using a clock synchronous to the line rate. If this is not needed, the DATAVALIDIN is always High. The INIT signal is used to initialize the scrambler as described above, and in addition, when this signal is High, the current data word is forwarded unscrambled.

Design Files

The design files described for the various cases above are written for all Virtex and Virtex-II family devices and are available in both Verilog 2001 and VHDL from the Xilinx web site (**xapp651.zip**). See the enclosed **readme.txt** file for latest details.

Conclusion

Scrambling and descrambling logic for data links up to 160 Gb/s can easily be implemented using very little logic resources in the Virtex and Virtex-II family devices.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/08/02	1.0	Initial Xilinx Release
11/15/02	1.1	Updated OTU in title to OTN.