XAPP653 (v1.2) April 14, 2003

Virtex-II Pro and Spartan-3 3.3V PCI Reference Design

Summary

This application note describes the 3.3V PCI solution for the Virtex-II Pro™ and Spartan-3™ FPGA families.

Virtex-II Pro and Spartan-3 Basic Requirements for PCI Designs

The 3.3V regulator reference design described in this application note is verified to work with the Virtex-II Pro I/O pins operating in their 3.3V PCI I/O standard. The **Virtex-II Pro User Guide** has further details on Virtex-II Pro devices and the PCI standard. This same reference design supports the Spartan-3 FPGA, since the Virtex-II Pro I/O structures are similar.

Overview

The reference design offers a number of features including full electrical compliance to the PCI standard for Virtex-II Pro and Spartan-3 designs. This low cost solution uses minimal PC board space. This proven easy-to-use design is shown in Figure 1.

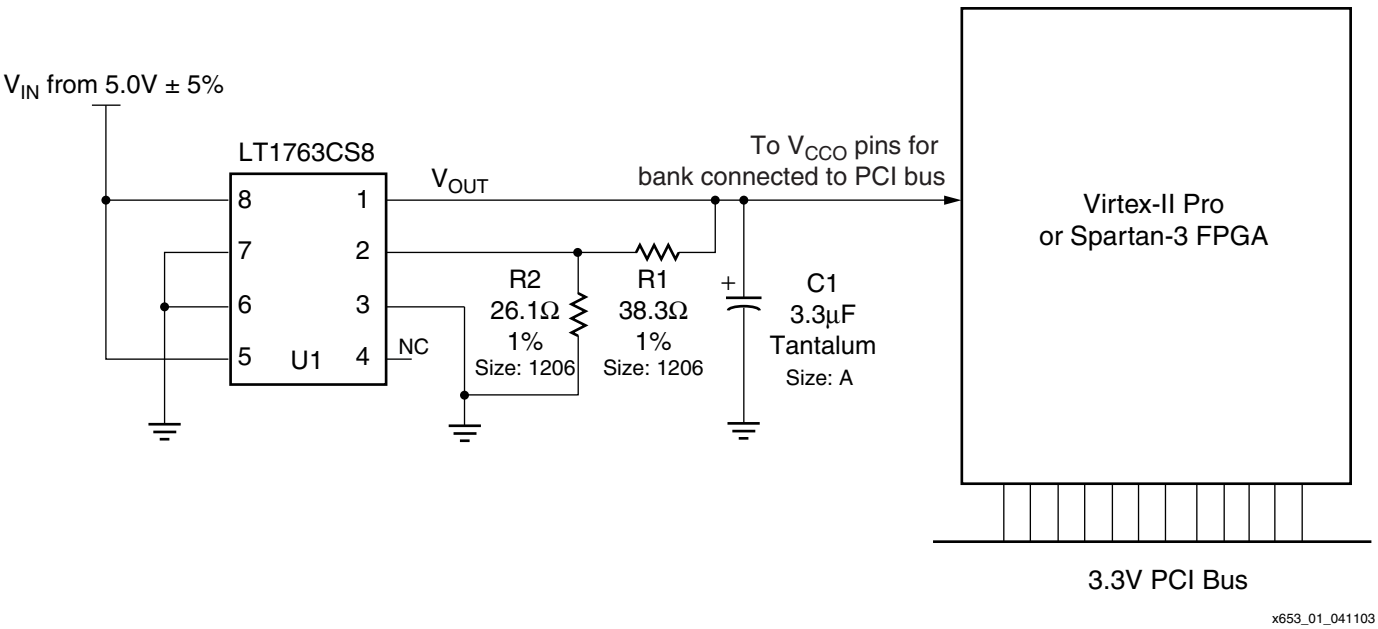

Figure 1: **Reference Design Schematic**

PCI Compliance

The minimum input voltage allowed by the PCI bus specification is –0.5V. Although the absolute maximum specification for Virtex-II Pro input (V_{IN}) is –0.3V when V_{CCO} is at 3.45V, this lower limit is changed from –0.3V to –0.5V when V_{CCO} is lowered to 3.0V.

The signal level below –0.5V is clamped by the intrinsic diode in the I/O. The PCI compliance specification requires the clamp diode to withstand a –3.5V input voltage for more than 11 ns in an undershoot test. In this scenario, the voltage across the clamp diode could be as high as –0.9V. However, the diode passes this undershoot test without concern.

Regulator Implementation

The highlighted elements in Figure 2 (U1, R1, R2, and C1) comprise the regulator implementation on a typical FPGA PCB layout. This configuration supplies a V_{OUT} tightly regulated at 3.0V for the 3.3V PCI V_{CCO} banks. The LT1763CS8 regulator covers an industrial operating temperature range, since the regulator has a junction temperature range of –40°C to +125°C. The reference design provides a fully compliant PCI electrical interface for Virtex-II Pro and Spartan-3 devices. Depending on PCI performance requirements, use the PCI33 or PCI66 I/O standard for the I/Os connecting to the PCI bus. The user is cautioned to not substitute alternative solutions. Alternative designs should be analyzed at Xilinx by the Hotline (by opening a web case at www.support.xilinx.com) or with documented concurrence by a local Xilinx FAE.

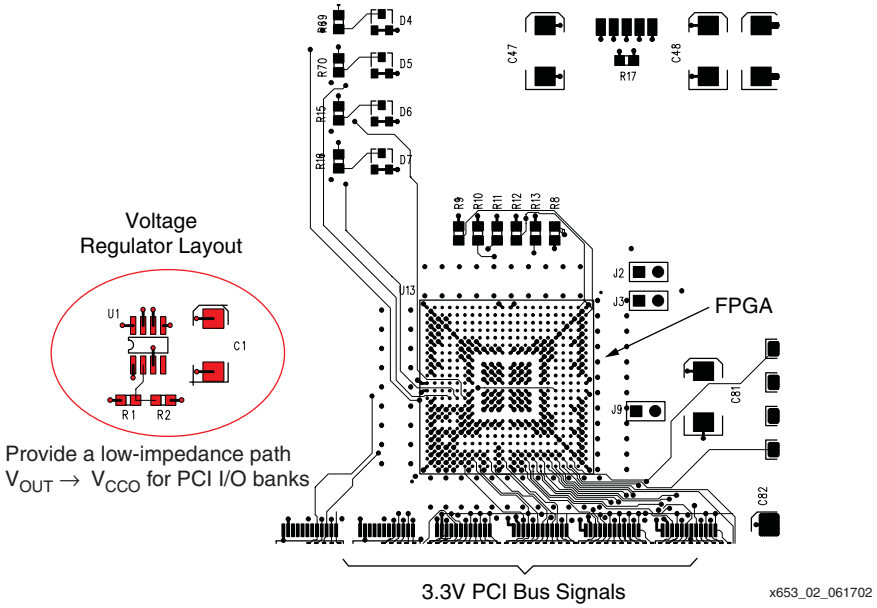

Figure 2: **Layout Area Example**

Linear Technology - LT1763CS8 Devices

Linear Technology manufactures the low noise, low dropout, micropower LT1763 series of regulators. These devices are capable of supplying 500 mA of output current with a dropout voltage of 300mV. Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting, and reverse current protection. The LT1763CS8 regulator used in this application is an adjustable device with a 1.22V reference voltage. Refer to the following URL for more details. http://www.linear.com/prod/datasheet.html?datasheet=520

Solution Cost

The total cost of the solution shown in Figure 1 is estimated to be less than $2.00 in 1000 piece quantities. This estimate includes the LT1763CS8 regulator, resistors, and 3.3µF capacitor.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/17/02	1.0	Initial Xilinx release.
02/06/03	1.1	Added **PCI Compliance** section. Added I/O standard suggestions for connecting to PCI bus.
04/14/03	1.2	Added references to Spartan-3 FPGA family.