Xilinx Global Services
Finish Faster

Training Path for ASIC Designers

Knowledge at Your Fingertips

Xilinx Education Services has expanded the curriculum path for the ASIC designer. The expanded curriculum path now includes four ***New*** recorded e-Learning technical lectures.

These four lectures are on the Xilinx Education home page, Xilinx.com/education. Anyone can access these modules 24 hours a day, 7 days a week. There is no charge for viewing these modules.

ASIC Curriculum Path

Introduction to VHDL or Introduction to Verilog
(3-day course)

↓

New
FPGA and ASIC Technology Comparison (Recorded e-Learning)
&
FPGA Versus ASIC Design Flow (Recorded e-Learning)
&
ASIC to FPGA Coding Conversion (Recorded e-Learning)

↓

New
Spartan-3 Architecture Overview (Recorded e-Learning)

↓

Fundamentals of FPGA Design
(1-day course)

↓

Designing for Performance
(2-day course)

↓

Advanced FPGA Implementation*
(2-day course)

For registration details and access to the Technical Lectures visit the Xilinx Education web site.
http://www.support.xilinx.com/support/training/north-america-home-page.htm

Overview of Four Lectures for the ASIC User

Module 1: FPGA and ASIC Technology Comparison

Objectives

- Describe differences between ASIC and FPGA architectures and describe how these differences affect coding style, implementation, and product selection
  - Gate conversion
  - Delays
  - Frequency comparison
- Discuss reconfigurability

Associated Lab: Pipelining Lab

- Implement and analyze timing for an HDL-coded multiplier
- Implement and analyze a Coregen multiplier core

Module 2: FPGA Versus FPGA Design Flow

Objectives

- Describe key differences between the ASIC and FPGA design flows
  - Design methodology
  - Verification techniques
  - Test generation logic
  - Tools

Associated Lab: NONE

Module 3: ASIC to FPGA Coding Conversion

Objectives

- Optimize ASIC code for implementation in Xilinx FPGAs
  - Xilinx special resources
  - Xilinx combinatorial resources
  - Xilinx synchronous resources
  - Intellectual Property (IP)
- Describe the steps to perform ASIC-to-FPGA code conversion

Associated Lab:

- Describe how improper multiplexer coding can generate slow and unreliable circuits
- Write code to implement a multiplexer implemented with 3-state buffers
- Describe why certain multiplexer styles are faster and more area-efficient

Lab Exercises:

Two self-paced labs, or tutorials, that complement two of the ASIC lectures will be provided. Both labs will be downloadable and printable.

Module 4: "Spartan-3 Architecture Overview" e-Learning Module

This technical lecture focuses on the following topics:

- Spartan -3 architecture features and a comparison of Spartan-3 architecture to existing Xilinx FPGA families
- Product family overview (product matrix)
  - Software support and Prom Support