Xilinx Global Services
Finish Faster

Xilinx Education Services Course:
Advanced FPGA Implementation

The Advanced FPGA Implementation course deliver the knowledge and practice you need to optimize the ISE 5 tool suite in your design.

If you have a burning desire to obtain the best possible performance from your Xilinx FPGAs, you need to know the ISE 5 design suite inside and out. You must master the smallest details of the Xilinx architecture and have every possible design technique at your disposal. But taming tough timing problems and fully appreciating the art of placing macros are skills you won't learn on your own without falling into design traps.

Proactive floorplanning, expert I/O placement, and improving on the software tools' place-and-route algorithms can push a design from very good to excellent. The quickest, safest route to high-performance designs is a saturation course from Xilinx experts. Spark a design revolution in your head.

Hands-on Instruction – Enhancing Productivity and Performance

Human Design Intelligence Goes Beyond Tools

Advanced FPGA Implementation is the perfect course for designers who are ready to tackle the most sophisticated aspects of the ISE 5 tool suite. This two-day course provides plenty of hands-on experience. You will learn how to:

- **Increase Efficiency and Increase Performance –** Six labs cover advanced design topics, from timing analysis/control using scripting, to creating your own Relationally Placed Macro (RPMs), to floorplanning and incremental design. The course also expands your tool knowledge beyond ISE 5 to Synplicity's Synplify™ and Mentor Graphics' Leonardo Spectrum.™
- **Reduce Your Development Costs –** You will improve your time-to-knowledge on the advanced capabilities of our design tools, minimizing your development cycle and design risks.

The last in a three-part course sequence that includes Fundamentals of FPGA Design and Designing for Performance, the *Advanced FPGA Implementation* course builds on the previous two courses, as prerequisites. The course helps you:

- Take advantage of Xilinx scripting tools.
- Create and edit constraints for hand-placing logic and creating timing constraints.
- Build RPMs to improve performance on critical paths.
- Reduce run time with incremental design techniques.
- Use floorplanning tools to create effective layouts and cut place-and-route run times.
- Learn more about I/O layout, high-speed I/O, and clock design so you can take advantage of the Xilinx architectures.
- Optimize post place-and-route design in the FPGA Editor for more efficient in-circuit testing.

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Level – Advanced

Course Duration – 2 days

Price – $1000 USD or 10 Training Credits

Who Should Attend? – Customers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Prerequisites

- Xilinx Fundamentals of FPGA Design course
- Xilinx Designing for Performance course
- Intermediate knowledge of VHDL or Verilog strongly recommended
- Six months, or more, of design experience with Xilinx tools and FPGAs

Software Tools:

- ISE 5
- Mentor Leonardo Spectrum
- Synplicity Synplify

Course Outline

NOTE: Target Architecture includes both Virtex™-and Spartan™-series FPGAs

Introduction
Lab 1: Timing Analyzer, Constraints, and Closure
Command Line Implementation
UCF Editing
Lab 2: UCF and Scripting
Creating Your Own Relationally Placed Macros (RPM)
Lab 3: RPM
FPGA Editor: Viewing and Editing a Routed Design
Lab 4: FPGA Editor
Incremental Design Techniques
Floorplanner: Effective Layout
Lab 5: Floorplanner and Incremental Design
Advanced Architecture and Design
Lab 6: Reduce Clock Period

Lab Descriptions

- **Lab 1: Timing Analyzer, Constraints, and Closure –** Create global timing constraints, read timing reports, apply path-specific constraints (multi-cycle and false paths), and apply advanced implementation options.
- **Lab 2: UCF and Scripting –** Write constraints directly into a UCF file. Write program commands into a batch file to implement the design. Modify the constraint values and program switches to obtain the greatest possible performance from the design.
- **Lab 3: RPM –** Create an RPM in a UCF file. Use the Timing Analyzer to find a path that is not meeting timing constraints, and identify the components of that path. RLOC the components to create the RPM and improve timing for that path.
- **Lab 4: FPGA Editor –** Use the FPGA Editor to view and edit a design. Analyze the contents of a CLB; add a probe; remove, place, and modify components; and analyze long nets.
- **Lab 5: Floorplanner and Incremental Design –** Use incremental design techniques and Floorplanner to gain faster turnaround times (on iterative design changes) when you make changes to a module.
- **Lab 6: Reduce Clock Period –** Use all of your obtained knowledge to reduce the clock period delay

Get the Advantage Today

Xilinx delivers public and private courses in locations throughout the world. Please contact us for more information. You must have your tuition payment information available when you enroll. We accept credit cards (Visa, Master Card, or American Express) as well as purchase orders and training credits.

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In Europe

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