EDUCATION SERVICES
Xilinx Global Services

EDUCATION SERVICES COURSE LISTING

EFFECTIVE January 1, 2003

Xilinx Education Services courses dramatically reduce your time to knowledge which improves your design efficiency and reduces your overall development costs.

FPGA DESIGN

Fundamentals of FPGA Design, ISE 5

Level: Fundamental **Duration: 1 Day** **Credits (N. America): 5** **Cost: US $500**

Understand Xilinx FPGA architecture and learn to implement a complete design in one day. This course provides you with an introduction to designing with Xilinx FPGAs using Xilinx ISE 5. New ISE 5 features covered in this course include the Architecture Wizard, assistance in assigning pins, and creating area constraints (PACE). Other topics include design planning, implementation options, and global timing constraints. Reduce your learning curve through several practical labs.

Designing for Performance, ISE 5

Level: Intermediate **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

Learn design techniques to help improve your design's performance. This course builds on the principles covered in our "Fundamentals of FPGA Design" course with an emphasis on achieving timing closure. Topics include FPGA design techniques, HDL coding techniques, the CORE Generator™ system, power estimation, timing analysis, advanced timing constraints, and advanced implementation options.

Designing for Performance Live Online

Level: Intermediate **Duration: Series** **Credits (N. America): 9** **Cost: US $900**

Enhance your knowledge of Xilinx FPGA tools without ever leaving the office! This Live Online offering includes a series of five one-hour lecture modules and four one-hour lecture modules with labs - all of which have been selected from our Designing for Performance instructor led course. In fact, a live instructor delivers this course as they would in a classroom setting. Opportunities exist to ask questions remotely as well as participate in hands on lab work. Modules are scheduled sequentially twice a week over a five-week period. Avoid travel time and costs while staying on track with a competitive edge.

Designing for Performance for the ASIC User, ISE 5

Level: Intermediate **Duration: 3 days** **Credits (N. America): 15** **Cost: US $1500**

Are you an ASIC designer that wants to get the most out of your FPGA design? Then, this course is for you. Learn the FPGA design techniques you need to improve your design's performance. Course highlights include ASIC design and verification techniques compared and contrasted to FPGA design and verification techniques, how to re-target ASIC code for Xilinx with a 10-step Conversion Guide, and HDL inference of FPGA resources with coding examples.

Advanced FPGA Implementation, ISE 5

Level: Advanced **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

Push the limits of your design by learning how to effectively use the advanced-level Xilinx tools. Several new ISE 5 features are covered in this course, which include Data2BRAM enhancements, incremental design, scripting capability in Project Navigator, ability to create an IP core from an RPM, and FPGA Editor Probe enhancements.

DSP DESIGN

DSP Design Flow

Level: Intermediate **Duration: 3 days** **Credits (N. America): 15** **Cost: US $1500**

This course covers the Xilinx design flow for implementing DSP functions. The main focus of this course is on the System Generator for DSP. The class also includes information on HDL design flow, the CORE Generator, design implementation tools, and hardware verification. You will gain extensive experience with system-level design, while also becoming familiar with Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware verification.

DSP Implementation Techniques

Level: Advanced **Duration: 3 days** **Credits (N. America): 18** **Cost: US $1800**

This course bridges the gap between the DSP algorithm/system designer and the hardware engineer. As well as describing how the algorithms can be efficiently implemented, the techniques will also demonstrate which decisions, at the system level, have the greatest impact on the implementation process and product costs.

HIGH-SPEED SERIAL DESIGN

Designing with RocketIO Multi-Gigabit Transceiver

Level: Intermediate **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

Learn how to employ RocketIO™ in your Virtex-II Pro™ design. Understand and use the features of the Rocket I/O transceiver blocks such as CRC, 8b/10b encoding, channel bonding, clock correction, and comma detection. Additional highlighted topics include debugging techniques, use of the Architecture Wizard, and synthesis and implementation considerations. More than half of this class is in the lab, where you get practical hands-on training in addition to classroom instruction, so you'll quickly become proficient in high-speed serial I/O design.

EMBEDDED SYSTEMS DESIGN

Embedded Systems Development

Level: Intermediate **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

Looking for a hands on approach to developing embedded systems? Attend this training to gain a better understanding of developing a PowerPC and MicroBlaze embedded system using the Embedded Development Kit (EDK). The course will discuss and provide hands on labs regarding the development, debug, and simulation of the embedded system. Currently all lab work is done utilizing the PowerPC included in Virtex-II Pro.

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LANGUAGES

Introduction to Verilog
Level: Fundamental **Duration: 3 days** **Credits (N. America): 15** **Cost: US$1500**

This comprehensive course is an effective introduction to the Verilog language. Course emphasis includes targeting Xilinx and FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design using a top-down synthesis approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

Introduction to VHDL
Level: Fundamental **Duration: 3 days** **Credits (N. America): 15** **Cost: US $1500**

This comprehensive course is an effective introduction to the VHDL language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design using a top-down synthesis design approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

Advanced VHDL
Level: Advanced **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

Increase your VHDL proficiency by learning advanced techniques to help you write more robust and reusable code. This comprehensive course is targeted towards designers who already have some experience with VHDL. The course highlights modeling, testbenches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs, as compared to lecture modules.

PCI DESIGN

PCI Core Basics
Level: Fundamental **Duration: 1 day** **Credits (N. America): 5** **Cost: US $500**

This course introduces basic PCI concepts and architectures. It also gives an overview of Xilinx PCI solutions and includes two labs illustrating the general design flow from core configuration to verification and PCI bus transactions.

Designing a PCI System
Level: Intermediate **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

Using the Xilinx PCI core in your system? This course provides intensive training for designing with Xilinx PCI products. You will learn about specific Xilinx PCI cores, including PCI 64/66 Virtex, PCI 32 Spartan™/Spartan-XL, and PCI 32/33. Design concepts and verification strategies for a PCI system design are covered in detail. The course focuses on hands-on experience via labs where you perform extensive simulation verification using the Xilinx PCI core.

Designing for PCI-X
Level: Intermediate **Duration: 2 days** **Credits (N. America): 10** **Cost: US $1000**

This course focuses on the PCI-X Addendum to the PCI Local Bus Specification and provides a detailed investigation into the operation of the PCI-X LogiCORE. Explaining the basic principles and concepts introduced by the PCI-X Addendum, this course is also intended to provide an in-depth understanding of the PCI-X LogiCORE and how a digital designer may interface this to a typical user application to create a flexible PCI-X solution.

Free Recorded e-Learning — Learn All About What's New In ISE 5

Learn about the advanced ISE software technologies in our series of free, recorded ISE 5 technical lectures that are available online 24 hours a day/7 days a week. View them on the Education Services website at:
http://www.xilinx.com/support/training/ise-whats-new-5.htm

Education Packages — Special Savings on Course/Product Combinations

- FPGA Essentials – Fundamentals of FPGA Design & Designing for Performance, save $200 on 3 days of training
- Designing for Performance Live Online - Save time and travel costs
- DSP – DSP Design Flow + Xilinx System Generator for DSP
- EDK – Embedded Systems Development + Embedded Development Kit

For more information, see the Education Services website at:
http://www.support.xilinx.com/support/training/training.htm

For a complete description of the above courses, including detailed course outlines, lab descriptions, and availability in your region, please reference: **http://www.support.xilinx.com/support/training/training.htm**

In Europe, please reference: **http://www.support.xilinx.com/support/training/europe-home-page.htm**

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