

Introduction

The Spartan™-II family is the second generation high-volume production FPGA solution, based on the highly successful Virtex™ family architecture. The family delivers all the key requirements for ASIC replacement with up to 200,000 gates and 200 MHz system performance at 2.5V logic supply. These requirements include high performance, on-chip RAM, core solutions and prices that, in high volume, approach and in many cases are equivalent to mask programmed ASIC devices.

The Spartan-II family is the result of more than fifteen years of FPGA design experience and feedback from thousands of customers. By streamlining the Virtex family feature set, leveraging advanced hybrid process technologies and focusing on total cost management, the Spartan-II family delivers the key features required by ASIC and other high volume logic users while avoiding the initial cost, long development cycles and inherent risk of conventional ASICs. The Spartan-II family currently has five members, as shown in [Table 1](#).

Features

- Second generation ASIC replacement technology
 - On-chip RAM (block and distributed)
 - Power down mode ($I_{CCO} = 100 \mu A$)
 - Density up to 5,292 logic cells or 200,000 system gates
 - Hot-swappable for Compact PCI
 - Advanced 0.22/0.18 μm 6-layer metal process
 - Streamlined feature set based on Virtex architecture
 - Unlimited reprogrammability
 - Very low cost

- System level features
 - Two types of on-chip SelectRAM™ memory, distributed and block
 - Fully PCI compliant
 - Low power segmented routing architecture
 - Full readback capability for program verification and internal node observability
 - Dedicated carry logic for high-speed arithmetic
 - Dedicated multiplier support
 - Cascade chain for wide-input functions
 - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
 - Four dedicated delay-locked loops (DLLs) for advanced clock control
 - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
 - IEEE 1149.1-compatible boundary scan logic
- Versatile I/O and packaging
 - Low cost packages available in all densities
 - Family footprint compatibility in common packages
 - 16 high-performance interface standards
 - Zero input register hold time simplifies system timing
- Fully supported by powerful Xilinx development system
 - Foundation Series: Integrated, shrink-wrap software
 - Alliance Series: Over 100 PC and workstation third party development systems supported
 - Fully automatic mapping, placement and routing
 - Interactive design editor for design optimization

Table 1: Spartan-II Field-Programmable Gate Array Family Members.

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array	Total CLBs	Maximum Available User I/O	Total Block Ram Blocks	Total Block RAM Bits
XC2S15	432	6,000 - 15,000	8x12	96	86	4	16,384
XC2S30	972	13,000 - 30,000	12x18	216	132	6	24,576
XC2S50	1,728	23,000 - 50,000	16x24	384	176	8	32,768
XC2S100	2,700	37,000 - 100,000	20x30	600	196	10	40,960
XC2S150	3,888	52,000 - 150,000	24x36	864	260	12	49,152
XC2S200	5,292	71,000 - 200,000	28x42	1,176	284	14	57,344

General Overview

Spartan-II family of FPGAs is implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels) also providing advanced functions such as Block RAM and DLL clock control blocks. (See [Figure 1](#).)

The devices are customized by loading configuration data into internal static memory cells. Unlimited Re-programming cycles are possible with this approach. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can be programmed in one of three modes. The traditional Master Serial mode, Slave Serial mode, or Slave Parallel mode.

Spartan-II family FPGAs are typically used in high volume, applications where the versatility of a fast programmable

solution will add benefits. Spartan-II family FPGAs are ideal for shortening design and development cycles, and at the same time offer a cost-effective solution where product production volumes require 50,000 to well over 1,000,000 devices per year.

Spartan-II family devices achieve high-performance, low cost operation through the use of an advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates exceeding 200 MHz and internal performance in excess of 350 MHz. In contrast to other FPGA devices, Spartan-II FPGAs offer the most cost effective solution while maintaining leading edge performance. In addition to the conventional benefit of high volume programmable logic solutions, Spartan-II FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, block RAM, DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

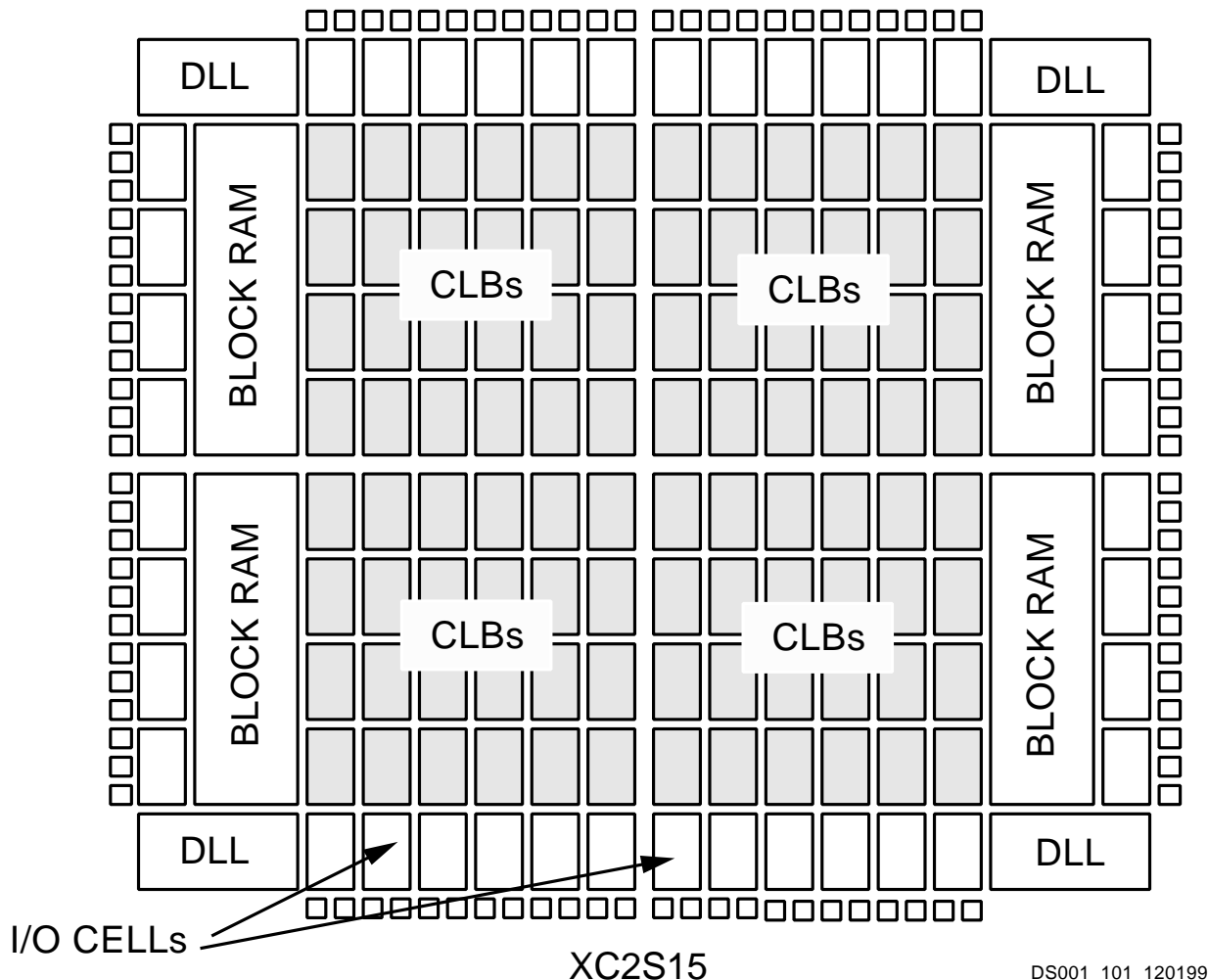


Figure 1: Basic Spartan-II Family FPGA Block Diagram

Architectural Description

Spartan-II Array

The Spartan-II user-programmable gate array, shown in Figure 1, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versital Multi-Level Interconnect structure

As you can see in the figure, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be desicussed in detail in the following discussions.

Input/Output Block

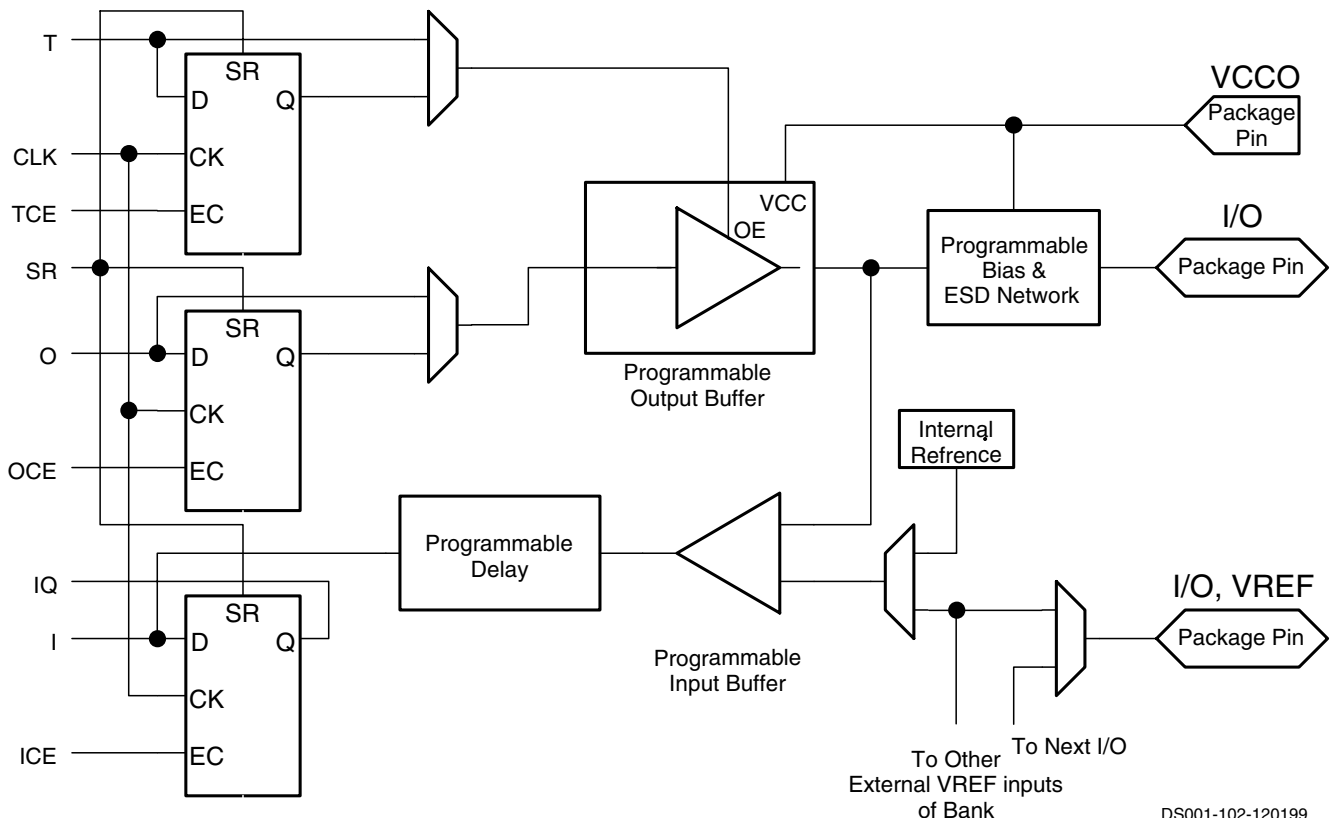
The Spartan-II IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signalling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and buss interfaces. Table 2 lists several of the standards which are supported along with the required refrence, output & termination voltages needed to meet the standard.

The three IOB registers function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent clock enable signals for each registers.

In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each registers, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

A feature not shown in the block diagram, but controllable by the software is polarity control. The input and output buffers and all of the IOB control signals have independent polarity controls.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration all outputs not involved in configuration are forced



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Figure 2: Spartan-II Input/Output Block (IOB)

into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up.

Table 2: Supported I/O Standards

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTTL 2 to 24 mA	N/A	3.3	N/A
LVC MOS2	N/A	2.5	N/A
PCI	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	1.5
HSTL Class III	0.75	1.5	1.5
HSTL Class IV	0.75	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP	1.32	3.3	N/A

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5V compliance, and one that does not. For 5V compliance, a zener-like structure connected to ground turns on when the output rises to approximately 6.5V. When 5V compliance is not required, a conventional clamp diode may be connected to the output supply voltage, V_{CCO} . The type of over-voltage protection can be selected independently for each pad.

All Spartan-II IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the Spartan-II IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} . The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking" on page 5.

There are optional pull-up and pull-down resistors at each input for use after configuration. Their value is in the range 50 to 150 kohms.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

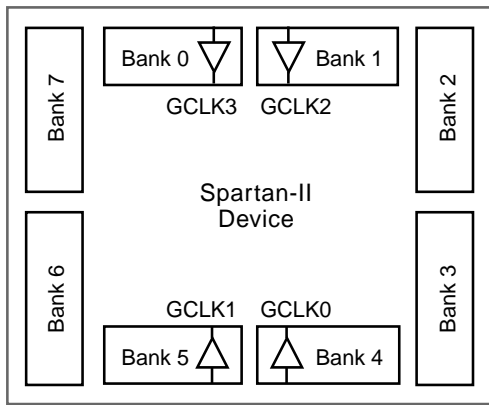
The 3-state control of the output can also be routed directly from the internal logic or through a flip-flop that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking" on page 5.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.



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Figure 3: Spartan-II I/O Banks

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Within a bank, output standards may be mixed only if they use the same V_{CCO} . Compatible standards are shown in Table 3. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO} .

Table 3: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF} . In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage may be used within a bank. Input buffers that use V_{REF} are not 5V-tolerant. LVTTTL, LVCMOS2, and PCI are 5V-tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins may be left unconnected externally, or may be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

In TQ144 and PQ208 packages, all V_{CCO} pins are bonded together internally, and consequently the same V_{CCO} voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for V_{CCO} . In both cases, the V_{REF} pins remain internally connected as eight banks, and may be used as described previously.

Configurable Logic Block

The basic building block of the Spartan-II CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Spartan-II CLB contains four LCs, organized in two similar slices, a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

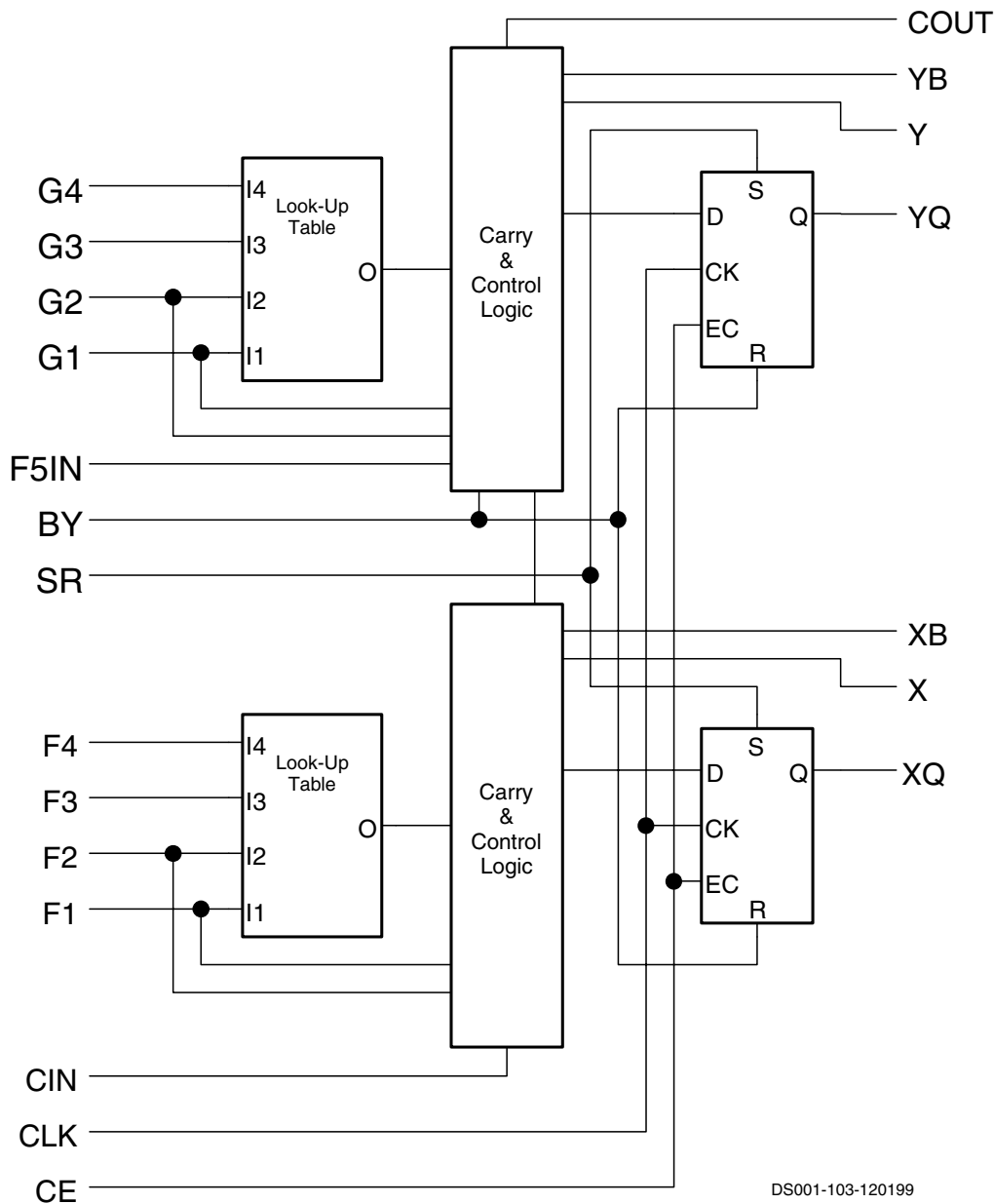
Look-Up Tables

Spartan-II function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Spartan-II slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by



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Figure 4: Spartan-II CLB Slice (two identical slices in each CLB)

the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Spartan-II CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See “Dedicated Routing” on page 8. Each Spartan-II BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Spartan-II FPGAs incorporate several large Block SelectRAM+ memories. These complement the distributed SelectRAM+ LUTRAMs that provide shallow RAM structures implemented in CLBs.

Block SelectRAM+ memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 4: Spartan-II Block SelectRAM+ Amounts

Spartan-II Device	# of Blocks	Total Block SelectRAM+ Bits
XC2S15	4	16,384
XC2S30	6	24,576
XC2S50	8	32,768
XC2S100	10	40,960
XC2S150	12	49,152
XC2S200	14	57,344

Each Block SelectRAM+ cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 5 shows the depth and width aspect ratios for the Block SelectRAM+.

Table 5: Block SelectRAM+ Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources, as shown in Figure 6, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

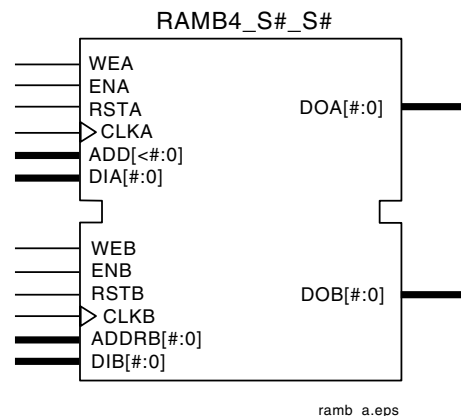


Figure 5: Dual-port Block SelectRAM+

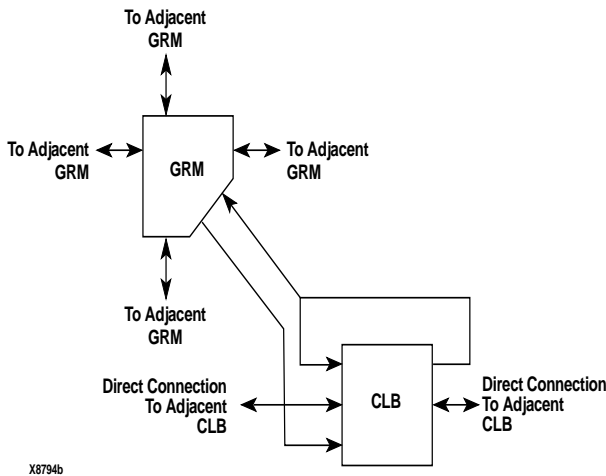


Figure 6: Spartan-II Local Routing

General Purpose Routing

Most Spartan-II signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that

distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-II devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-II architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 7.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-II devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12

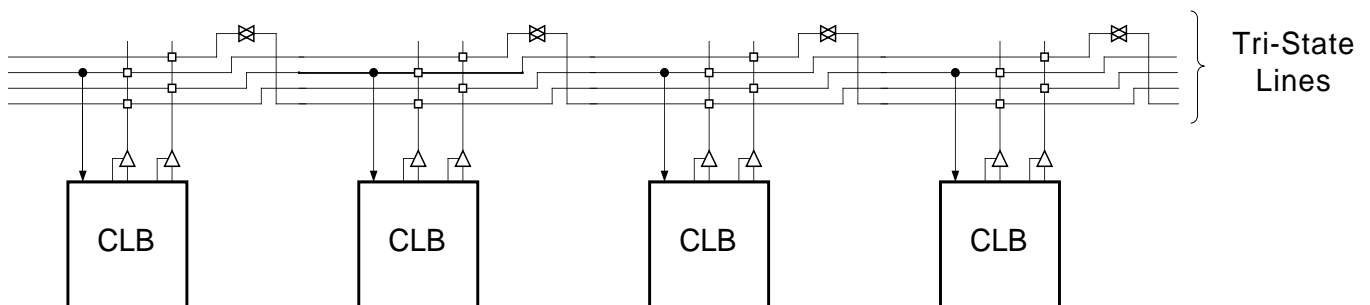


Figure 7: BUFT Connections to Dedicated Horizontal Bus Lines

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across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The

DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 6 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins. This technique partially compensates for the absence of INTEST support.

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

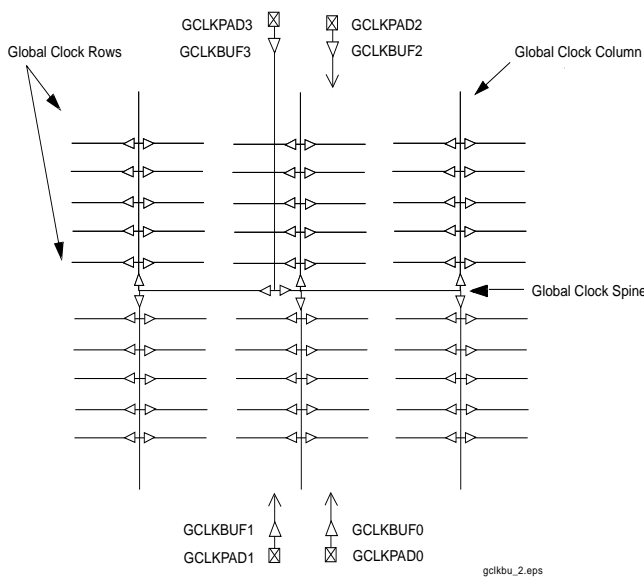


Figure 8: Global Clock Distribution Network

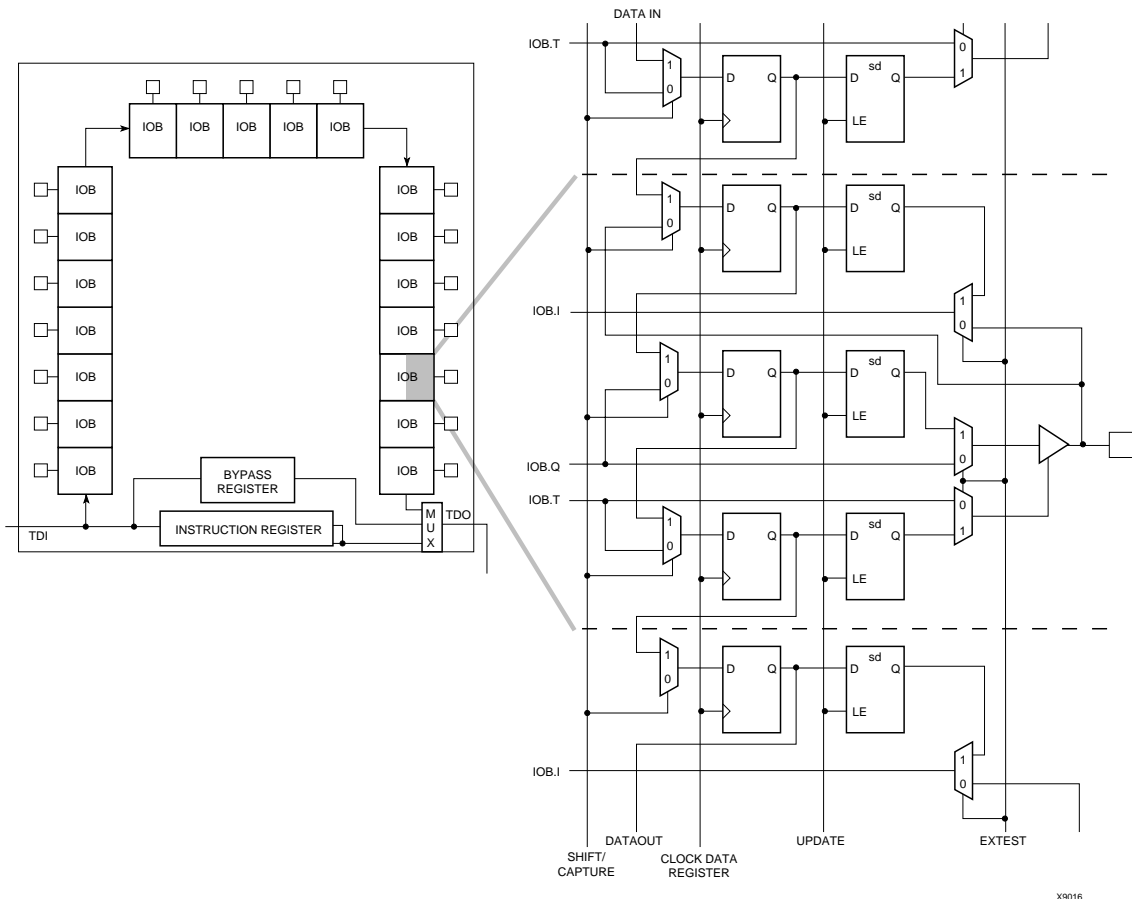


Figure 9: Spartan-II Family Boundary Scan Logic

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary

scan I/O data register, while the output-only pins contribute all three bits.

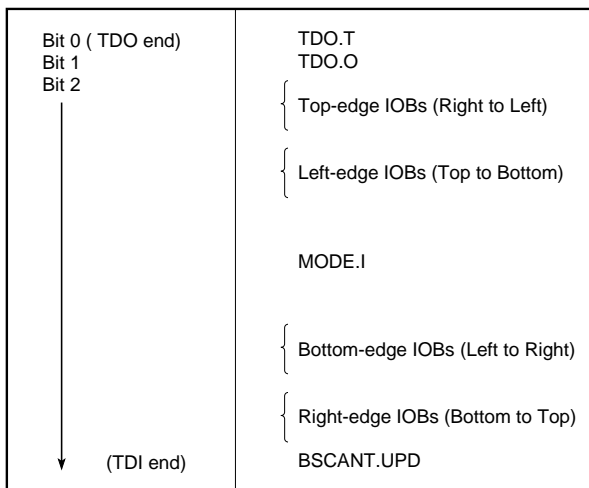
From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx web site in the File Download area.

Development System

Spartan-II FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Spartan-II design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.



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Figure 10: Boundary Scan Bit Sequence

Table 6: Boundary-scan Instructions

Boundary-scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan INTEST operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Tri-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Spartan-II design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The "soft macro" portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates Timing Wizard[®] timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE[®] static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Configuration is the process by which the bit-stream of a design, as generated by the Xilinx development software, is loaded into the internal configuration memory of the FPGA. Spartan-II devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Table 7: Spartan-II Configuration File Size

Device	Configuration File Size (Bits)
XC2S15	197,728
XC2S30	336,800
XC2S50	559,232
XC2S100	781,248
XC2S150	1,040,128
XC2S200	1,335,840

The Configuration File

Spartan-II devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. [Table 7](#) shows how much nonvolatile storage space is needed for Spartan-II devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (i.e., hard drives, FLASH cards, etc.) can be used. For more information on configuration without a PROM, refer to XAPP098 'The Low-Cost, Efficient Serial Configuration of Spartan FPGAs.

Modes

Spartan-II supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in [Table 8](#).

Table 8: Configuration Codes

Configuration Mode	Pre-configuration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D _{out}
Master-serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave-serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions. The other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the PROGRAM pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTTL signal. All the relevant pins fall in banks 2 or 3.

For a more detailed description than that given below, see Pin Definitions and XAPP176, "Spartan-II FPGA Series Configuration and Readback".

The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

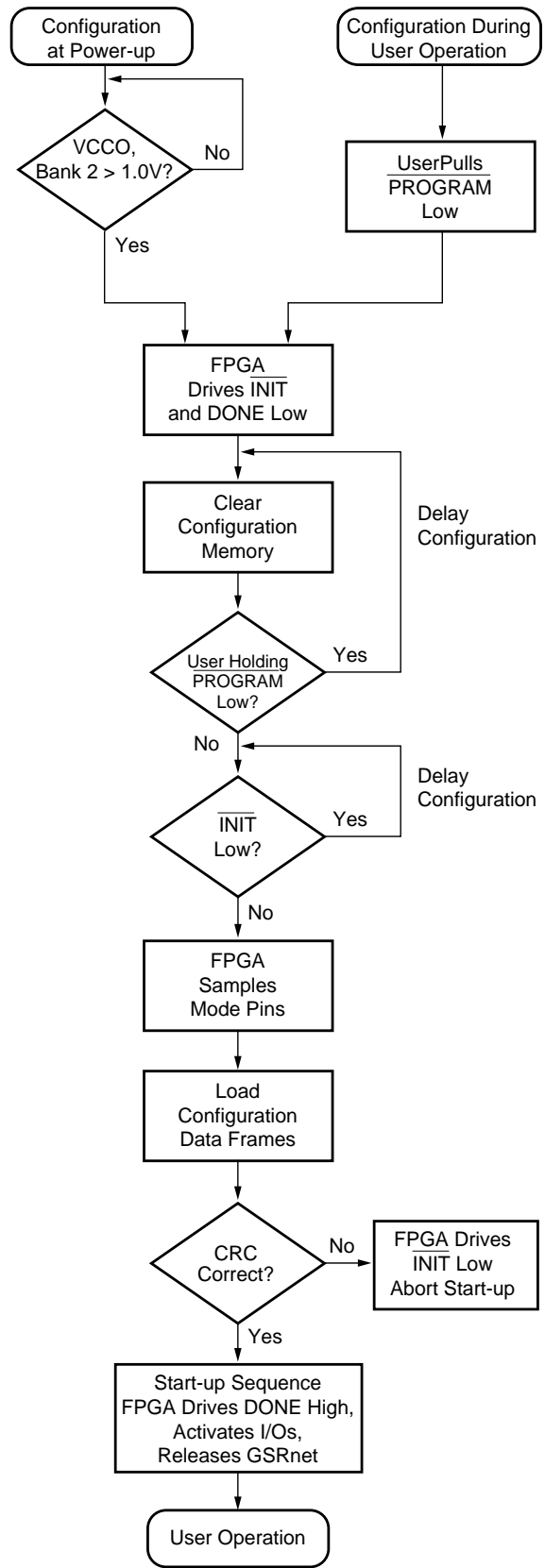
- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

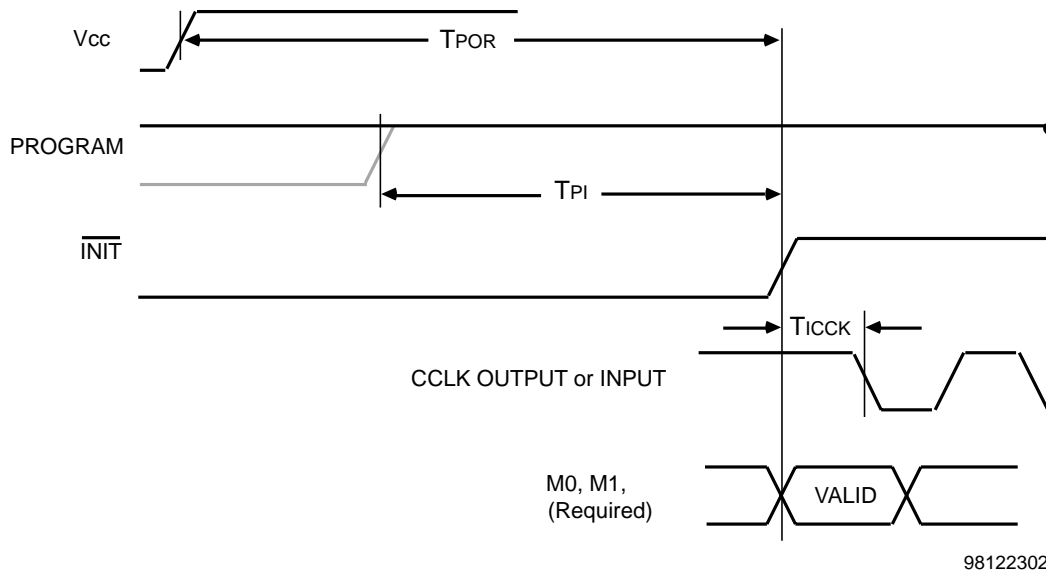
There are two different ways to initiate the configuration process: applying power to the device or asserting the PROGRAM input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown Figure 12 on page 14. Before configuration can begin, V_{CCO} for bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 2.5V supply. At power-up, V_{cc} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling



ds001_03_112299

Figure 11: Configuration Flow Diagram



Description	Symbol		Units
Power-on Reset	T_{POR}	2	ms, max
Program Latency	T_{PL}	100	μ s, max
CCLK (output) delay	T_{ICCK}	0.5	μ s, min
		4	μ s, max

Figure 12: Configuration Timing on Power-Up

$\overline{PROGRAM}$ Low until V_{cc} is valid. For more information on delaying configuration, see the next section.

Once in user operation, the device can be re-configured simply by pulling the $\overline{PROGRAM}$ pin Low. The device acknowledges the beginning of the configuration process by driving $DONE$ Low, then enters the memory-clearing phase.

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving \overline{INIT} Low. At this time, the user can delay configuration by holding either $\overline{PROGRAM}$ or \overline{INIT} Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional \overline{INIT} line is driving a Low logic level during memory clearing. Thus, to avoid contention, use an open-drain driver to keep \overline{INIT} Low.

With no delay in force, the device indicates that the memory is completely clear by driving \overline{INIT} High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data.

Once \overline{INIT} is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of opera-

tions necessary to load configuration data using the serial modes is shown in [Figure 14](#) Loading data using the Slave Parallel mode is shown in [Figure 19 on page 19](#).

CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives \overline{INIT} Low to indicate that a frame error has occurred and configuration is aborted.

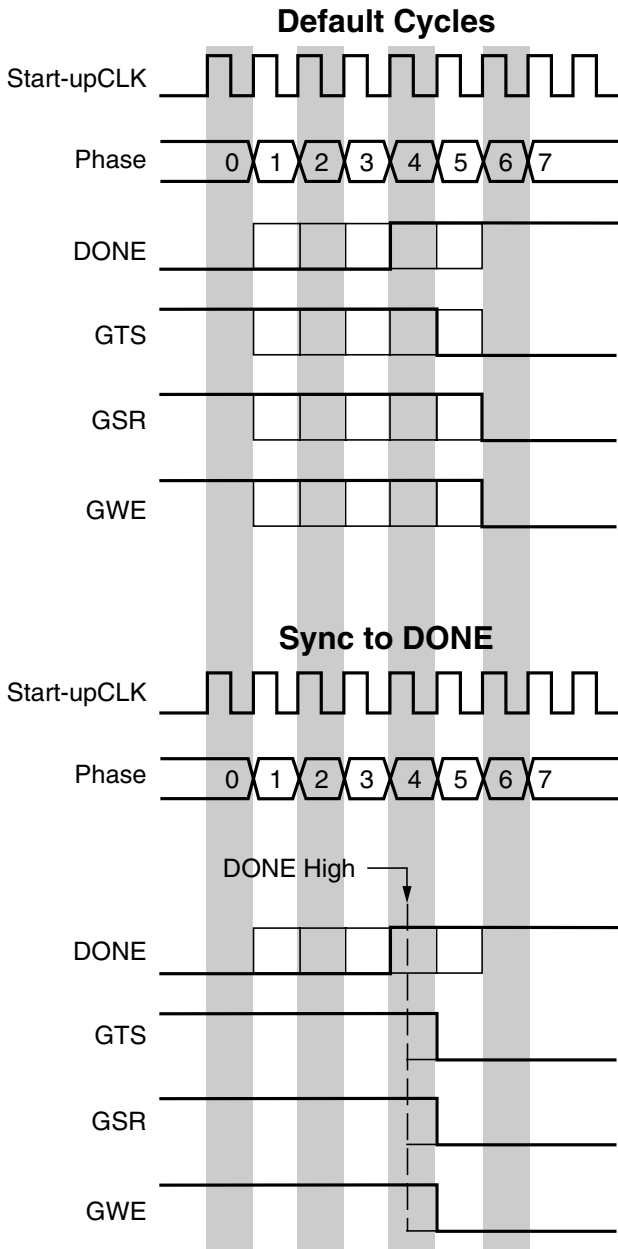
To reconfigure the device, the $\overline{PROGRAM}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See ["Initiating Configuration" on page 13](#)

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of $DONE$. The failure of $DONE$ to go High may indicate the unsuccessful loading of configuration data.



X138_01_082599

Figure 13: Start-up Waveforms

2. The release of the Global Three State. This activates all the I/Os.
3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13 on page 15. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in Bit-

Gen, part of the Xilinx Development Software. The heavy lines show the defaults settings.

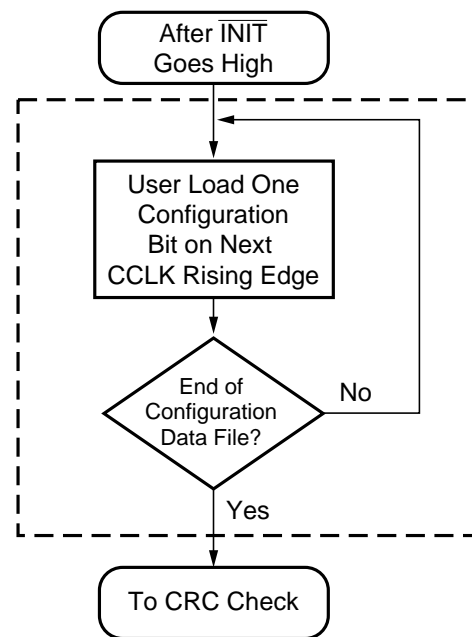
The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the BitGen configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The Serial Modes

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in the master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the D_{IN} pin first.

The sequence of operations necessary to load data into the Spartan-II FPGA serially appears in Figure 14. This is an expansion of the "Load Configuration Data Frames" block in Figure 11 on page 13.



ds001_01_112299

Figure 14: Loading Config. Data for the Serial Modes

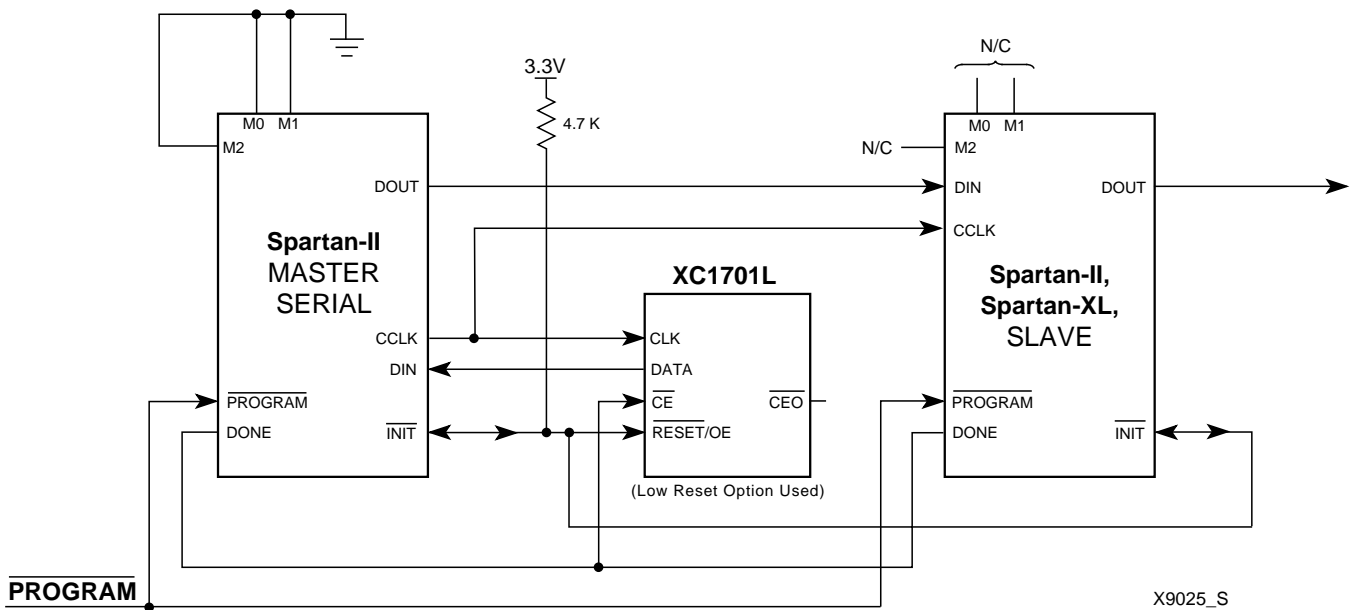


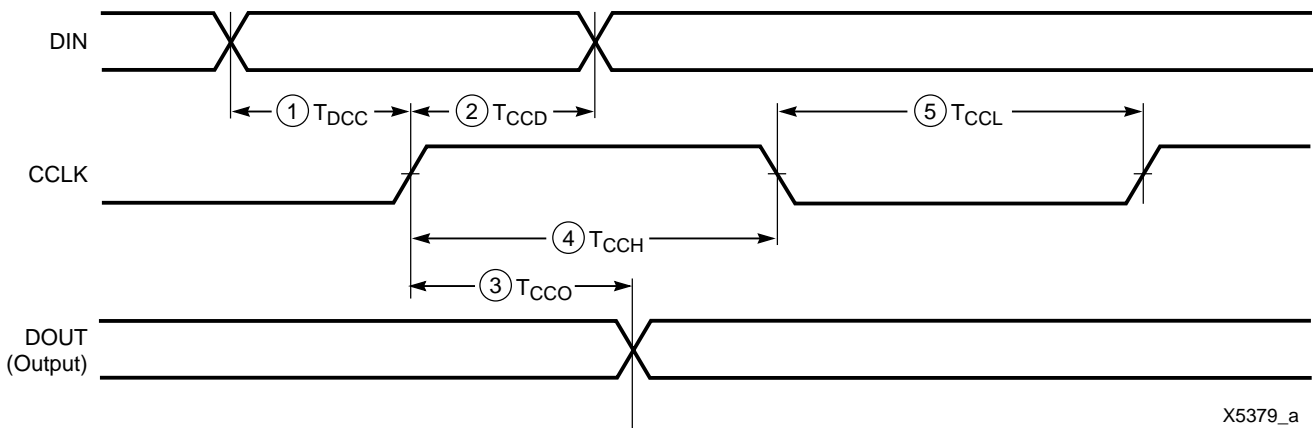
Figure 15: Master/Slave Serial Configuration Circuit Diagram

Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source. This mode allows for FPGAs to be configured from other logic devices, such as microprocessors, or in a daisy-chain configuration. Figure 15 on page 16 shows the connections for a Master Serial FPGA configuring a Slave Serial FPGA from an SPROM. A Spartan-II device in

slave serial mode should be connected as shown for the third device from the left. Master serial mode is selected by a <111> on the mode pins (M0, M1, M2).

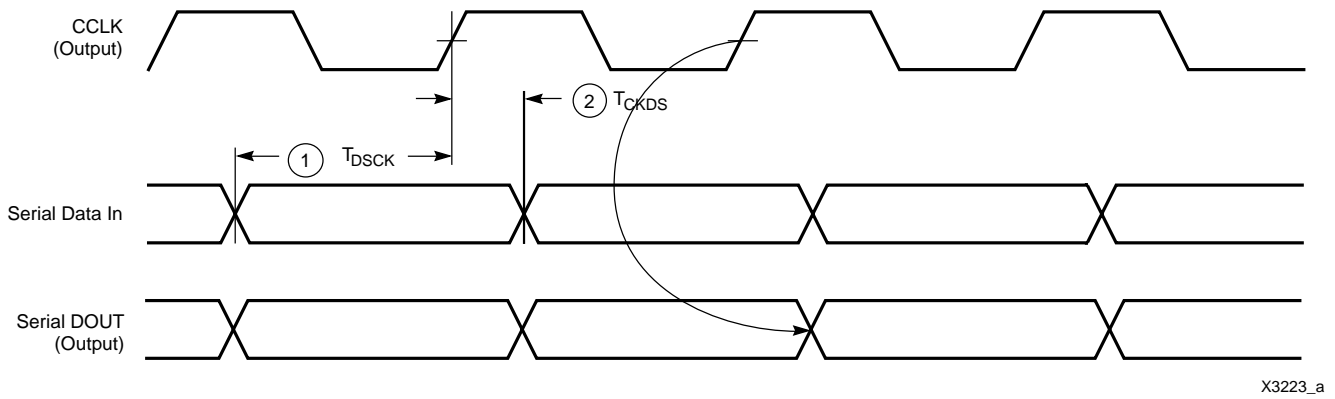
Figure 16 on page 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.



X5379_a

	Description	Symbol	Units
CCLK	DIN setup	1 T_{DCC}	5 ns, min
	DIN hold	2 T_{CCD}	0 ns, min
	DOUT	3 T_{CCO}	12 ns, max
	High time	4 T_{CCH}	5 ns, min
	Low time	5 T_{CCL}	5 ns, min
	Maximum Frequency		F_{CC}

Figure 16: Slave Serial Mode Timing



X3223_a

	Description	Symbol	Units
CCLK	DIN setup	1 T _{DSCK}	5.0 ns, min
	DIN hold	2 T _{CKDS}	0.0 ns, min
	Frequency Tolerance with respect to nominal		+45% -30%

Figure 17: Master Serial Mode Timing

Multiple FPGAs in slave serial mode can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see "Start-up" on page 14.

Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM which feeds a serial stream of configuration data to the FPGAs DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from an SPROM. A Spartan-II device in master serial mode should be connected as shown for the device on the left side. Master serial mode is selected by a <000> on the mode pins (M0, M1, M2). The SPROM RESET pin is driven by $\overline{\text{INIT}}$, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in BitGen, part of the Xilinx development software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The

period of the CCLK signal created by the internal oscillator has a variance of +45%/-30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at clock frequencies above 50 MHz.

Figure 18 on page 18 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting $\overline{\text{WRITE}}$. See "Readback" on page 19.

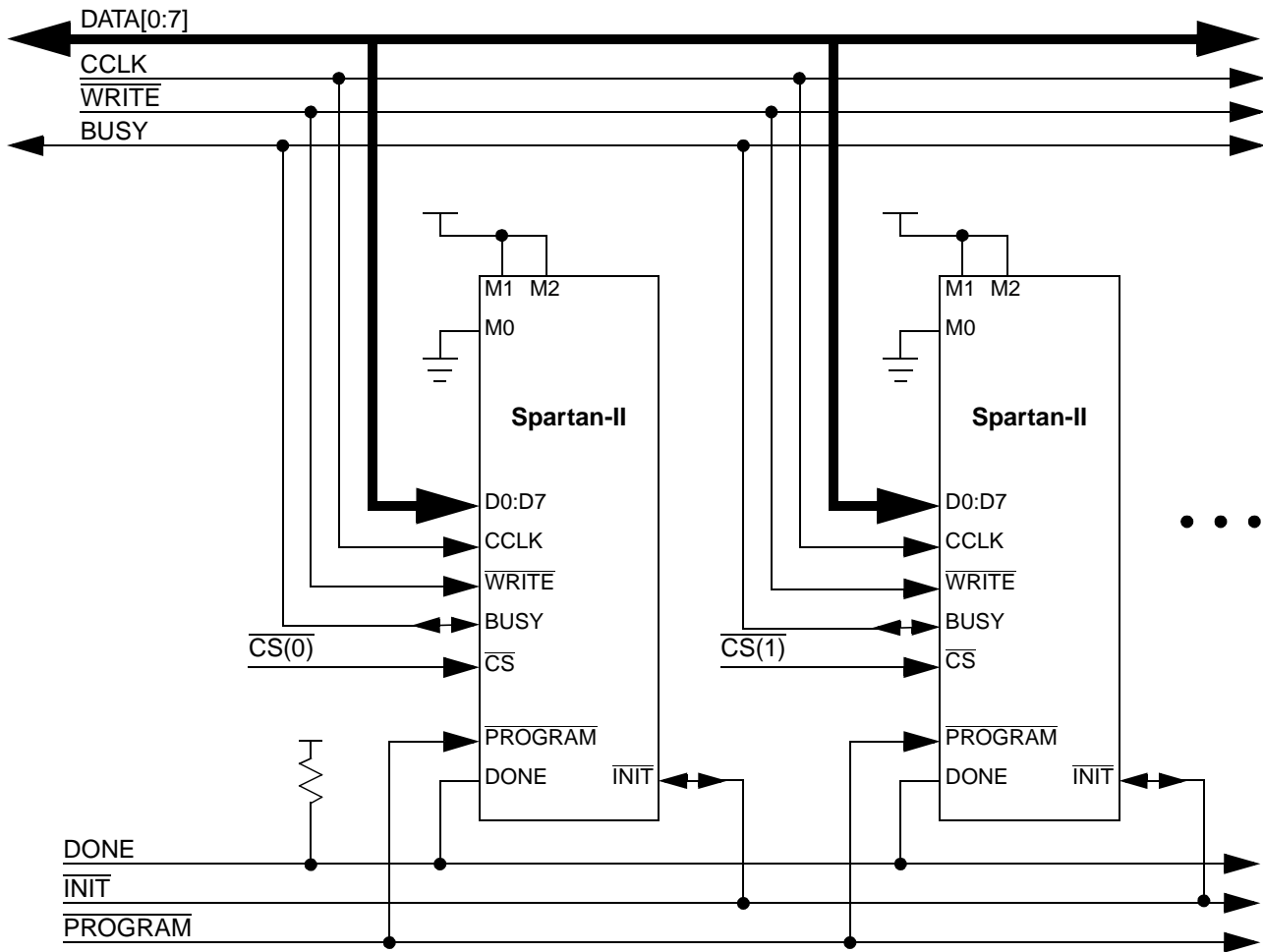


Figure 18: Slave Parallel Configuration Circuit Diagram

Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See [“Start-up” on page 14](#).

Write

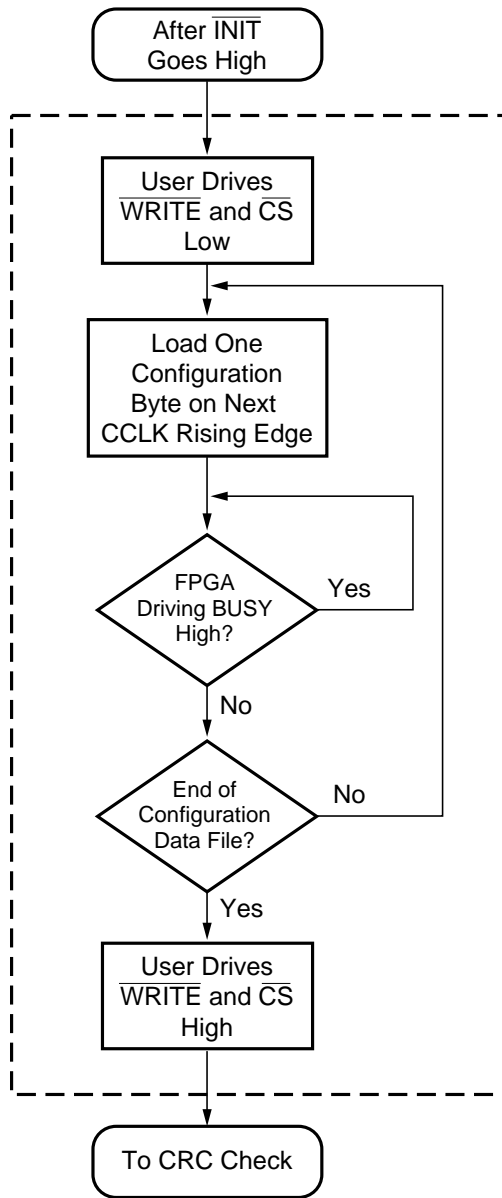
When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. [Figure 19 on page 19](#) shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in [Figure 11 on page 13](#). The timing for write operations is shown in [Figure 20 on page 20](#).

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that

when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

5. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
6. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
7. Repeat steps 2 and 3 until all the data has been sent.
8. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

If CCLK is slower than f_{CCNH} , the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



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Figure 19: Loading Configuration Data for the Slave Parallel Mode

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of \overline{CS} .

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the \overline{CS} signal may be de-asserted until the next byte

is valid on D0-D7. While \overline{CS} is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, \overline{WRITE} must continue to be asserted while \overline{CS} is asserted.

Abort

To abort configuration during a write sequence, de-assert \overline{WRITE} while holding \overline{CS} Low. The abort operation is initiated at the rising edge of CCLK, as shown in [Figure 21 on page 20](#). The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

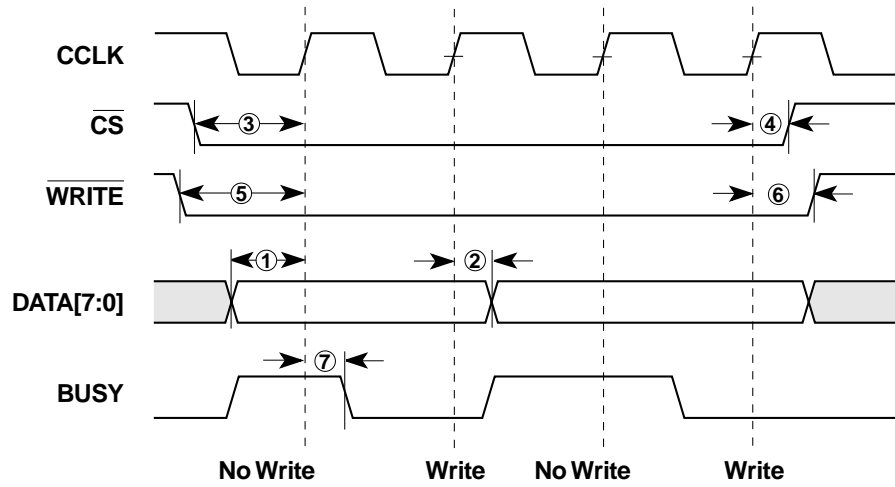
1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <101> on the mode pins (M0, M1, M2).

Readback

The configuration data stored in the Spartan-II configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

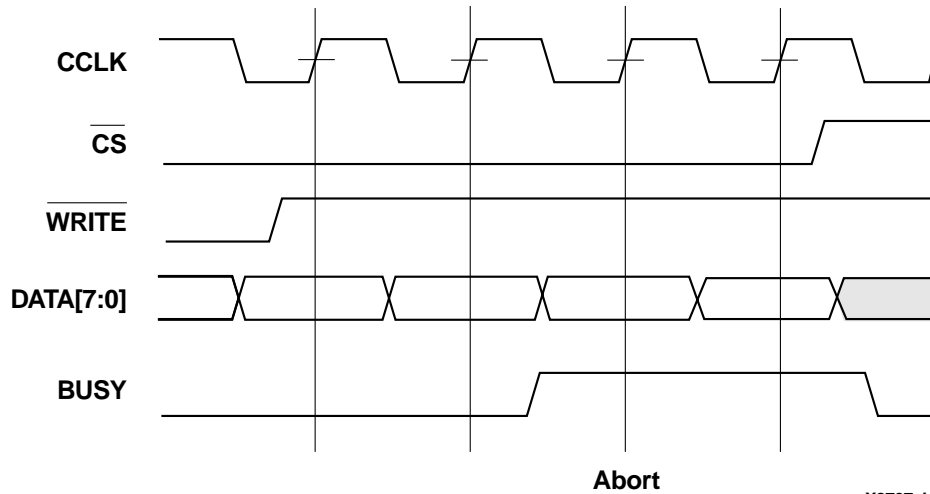
For more detailed information see XAPP176 "Spartan-II FPGA Family Configuration and Readback"



X8796_b

	Description	Symbol			Units
CCLK	D ₀₋₇ Setup/Hold	1	T _{SMDCC}	5	ns, min
	D ₀₋₇ Hold	2	T _{SMCCD}	0	ns, min
	CS Setup	3	T _{SMCSCC}	7	ns, min
	CS Hold	4	T _{SMCCCS}	0	ns, min
	WRITE Setup	5	T _{SMCCW}	7	ns, min
	WRITE Hold	6	T _{SMWCC}	0	ns, min
	BUSY Propagation Delay	7	T _{SMCKBY}	12	ns, max
	Maximum Frequency		F _{CC}	66	MHz, max
	Maximum Frequency with no handshake		F _{CCNH}	50	MHz, max

Figure 20: Slave Parallel Write Timing



X8797_b

Figure 21: Slave Parallel Write Abort Waveforms

Design Considerations

This section contains more detailed design information on the following features.

- Delay-Locked Loop . . . see [page 21](#)
- Block RAM . . . see [page 25](#)
- Versatile I/O . . . see [page 31](#)

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits which improve and simplify system level design.

Introduction

As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit. Two DLLs in can be connected in series to increase the effective clock multiplication factor to four.

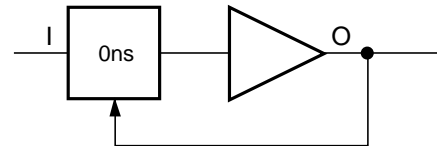
The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

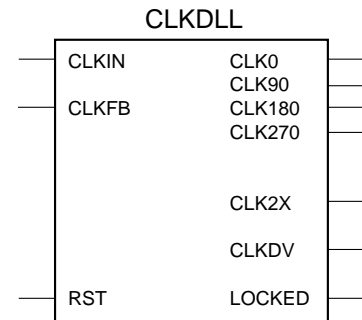
Library DLL Symbols

Figure 22 shows the simplified Xilinx library DLL macro symbol, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These symbols provide access to the complete set of DLL features when implementing more complex applications.



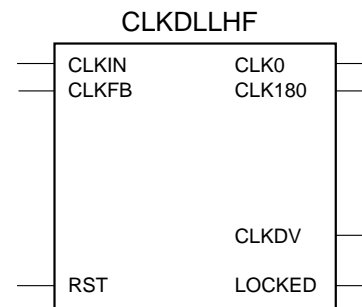
ds022_25_121099

Figure 22: Simplified DLL Macro Symbol BUFGDLL



ds022_26_121099

Figure 23: Standard DLL Symbol CLKDLL



ds022_027_121099

Figure 24: High Frequency DLL Symbol CLKDLLHF

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in [Figure 25](#).

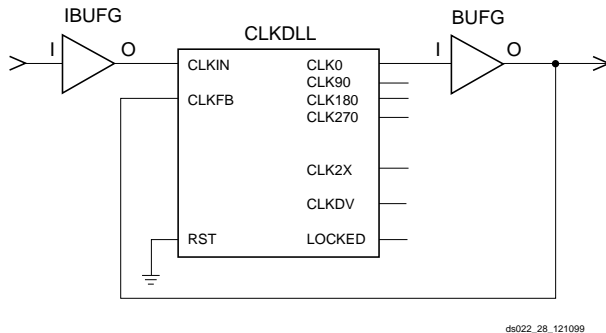


Figure 25: BUFGDLL Schematic

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another

CLKDLL or one of the global clock input buffers (IBUFG) must source this clock signal.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pin.

IBUFG - Global Clock Input Pad

If an IBUFFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer de-skew with respect to one another. For these reasons, rarely use the reset pin unless re-configuring the device or changing the input frequency.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction such that the CLKDV output pin always has a 50/50 duty cycle.

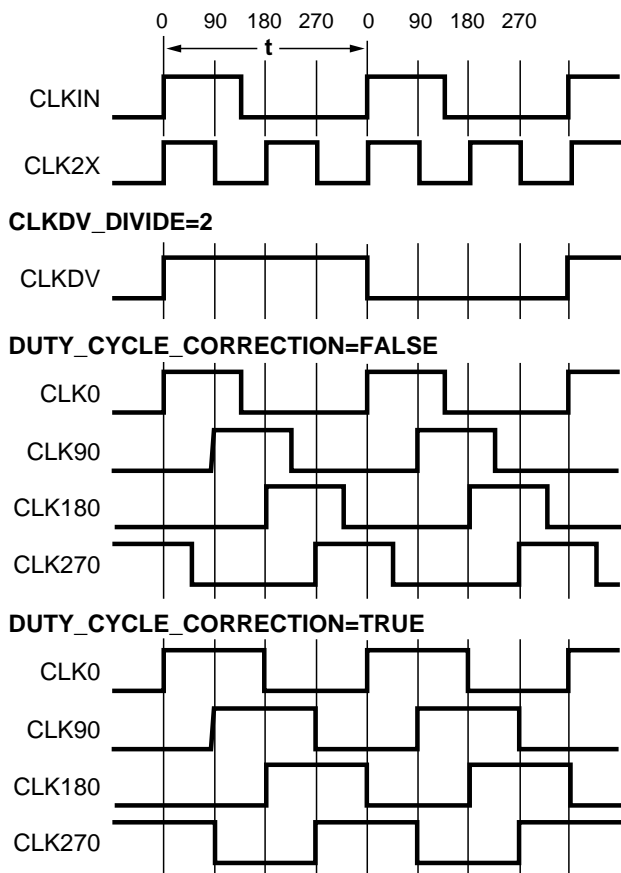
1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 9.

Table 9: Relationship of Phase-Shifted Output Clock to Period Shift

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The timing diagrams in Figure 26 illustrate the DLL clock output characteristics.



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Figure 26: DLL Output Characteristics

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the

DLL symbol. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The DLL timing parameter section of the data sheet provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

DLL Properties

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty-cycle correction deactivates, the output clock has the same duty cycle as the source clock.

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

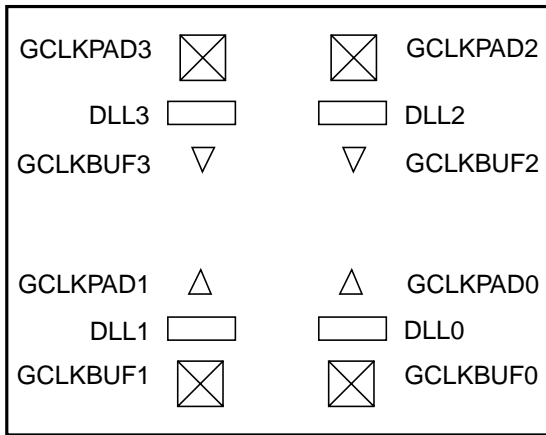
DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL symbol with the numeric identifier 0, 1, 2, or 3,

controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2



x132_08_012400

Figure 27: Orientation of DLLs

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 μs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom).

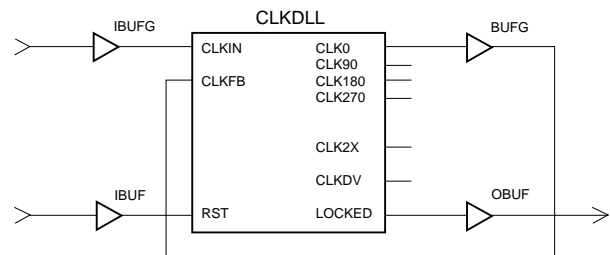
Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Spartan-II DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications.

Standard Usage

The circuit shown in Figure 28 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.



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Figure 28: Standard DLL Implementation

De-skew of Clock and Its 2x Multiple

The circuit shown in Figure 29 implements a 2x clock multiplier and also uses the CLK0 clock output with zero ns skew between registers on the same chip. A clock divider circuit could alternatively be implemented using similar connections.

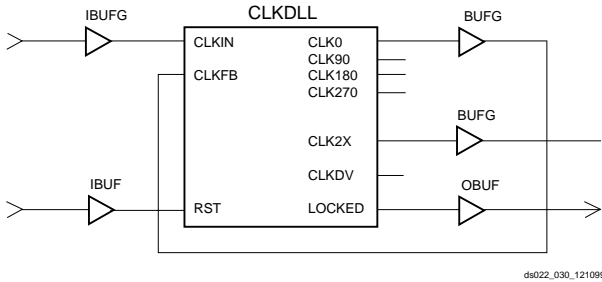


Figure 29: DLL De-skew of Clock and 2x Multiple

Because any single DLL can only access at most two BUFGs, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

Generating a 4x Clock

By connecting two DLL circuits each implementing a 2x clock multiplier in series as shown in Figure 30, a 4x clock multiply can be implemented with zero ns skew between registers in the same device.

If other clock output is needed, the clock could access a BUFG only if the DLLs are constrained to exist on opposite edges (Top or Bottom) of the device.

When using this circuit it is vital to use the SRL16 cell to reset the second DLL after the initial chip reset. If this is not done, the second DLL may not recognize the change of frequencies from when the input changes from a 1x (25/75) waveform to a 2x (50/50) waveform.

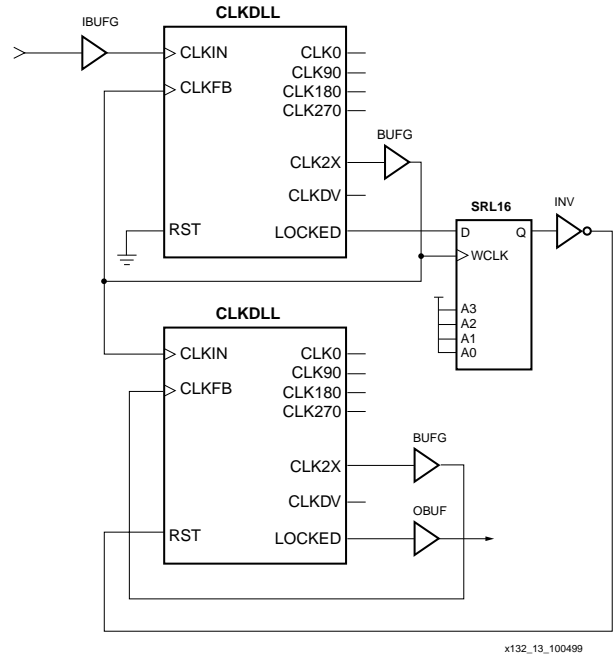


Figure 30: DLL Generation of 4x Clock

Using Block SelectRAM+ Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the Block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The Block SelectRAM+ memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block SelectRAM+ memory supports two operating modes.

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

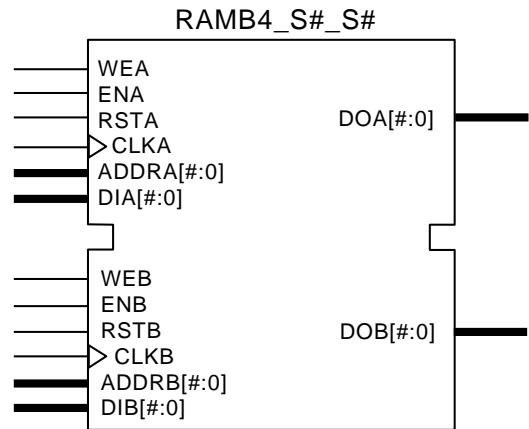
Block SelectRAM+ Characteristics

1. All inputs are registered with the port clock and have a set-up to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The Block SelectRAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (i.e., clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

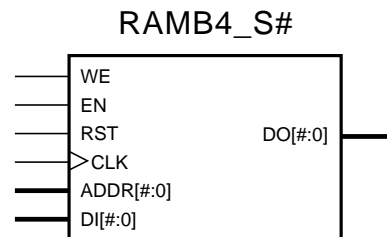
Library Primitives

Figure 31 and Figure 32 show the two generic library Block SelectRAM+ primitives. Table 10 describes all of the available primitives for synthesis and simulation.



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Figure 31: Dual-Port Block SelectRAM+ Memory



ds022_033_121399

Figure 32: Single-Port Block SelectRAM+ Memory

Table 10: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S1		N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4	1	4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2		N/A
RAMB4_S2_S2		2
RAMB4_S2_S4	2	4
RAMB4_S2_S8		8
RAMB4_S2_S16		16
RAMB4_S4		N/A
RAMB4_S4_S4	4	4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8		N/A
RAMB4_S8_S8	8	8
RAMB4_S8_S16		16
RAMB4_S16		N/A
RAMB4_S16_S16	16	16

Port Signals

Each Block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 11 describes the depth and width aspect ratios for the Block SelectRAM+ memory.

Table 11: Block SelectRAM+ Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A/B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A/B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A/B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A/B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A/B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 11.

Data In Bus—DI[A/B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 11.

Data Output Bus—DO[A/B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 11.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ((\text{ADDR}_{\text{port}} + 1) * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Table 12 shows low order address mapping for each port width.

Table 12: Port Address Mapping

Port Width	Port Addresses																
1	4095...	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
		5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	
2	2047...	07	06	05	04	03	02	01	00								
4	1023...	03		02		01		00									
8	511...	01				00											
16	255...	00															

Creating Larger RAM Structures

The Block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The Block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

$$\text{LOC} = \text{RAMB4_R\#C\#}$$

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Conflict Resolution

The Block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
 - The write succeeds
 - The data out on the writing port accurately reflects the data written.
 - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 33 shows a timing diagram for a single port of a Block SelectRAM+ memory. The Block SelectRAM+ AC switching characteristics are specified in the data sheet. The Block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO

bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

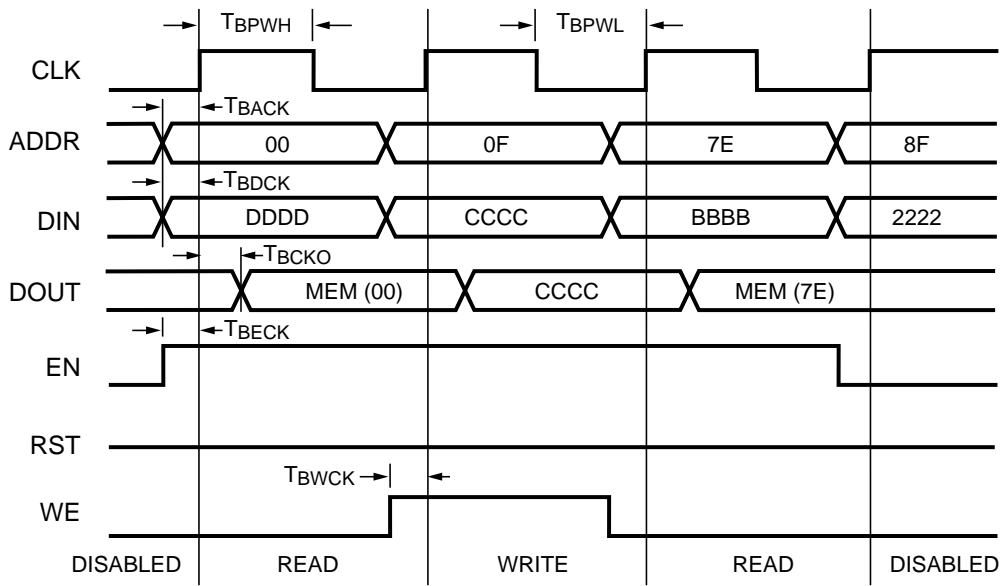
At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the Block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write Block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS} , (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in **Figure 33**.

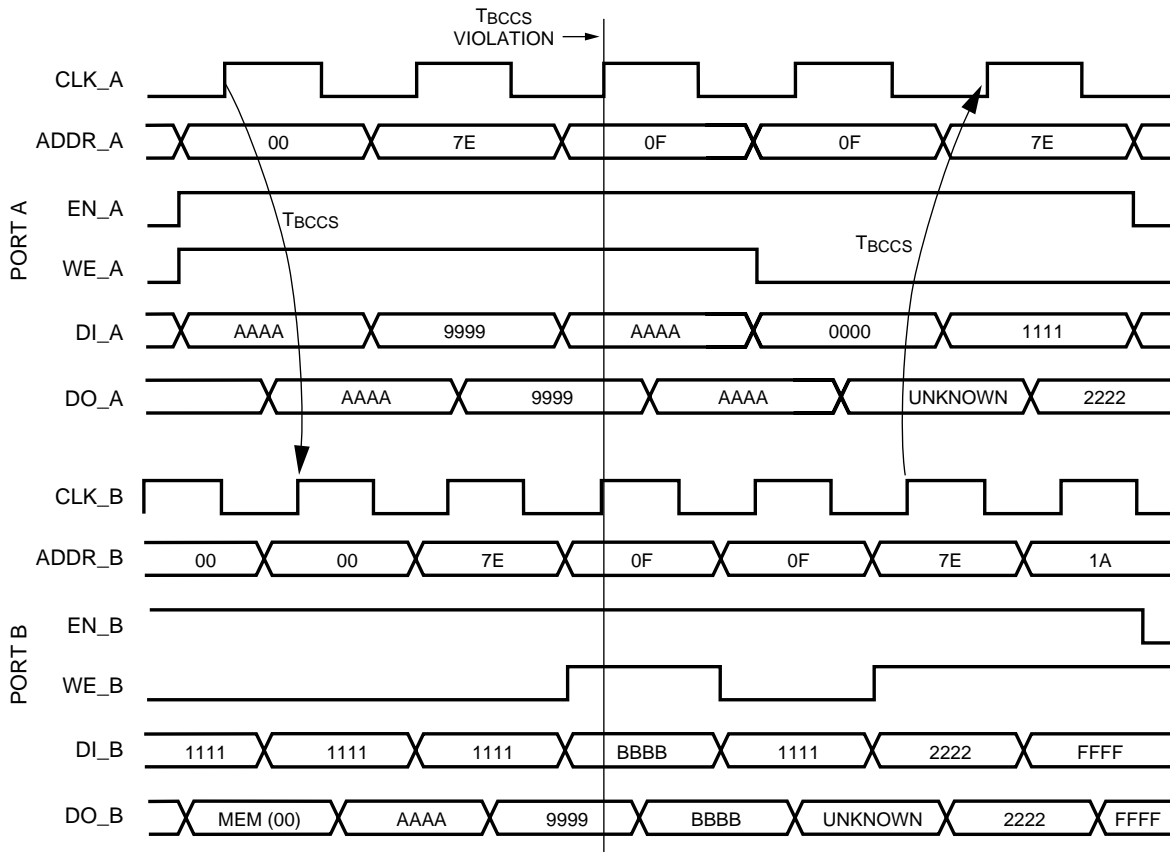
T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.



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Figure 33: Timing Diagram for Single Port Block SelectRAM+ Memory



ds022_035_121399

Figure 34: Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. The DOA bus reflects the recently written value by Port B.

Initialization

The Block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in [Table 13](#). Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The Block SelectRAM+ structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys `dc_script`. The `translate_off` statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 13: RAM Initialization Properties

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 1536
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

Initialization in Verilog and Synopsys

The Block SelectRAM+ structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a `defparam` to pass the initialization. The Synopsys FPGA compiler does not presently support `defparam`. The initialization values instead attach as attributes to the RAM by a built-in Synopsys `dc_script`. The `translate_off` statement stops synthesis translation of the `defparam` statements. The following code illustrates a module that employs these techniques.

Block Memory Generation

The CoreGen program generates memory structures using the Block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

Using Versatile I/O

The Spartan-II FPGA family includes a highly configurable, high-performance I/O resource, called Versatile I/O to provide support for a wide variety of I/O standards. The Versatile I/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and Versatile I/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. Versatile I/O, the revolutionary input/output resources of Spartan-II devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Spartan-II Versatile I/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each Versatile I/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features,

system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in [Table 14](#), each buffer type can support a variety of voltage requirements.

Table 14: Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTTL	3.3	3.3	N/A	N/A
LVC MOS2	2.5	2.5	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI33_5	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance Jedec website at: <http://www.jedec.org>

LVTTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTTL input buffer and a Push-Pull output buffer. This

standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVC MOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower, or LVC MOS2 standard is an extension of the LVC MOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both

classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of Versatile I/O features. Most of these symbols represent variations of the five generic Versatile I/O symbols.

- IBUF (input buffer)
- IBUG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF symbol appears in [Figure 35](#). The extension to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTTL when the generic IBUF has no specified extension.

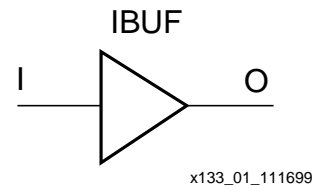


Figure 35: Input Buffer (IBUF) Symbols

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVC MOS2
- IBUF_PCI33_3
- IBUF_PCI33_5
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I

- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP

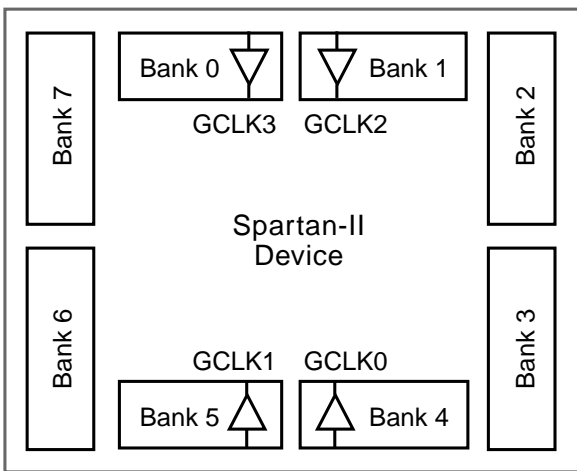
When the IBUF symbol supports an I/O standard such as LVTTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V-tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO} < 2V$), the input buffer is not 5V-tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 15 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.



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Figure 36: I/O Banks

Table 15: Xilinx Input Standards Compatibility Requirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG symbol can only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic IBUFG symbol appears in Figure 37.

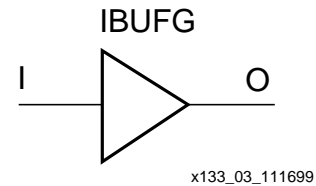


Figure 37: Global Clock Input Buffer (IBUFG) Symbol

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI33_5
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in [Figure 38](#).

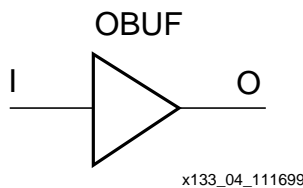


Figure 38: Output Buffer (OBUF) Symbol

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

The LVTTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTTL output buffers have selectable drive strengths.

The format for LVTTTL OBUF symbol names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12

- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI33_5
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. [Table 16](#) summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 16: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards which share compatible V_{CCO} may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO} .
V_{CCO}	Compatible Standards
3.3	LVTTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in [Figure 39](#), typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

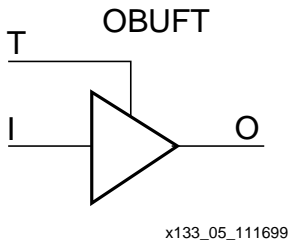
The LVTTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTTL 3-state output buffers have selectable drive strengths.

The format for LVTTTL OBUFT symbol names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).



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Figure 39: 3-State Output Buffer Symbol (OBUFT)

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI33_5
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP

The Versatile I/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the

appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTTL input buffer and slew rate limited LVTTTL with 12 mA drive strength for the output buffer.

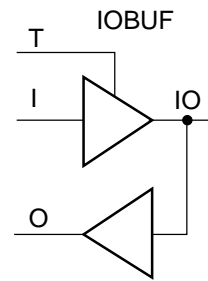
The LVTTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTTL IOBUF symbol names is as follows.

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).



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Figure 40: Input/Output Buffer Symbol (IOBUF)

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16

- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI33_5
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP

When the IOBUF symbol supports an I/O standard such as LVTTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V-tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO} < 2V$), the input buffer is not 5V-tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See [Figure 36 on page 33](#) for a representation of the Spartan-II I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the

appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O symbol with the location constraint LOC attached to the Versatile I/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form.

```
LOC=A42
```

```
LOC=P37
```

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

```
SLEW=SLOW
```

```
SLEW=FAST
```

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTTL output buffers (OBUF, OBUFT, and IOBUF), the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See [Figure 36 on page 33](#) for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined V_{CCO} supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTTL, LVCMOS2, PCI133_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short dis-

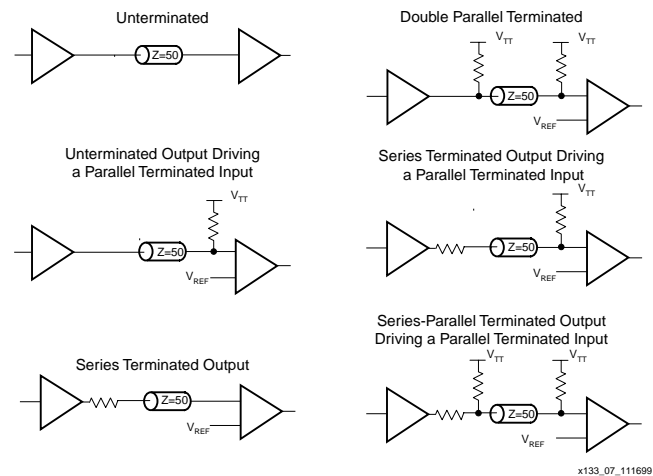


Figure 41: Overview of Standard Input and Output Termination Methods

tance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques.

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in [Figure 41](#).

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 17 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 18 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

Table 17: Guidelines for Max. Number of Simultaneously Switching Outputs per Power/Ground Pair

Standard	Package	
	CS, FG	PQ, TQ, VQ
LVTTTL Slow Slew Rate, 2 mA drive	68	36
LVTTTL Slow Slew Rate, 4 mA drive	41	20
LVTTTL Slow Slew Rate, 6 mA drive	29	15
LVTTTL Slow Slew Rate, 8 mA drive	22	12
LVTTTL Slow Slew Rate, 12 mA drive	17	9
LVTTTL Slow Slew Rate, 16 mA drive	14	7
LVTTTL Slow Slew Rate, 24 mA drive	9	5
LVTTTL Fast Slew Rate, 2 mA drive	40	21
LVTTTL Fast Slew Rate, 4 mA drive	24	12
LVTTTL Fast Slew Rate, 6 mA drive	17	9
LVTTTL Fast Slew Rate, 8 mA drive	13	7
LVTTTL Fast Slew Rate, 12 mA drive	10	5
LVTTTL Fast Slew Rate, 16 mA drive	8	4
LVTTTL Fast Slew Rate, 24 mA drive	5	3
LVC MOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

Note:

1. This analysis assumes a 35 pF load for each output.

Table 18: Effective Output Power/Ground Pairs for Spartan-II Devices

Pkg.	Spartan-II Devices					
	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150	XC2S200
VQ100	8	8	-	-	-	-
CS144	12	12	-	-	-	-
TQ144	12	12	12	12	-	-
PQ208	-	16	16	16	16	16
FG256	-	-	16	16	16	16
FG456	-	-	-	48	48	48

Application Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the Versatile I/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 19 lists DC voltage specifications.

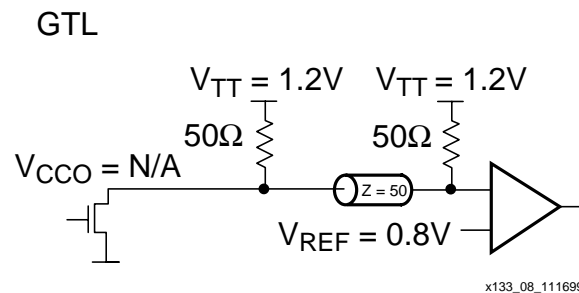


Figure 42: Terminated GTL

Table 19: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}^{-1}$	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Note:

- N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 20.

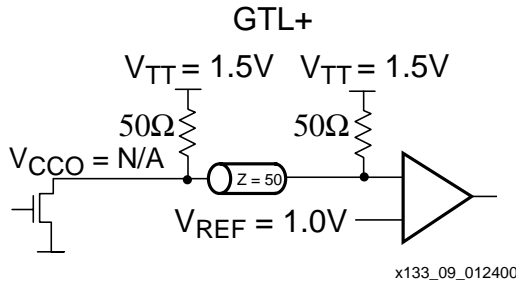


Figure 43: Terminated GTL+

Table 20: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}^{-1}$	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Note:

- N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 44. A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45.

HSTL Class I

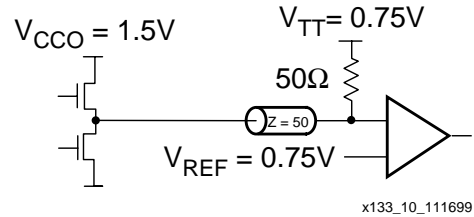


Figure 44: Terminated HSTL Class I

Table 21: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

HSTL Class III

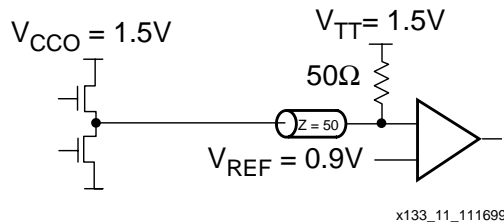


Figure 45: Terminated HSTL Class III

Table 22: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
$V_{REF}^{(1)}$	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note:

- Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL_IV appears in **Figure 46**.

HSTL Class IV

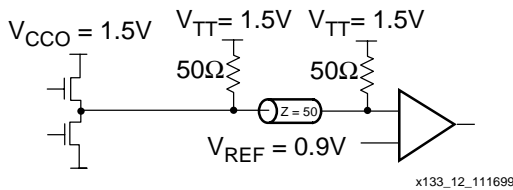


Figure 46: Terminated HSTL Class IV

Table 23: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Note:

- Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in **Figure 47**. DC voltage specifications appear in **Table 24**.

SSTL3 Class I

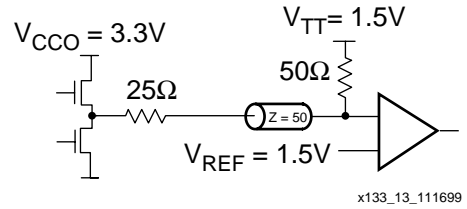


Figure 47: Terminated SSTL3 Class I

Table 24: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} = V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

- V_{IH} maximum is $V_{CCO} + 0.3$.
- V_{IL} minimum does not conform to the formula.

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in **Figure 48**. DC voltage specifications appear in **Table 25**.

SSTL3 Class II

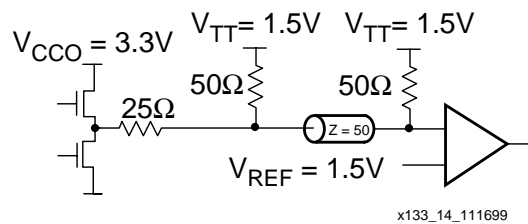


Figure 48: Terminated SSTL3 Class II

Table 25: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} = V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	-16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:

1. V_{IH} maximum is $V_{CCO} + 0.3$
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 49. DC voltage specifications appear in Table 26.

SSTL2 Class I

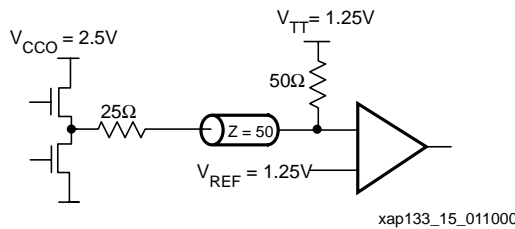


Figure 49: Terminated SSTL2 Class I

Table 26: SSTL2_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0 ⁽²⁾
$V_{IL} = V_{REF} - 0.18$	-0.3 ⁽³⁾	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL} = V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	-7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is $V_{CCO} + 0.3$.
3. V_{IL} minimum does not conform to the formula.

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 50. DC voltage specifications appear in Table 27.

SSTL2 Class II

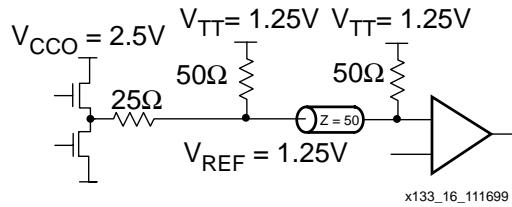


Figure 50: Terminated SSTL2 Class II

Table 27: SSTL2_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0 ⁽²⁾
$V_{IL} = V_{REF} - 0.18$	-0.3 ⁽³⁾	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	-15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is $V_{CCO} + 0.3$.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 28.

CTT

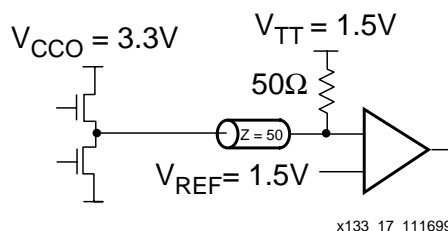


Figure 51: Terminated CTT

Table 28: CTT Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.05 ⁽¹⁾	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} = V_{REF} - 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in [Table 29](#).

Table 29: PCI33_3 and PCI66_3 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	$V_{CCO} + 0.5$
$V_{IL} = 0.3 \times V_{CCO}$	-0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Note:

1. Tested according to the relevant specification.

PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in [Table 30](#).

Table 30: PCI33_5 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.425	1.5	5.5
V_{IL}	-0.5	1.0	1.05
V_{OH}	2.4	-	-
V_{OL}	-	-	0.55
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Note:

1. Tested according to the relevant specification.

LVTTL

LVTTL requires no termination. DC voltage specifications appear in [Table 31](#).

Table 31: LVTTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	3.6
V_{IL}	-0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-24	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note:

1. V_{OL} and V_{OH} for lower drive currents sample tested.

LVC MOS2

LVC MOS2 requires no termination. DC voltage specifications appear in [Table 32](#).

Table 32: LVC MOS2 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	3.6
V_{IL}	-0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-12	-	-
I_{OL} at V_{OL} (mA)	12	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in [Table 33](#).

Table 33: AGP-2X Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}^{(1)}$	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-

Table 33: AGP-2X Voltage Specifications

Parameter	Min	Typ	Max
$V_{IL} = V_{REF} - 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL} at V_{OL} (mA)	Note 2	-	-

Notes:

1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

Spartan-II DC Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-II Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CCINT}	Supply voltage relative to GND	-0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND	-0.5 to 4.0	V
V_{REF}	Input Reference Voltage	-0.5 to 3.6	V
V_{IN}	Input voltage relative to GND	Using V_{REF}	-0.5 to 3.6
		Internal threshold	-0.5 to 5.5
V_{TS}	Voltage applied to 3-state output	-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1V to 2.375V	50	ms
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temp. (10s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- Power supplies may turn on in any order.
- For extended periods (e.g., longer than a day), V_{IN} should not exceed V_{CCO} by more than 3.6V.

Spartan-II Recommended Operating Conditions

Symbol	Description	Min	Max	Units	
V_{CCINT}	Supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	2.5 - 5%	2.5 + 5%	V
	Supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	2.5 - 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial		3.6	V
	Supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial		3.6	V
T_{IN}	Input signal transition time		250	ns	

Notes:

- Correct operation is guaranteed with a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} -10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50 mV reduction in V_{CCINT} below the specified range.
- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Input and output measurement threshold is ~50% of V_{CC} .

Spartan-II DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)	2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)			mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)			mA
I_{REF}	V_{REF} current per V_{REF} pin		20	μ A
I_L	Input or output leakage current	-10	+10	μ A
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8 pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$ (sample tested)	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.6V$ (sample tested)	Note 2	0.15	mA

Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Spartan-II DC Input and Output levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTTL (Note 1)	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
LVCOS2	-0.5	0.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3V	-0.5	44% V_{CCINT}	60% V_{CCINT}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	-0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	N/A	40	N/A
GTL+	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	N/A	36	N/A
HSTL I	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL III	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV	-0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
SSTL3 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	-8
SSTL3 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	-16
SSTL2 I	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.5$	$V_{REF} + 0.5$	7.6	-7.6
SSTL2 II	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.5$	$V_{REF} + 0.5$	15.2	-15.2
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

Spartan-II Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

Spartan-II Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Symbol	Description	Speed Grade		Units	
		Device	-6		-5
T _{ICKOFDLL}	LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Output Delay Adjustments.	XC2S15		3.3	ns, min
		XC2S30		3.3	ns, min
		XC2S50		3.3	ns, min
		XC2S100		3.3	ns, min
		XC2S150		3.3	ns, min
		XC2S200			ns, min

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see [Table 34](#) and [Table 35](#).
3. DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Symbol	Description	Speed Grade		Units	
		Device	-6		-5
T _{ICKOF}	LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>without</i> DLL. For data <i>output</i> with different standards, adjust delays with the values shown in Output Delay Adjustments.	XC2S15		5.1	ns, min
		XC2S30		5.1	ns, min
		XC2S50		5.2	ns, min
		XC2S100		5.2	ns, min
		XC2S150		5.2	ns, min
		XC2S200			ns, min

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see [Table 34](#) and [Table 35](#).

Spartan-II Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *with* DLL

Symbol	Description	Speed Grade		Units	
		Device	-6		-5
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.					
T_{PSDLL} / T_{PHDLL}	No Delay Global Clock and IFF, with DLL	XC2S15		1.9 / 0	ns, min
		XC2S30		1.9 / 0	ns, min
		XC2S50		1.9 / 0	ns, min
		XC2S100		2.0 / 0	ns, min
		XC2S150		2.0 / 0	ns, min
		XC2S200			ns, min

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL

Symbol	Description	Speed Grade		Units	
		Device	-6		-5
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.					
T_{PSFD} / T_{PHFD}	No Delay Global Clock and IFF, without DLL	XC2S15		2.8 / 0	ns, min
		XC2S30		2.8 / 0	ns, min
		XC2S50		2.8 / 0	ns, min
		XC2S100		2.8 / 0	ns, min
		XC2S150		2.9 / 0	ns, min
		XC2S200			ns, min

Notes:

1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Spartan-II IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 49.

Symbol	Description	Device	Speed Grade		Units
			-6	-5	
Propagation Delays					
T_{IOPI}	Pad to I output, no delay	All		1.0	ns, max.
T_{IOPID}	Pad to I output, with delay	XC2S15		1.8	ns, max
		XC2S30		1.8	ns, max
		XC2S50		1.8	ns, max
		XC2S100		1.8	ns, max
		XC2S150		1.8	ns, max
		XC2S200			ns, max
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All		1.9	ns, max.
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S15		4.5	ns, max
		XC2S30		4.5	ns, max
		XC2S50		4.5	ns, max
		XC2S100		4.5	ns, max
		XC2S150		4.6	ns, max
		XC2S200			ns, max
Sequential Delays					
T_{IOCKIQ}	Clock CLK to output IQ			0.8	ns, max
Setup / Hold Times with Respect to Clock CLK					
T_{IOPICK} / T_{IOICKP}	Pad, no delay			1.9 / 0	ns, max.
$T_{IOPICKD} / T_{IOICKPD}$	Pad, with delay (Note 1)	XC2S15		4.4 / 0	ns, max
		XC2S30		4.4 / 0	ns, max
		XC2S50		4.4 / 0	ns, max
		XC2S100		4.4 / 0	ns, max
		XC2S150		4.6 / 0	ns, max
		XC2S200			ns, max
$T_{IOICECK} / T_{IOICKICE}$	ICE input			0.9 / 0.01	ns, max.
Set/Reset Delays					
$T_{IOSRCKI}$	SR input (IFF, synchronous)			1.2	ns, max.
T_{IOSRIQ}	SR input to IQ (asynchronous)			1.7	ns, max.
T_{GSRQ}	GSR to output IQ			11.7	ns, max.

Note:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see [Table 35](#).

IOB Input Switching Characteristics Standard Adjustments

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTTL		0	ns
$T_{ILVCMOS2}$		LVCMOS2		-0.05	ns
$T_{I PCI33_3}$		PCI, 33 MHz, 3.3V		-0.13	ns
$T_{I PCI33_5}$		PCI, 33 MHz, 5.0V		0.30	ns
$T_{I PCI66_3}$		PCI, 66 MHz, 3.3V		-0.13	ns
T_{IGTL}		GTL		0.24	ns
T_{IGTLP}		GTL+		0.13	ns
T_{IHSTL}		HSTL		0.04	ns
T_{ISSTL2}		SSTL2		-0.09	ns
T_{ISSTL3}		SSTL3		-0.05	ns
T_{ICTT}		CTT		0.02	ns
T_{IAGP}		AGP		-0.07	ns

Note:

1. Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see [Table 35](#).

Spartan-II IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in “IOB Output Switching Characteristics Standard Adjustments” on page 51.

Symbol	Description	Speed Grade		Units
		-6	-5	
Propagation Delays				
T_{IOOP}	O input to Pad		3.4	ns, max
T_{IOOLP}	O input to Pad via transparent latch		3.9	ns, max
3-state Delays				
T_{IOTHZ}	T input to Pad high-impedance		2.3	ns, max
T_{IOTON}	T input to valid data on Pad		3.6	ns, max
$T_{IOTLPHZ}$	T input to Pad high-impedance via transparent latch		2.8	ns, max
$T_{IOTLPON}$	T input to valid data on Pad via transparent latch		4.1	ns, max
T_{GTS}	GTS to Pad high impedance		5.9	ns, max
Sequential Delays				
T_{IOCKP}	Clock CLK to Pad		3.4	ns, max
T_{IOCKHZ}	Clock CLK to Pad high-impedance (synchronous)		2.7	ns, max
T_{IOCKON}	Clock CLK to valid data on Pad (synchronous)		4.0	ns, max
Setup Times before Clock CLK				
T_{IOOCK} / T_{IOCKO}	O input		1.3 / 0	ns, max
$T_{IOOCECK} / T_{IOCKOCE}$	OCE input		0.9 / 0	ns, max
$T_{IOSRCKO} / T_{IOCKOSR}$	SR input (OFF)		1.3 / 0	ns, max
T_{IOTCK} / T_{IOCKT}	3-state Setup Times , T inpuh		0.9 / 0	ns, max
$T_{IOTCECK} / T_{IOCKTCE}$	3-state Setup Times , TCE input		1.0 / 0	ns, max
$T_{IOSRCKT} / T_{IOCKTSR}$	3-state Setup Times ,SR input (TFF)		1.2 / 0	ns, max
Set/Reset Delays				
T_{IOSRP}	SR input to Pad (asynchronous)		4.4	ns, max
$T_{IOTSRHZ}$	SR input to Pad high impedance (asynchronous)		3.7	ns, max
$T_{IOTSRON}$	SR input to valid data on Pad (asynchronous)		4.9	ns, max
T_{IOGSRQ}	GSR to Pad		11.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Tri-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Output Delay Adjustments					
T _{OLVTTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	LVTTTL, Slow, 2 mA		16.9	ns
T _{OLVTTTL_S4}		4 mA		8.6	ns
T _{OLVTTTL_S6}		6 mA		5.5	ns
T _{OLVTTTL_S8}		8 mA		3.5	ns
T _{OLVTTTL_S12}		12 mA		2.2	ns
T _{OLVTTTL_S16}		16 mA		2.0	ns
T _{OLVTTTL_S24}		24 mA		1.5	ns
T _{OLVTTTL_F2}		LVTTTL, Fast, 2 mA		15.0	ns
T _{OLVTTTL_F4}		4 mA		6.1	ns
T _{OLVTTTL_F6}		6 mA		3.6	ns
T _{OLVTTTL_F8}		8 mA		1.2	ns
T _{OLVTTTL_F12}		12 mA		0	ns
T _{OLVTTTL_F16}		16 mA		-0.15	ns
T _{OLVTTTL_F24}		24 mA		-0.23	ns
T _{OLVCMOS2}		LVCNOS2		0.18	ns
T _{OPCI33_3}		PCI, 33 MHz, 3.3V		2.9	ns
T _{OPCI33_5}	PCI, 33 MHz, 5.0V		3.5	ns	
T _{OPCI66_3}	PCI, 66 MHz, 3.3V		-0.42	ns	
T _{OGTL}	GTL		0.7	ns	
T _{OGTLP}	GTL+		1.1	ns	
T _{OHSTL_I}	HSTL I		-0.54	ns	
T _{OHSTL_III}	HSTL III		-1.0	ns	
T _{OHSTL_IV}	HSTL IV		-1.1	ns	
T _{OSSTL3_I}	SSTL3 I		-0.54	ns	
T _{OSSTL3_II}	SSTL3 II		-1.1	ns	
T _{OSSTL2_I}	SSTL2 I		-0.54	ns	
T _{OSSTL2_II}	SSTL2 II		-1.0	ns	
T _{OCTT}	CTT		-0.6	ns	
T _{OAGP}	AGP		-1.0	ns	

Notes:

- Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTTL. For other I/O standards and different loads, see [Table 34](#) and [Table 35](#).

Calculation of $T_{i\text{oop}}$ as a Function of Capacitance

$T_{i\text{oop}}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{i\text{oop}}$ were based on the standard capacitive load (C_{sl}) for each I/O standard as listed in [Table 34](#).

For other capacitive loads, use the formulas below to calculate the corresponding $T_{i\text{oop}}$.

$$T_{i\text{oop}} = T_{i\text{oop}} + T_{\text{opadjust}} + (C_{\text{load}} - C_{\text{sl}}) * f_l$$

Where:

T_{opadjust} is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 34: Constants for Calculating $T_{i\text{oop}}$

Standard	C_{sl} (pF)	f_l (ns/pF)
LVTTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTTL Slow Slew Rate, 24 mA drive	35	0.048
LVC MOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

- I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP179 for appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Table 35: Delay Measurement Methodology

Standard	$V_L^{(1)}$	$V_H^{(1)}$	Meas. Point	$V_{\text{REF}}^{(2)}$ (Typ)
LVTTTL	0	3	1.4	-
LVC MOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{\text{REF}} - 0.2$	$V_{\text{REF}} + 0.2$	V_{REF}	0.80
GTL+	$V_{\text{REF}} - 0.2$	$V_{\text{REF}} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	V_{REF}	0.90
SSTL3 I and II	$V_{\text{REF}} - 1.0$	$V_{\text{REF}} + 1.0$	V_{REF}	1.5
SSTL2 I and II	$V_{\text{REF}} - 0.75$	$V_{\text{REF}} + 0.75$	V_{REF}	1.25
CTT	$V_{\text{REF}} - 0.2$	$V_{\text{REF}} + 0.2$	V_{REF}	1.5
AGP	$V_{\text{REF}} - (0.2xV_{\text{CCO}})$	$V_{\text{REF}} + (0.2xV_{\text{CCO}})$	V_{REF}	Per AGP Spec

Notes:

- Input waveform switches between V_L and V_H .
- Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.
- I/O parameter measurements are made with the capacitance values shown in [Table 34](#). See Xilinx application note XAPP179 for appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Spartan-II Clock Distribution Guidelines

Symbol	Description	Device	Speed Grade		Units
			-6	-5	
GCLK Clock Skew					
T _{GSKWIOB}	Global Clock Skew between IOB flip-flops	XC2S15		0.14	ns, max
		XC2S30		0.14	ns, max
		XC2S50		0.14	ns, max
		XC2S100		0.15	ns, max
		XC2S150		0.15	ns, max
		XC2S200			ns, max

Note:

1. These clock-distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Spartan-II Clock Distribution Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
GCLK IOB and Buffer				
T _{GPIIO}	Global Clock PAD to output.		0.8	ns, max
T _{GIO}	Global Clock Buffer I input to O output		0.9	ns, max

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
F _{CLKINHF}	Input Clock Frequency (CLKDLLHF)			60	180	MHz
F _{CLKINLF}	Input Clock Frequency (CLKDLL)			25	90	MHz
T _{DLLPWHF}	Input Clock Pulse Width (CLKDLLHF)			2.4	-	ns
T _{DLLPWL}	Input Clock Pulse Width (CLKDLL)			3.0	-	ns

Note:

1. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Symbol	Description	F _{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T _{IPTOL}	Input Clock Period Tolerance		-	1.0	-	1.0	ns
T _{IJTCC}	Input Clock Jitter Tolerance (Cycle to Cycle)		-	±150	-	±300	ps
T _{LOCK}	Time Required for DLL to Acquire Lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T _{OJITCC}	Output Jitter (cycle-to-cycle) for any DLL Clock Output ¹		-	±60	-	±60	ps
T _{PHIO}	Phase Offset between CLKIN and CLKO ²		-	±100	-	±100	ps
T _{PHOO}	Phase Offset between Clock Outputs on the DLL ³		-	±140	-	±140	ps
T _{PHIOM}	Maximum Phase Difference between CLKIN and CLKO ⁴		-	±160	-	±160	ps
T _{PHOOM}	Maximum Phase Difference between Clock Outputs on the DLL ⁵		-	±200	-	±200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN and CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output Jitter and Phase Offset between any two DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).
6. All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Spartan-II CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{ILO}	4-input function: F/G inputs to X/Y outputs		0.7	ns, max
T_{IF5}	5-input function: F/G inputs to F5 output		0.8	ns, max
T_{IF5X}	5-input function: F/G inputs to X output		0.9	ns, max
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX		1.1	ns, max
T_{F5INY}	6-input function: F5IN input to Y output		0.39	ns, max
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs		0.8	ns, max
T_{BYYB}	BY input to YB output		0.7	ns, max
Sequential Delays				
T_{CKO}	FF Clock CLK to XQ/YQ outputs		1.3	ns, max
T_{CKLO}	Latch Clock CLK to XQ/YQ outputs		1.5	ns, max
Setup Times before Clock CLK				
T_{ICK} / T_{CKI}	4-input function: F/G Inputs		1.5 / 0	ns, max
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs		1.6 / 0	ns, max
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input		1.1 / 0	ns, max
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX		1.8 / 0	ns, max
T_{DICK} / T_{CKDI}	BX/BY inputs		0.8 / 0	ns, max
T_{CECK} / T_{CKCE}	CE input		0.9 / 0	ns, max
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)		0.8 / 0	ns, max
Clock CLK				
T_{CH}	Minimum Pulse Width, High		1.9	ns, max
T_{CL}	Minimum Pulse Width, Low		1.9	ns, max
Set/Reset				
T_{RPW}	Minimum Pulse Width, SR/BY inputs		3.1	ns, max
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)		1.3	ns, max
T_{IOGSRQ}	Delay from GSR to XQ/YQ outputs		11.7	ns, max
F_{TOG}	Toggle Frequency (for export control)		276.9	MHz

Note:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Spartan-II CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{OPX}	F operand inputs to X via XOR		0.9	ns, max
T_{OPXB}	F operand input to XB output		1.3	ns, max
T_{OPY}	F operand input to Y via XOR		1.9	ns, max
T_{OPYB}	F operand input to YB output		1.8	ns, max
T_{OPCYF}	F operand input to COUT output		1.4	ns, max
T_{OPGY}	G operand inputs to Y via XOR		1.1	ns, max
T_{OPGYB}	G operand input to YB output		2.0	ns, max
T_{OPCYG}	G operand input to COUT output		1.5	ns, max
T_{BXCX}	BX initialization input to COUT		1.0	ns, max
T_{CINX}	CIN input to X output via XOR		0.49	ns, max
T_{CINXB}	CIN input to XB		0.05	ns, max
T_{CINY}	CIN input to Y via XOR		0.6	ns, max
T_{CINYB}	CIN input to YB		0.55	ns, max
T_{BYP}	CIN input to COUT output		0.11	ns, max
Multiplier Operation				
T_{FANDXB}	F1/2 operand inputs to XB output via AND		0.43	ns, max
T_{FANDYB}	F1/2 operand inputs to YB output via AND		1.0	ns, max
T_{FANDCY}	F1/2 operand inputs to COUT output via AND		0.52	ns, max
T_{GANDYB}	G1/2 operand inputs to YB output via AND		0.6	ns, max
T_{GANDCY}	G1/2 operand inputs to COUT output via AND		0.16	ns, max
Setup / Hold Times with Respect to Clock CLK				
T_{CCKX} / T_{CKCX}	CIN input to FFX		1.2 / 0	ns, max
T_{CCKY} / T_{CKCY}	CIN input to FFY		1.3 / 0	ns, max

Note:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Spartan-II CLB SelectRAM Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Sequential Delays (includes Shift-Register Mode)				
T_{SHCKO}	Clock CLK to X/Y outputs (WE active)		2.8	ns, max
Setup and Hold Times with Respect to Clock CLK				
T_{AS} / T_{AH}	F/G address inputs		0.7 / 0	ns, max
T_{DS} / T_{DH}	BX/BY data inputs (DIN)		0.8 / 0	ns, max
T_{WS} / T_{WH}	CE input (WS)		1.0 / 0	ns, max
Shift-Register Mode				
T_{SHDICK}	BX/BY data inputs (DIN)		0.8	ns, max
T_{SHCECK}	BX/BY data inputs (DIN)		1.0	ns, max
Clock CLK				
T_{WPH}	Minimum Pulse Width, High		2.9	ns, max
T_{WPL}	Minimum Pulse Width, Low		2.9	ns, max
T_{WC}	Minimum clock period to meet address write cycle time		5.8	ns, max
Shift-Register Mode				
T_{SRPH}	Minimum Pulse Width, High		2.9	ns, max
T_{SRPL}	Minimum Pulse Width, Low		2.9	ns, max

Note:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Spartan-II Block RAM Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Sequential Delays				
T_{BCKO}	Clock CLK to DOUT output		4.0	ns, max
Setup and Hold Times with Respect to Clock CLK				
T_{BACK} / T_{BCKA}	ADDR inputs		1.4 / 0	ns, max
T_{BDCK} / T_{BCKD}	DIN inputs		1.4 / 0	ns, max
T_{BECK} / T_{BCKE}	EN inputs		3.2 / 0	ns, max
T_{BRCK} / T_{BCKR}	RST input		2.9 / 0	ns, max
T_{BWCK} / T_{BCKW}	WEN input		2.8 / 0	ns, max
Clock CLK				
T_{BPWH}	Minimum Pulse Width, High		1.9	ns, max
T_{BPWL}	Minimum Pulse Width, Low		1.9	ns, max
T_{BCCS}	CLKA -> CLKB setup time for different ports			ns, max

Note:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

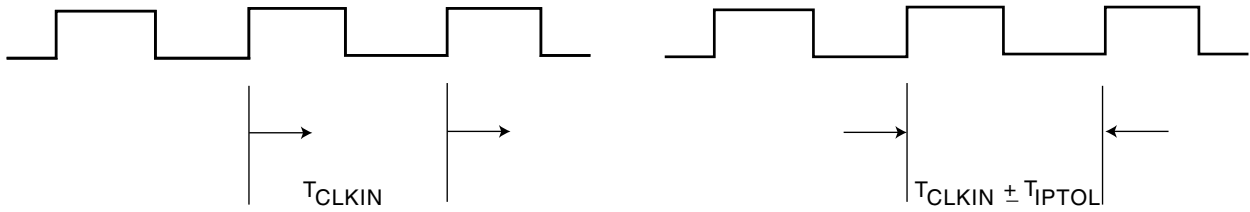
Spartan-II TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{IO}	IN input to OUT output		0	ns, max
T_{OFF}	TRI input to OUT output high-impedance		0.11	ns, max
T_{ON}	Tri input to valid data on OUT output		0.11	ns, max

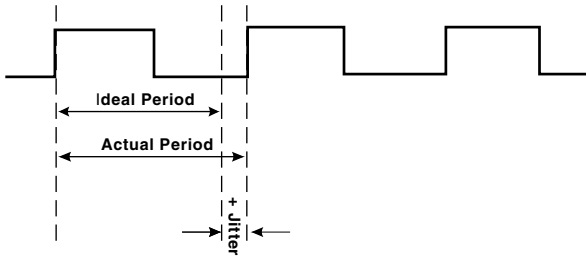
Spartan-II JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
Combinatorial Delays				
T_{TAPTCK}	TMS and TDI Setup times before TCK		4.0	ns, max
T_{TCKTAP}	TMS and TDI Hold times after TCK		2.0	ns, max
T_{TCKTDO}	Output delay from clock TCK to output TDO		11.0	ns, max
f_{TCK}	Maximum TCK clock frequency		33	MHz, max

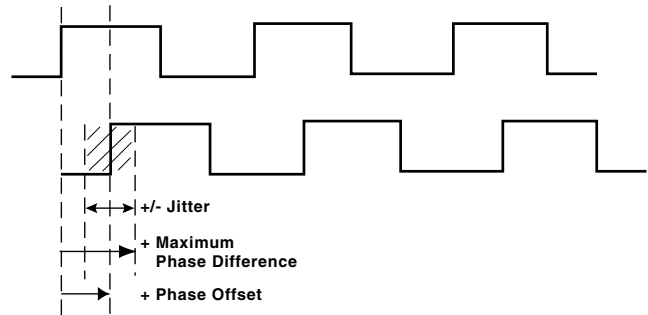
Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.



Phase Offset and Maximum Phase Difference



ds003_20c_110399

Figure 52: Frequency Tolerance and Clock Jitter

Pin Definitions

Table 36: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectRAM and slave-serial modes, and output in master-serial mode
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input	In Slave Parallel mode, D0-7 are configuration data input pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{\text{CS}}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground
$\overline{\text{PWDN}}$	Yes	Input	The pin is held High during normal operation and pulled Low for power down mode.
STATUS	Yes	Output	The pin goes Low when the part is in power down mode and is released High when part is ready to resume normal operation.

Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan-II device. They follow the pad locations around the die, and include boundary scan register locations.

XC2S15 Device Pinouts

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
GND	-	P1	P143	A1	-
TMS	-	P2	P142	B1	-
I/O	7	P3	P141	C2	77
I/O	7	-	P140	C1	80
I/O, V _{REF}	7	P4	P139	D4	83
I/O	7	P5	P137	D2	86
I/O	7	P6	P136	D1	89
GND	-	-	P135	E4	-
I/O	7	P7	P134	E3	92
I/O	7	-	P133	E2	95
I/O, V _{REF}	7	P8	P132	E1	98
I/O	7	P9	P131	F4	101
I/O	7	-	P130	F3	104
I/O, IRDY	7	P10	P129	F2	107
GND	-	P11	P128	F1	-
V _{CCO}	7	P12	P127	G2	-
V _{CCO}	6	P12	P127	G2	-
I/O, TRDY	6	P13	P126	G1	110
V _{CCINT}	-	P14	P125	G3	-
I/O	6	-	P124	G4	113
I/O	6	P15	P123	H1	116
I/O, V _{REF}	6	P16	P122	H2	119
I/O	6	-	P121	H3	122
I/O	6	P17	P120	H4	125
GND	-	-	P119	J1	-
I/O	6	P18	P118	J2	128
I/O	6	P19	P117	J3	131
I/O, V _{REF}	6	P20	P115	K1	134
I/O	6	-	P114	K2	137
I/O	6	P21	P113	K3	140
I/O	6	P22	P112	L1	143
M1	-	P23	P111	L2	146
GND	-	P24	P110	L3	-
M0	-	P25	P109	M1	147
V _{CCO}	6	P26	P108	M2	-
V _{CCO}	5	P26	P107	N1	-
M2	-	P27	P106	N2	148
PWDN	-	P28	P105	M3	-
STATUS	5	P29	P104	N3	-
I/O	5	-	P103	K4	155
I/O, V _{REF}	5	P30	P102	L4	158
I/O	5	P31	P100	N4	161
I/O	5	P32	P99	K5	164
GND	-	-	P98	L5	-
V _{CCINT}	-	P33	P97	M5	-
I/O	5	-	P96	N5	167
I/O	5	-	P95	K6	170
I/O, V _{REF}	5	P34	P94	L6	173
I/O	5	-	P93	M6	176
V _{CCINT}	-	P35	P92	N6	-

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
GCK1	-	P36	P91	M7	185
V _{CCO}	5	P37	P90	N7	-
V _{CCO}	4	P37	P90	N7	-
GND	-	P38	P89	L7	-
GCK0	-	P39	P88	K7	186
I/O	4	P40	P87	N8	190
I/O	4	-	P86	M8	193
I/O, V _{REF}	4	P41	P85	L8	196
I/O	4	-	P84	K8	199
I/O	4	-	P83	N9	202
V _{CCINT}	-	P42	P82	M9	-
GND	-	-	P81	L9	-
I/O	4	P43	P80	K9	205
I/O	4	P44	P79	N10	208
I/O, V _{REF}	4	P45	P77	L10	211
I/O	4	-	P76	N11	214
I/O	4	P46	P75	M11	217
I/O	4	P47	P74	L11	220
GND	-	P48	P73	N12	-
DONE	3	P49	P72	M12	223
V _{CCO}	4	P50	P71	N13	-
V _{CCO}	3	P50	P70	M13	-
PROGRAM	-	P51	P69	L12	226
I/O (INIT)	3	P52	P68	L13	227
I/O (D7)	3	P53	P67	K10	230
I/O	3	-	P66	K11	233
I/O, V _{REF}	3	P54	P65	K12	236
I/O	3	P55	P63	J10	239
I/O (D6)	3	P56	P62	J11	242
GND	-	-	P61	J12	-
I/O (D5)	3	P57	P60	J13	245
I/O	3	P58	P59	H10	248
I/O, V _{REF}	3	P59	P58	H11	251
I/O (D4)	3	P60	P57	H12	254
I/O	3	-	P56	H13	257
V _{CCINT}	-	P61	P55	G12	-
I/O, TRDY	3	P62	P54	G13	260
V _{CCO}	3	P63	P53	G11	-
V _{CCO}	2	P63	P53	G11	-
GND	-	P64	P52	G10	-
I/O, IRDY	2	P65	P51	F13	263
I/O	2	-	P50	F12	266
I/O (D3)	2	P66	P49	F11	269
I/O, V _{REF}	2	P67	P48	F10	272
I/O	2	P68	P47	E13	275
I/O (D2)	2	P69	P46	E12	278
GND	-	-	P45	E11	-
I/O (D1)	2	P70	P44	E10	281
I/O	2	P71	P43	D13	284
I/O, V _{REF}	2	P72	P41	D11	287

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
I/O	2	-	P40	C13	290
I/O (DIN, D0)	2	P73	P39	C12	293
I/O (DOUT, BUSY)	2	P74	P38	C11	296
CCLK	2	P75	P37	B13	299
V _{CCO}	2	P76	P36	B12	-
V _{CCO}	2	P76	P35	A13	-
TDO	2	P77	P34	A12	-
GND	-	P78	P33	B11	-
TDI	-	P79	P32	A11	-
I/O (\overline{CS})	1	P80	P31	D10	0
I/O (\overline{WRITE})	1	P81	P30	C10	3
I/O	1	-	P29	B10	6
I/O, V _{REF}	1	P82	P28	A10	9
I/O	1	P83	P27	D9	12
I/O	1	P84	P26	C9	15
GND	-	-	P25	B9	-
V _{CCINT}	-	P85	P24	A9	-
I/O	1	-	P23	D8	18
I/O	1	-	P22	C8	21
I/O, V _{REF}	1	P86	P21	B8	24
I/O	1	-	P20	A8	27
I/O	1	P87	P19	B7	30
GCK2	-	P88	P18	A7	36
GND	-	P89	P17	C7	-
V _{CCO}	1	P90	P16	D7	-
V _{CCO}	0	P90	P16	D7	-

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
GCK3	-	P91	P15	A6	37
V _{CCINT}	-	P92	P14	B6	-
I/O	0	-	P13	C6	44
I/O, V _{REF}	0	P93	P12	D6	47
I/O	0	-	P11	A5	50
I/O	0	-	P10	B5	53
V _{CCINT}	-	P94	P9	C5	-
GND	-	-	P8	D5	-
I/O	0	P95	P7	A4	56
I/O	0	P96	P6	B4	59
I/O, V _{REF}	0	P97	P5	C4	62
I/O	0	-	P4	A3	65
I/O	0	P98	P3	B3	68
TCK	-	P99	P2	C3	-
V _{CCO}	0	P100	P1	A2	-
V _{CCO}	7	P100	P144	B2	-

3/1/00

Additional XC2S15 Package Pins

TQ144

Not Connected Pins					
P42	P64	P78	P101	P116	P138

CS144

Not Connected Pins					
D3	D12	J4	K13	M4	M10

3/1/00

XC2S30 Device Pinouts

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
GND	-	P1	P143	A1	P1	-
TMS	-	P2	P142	B1	P2	-
I/O	7	P3	P141	C2	P3	113
I/O	7	-	P140	C1	P4	116
I/O	7	-	-	-	P5	119
I/O, V _{REF}	7	P4	P139	D4	P6	122
I/O	7	-	P138	D3	P8	125
I/O	7	P5	P137	D2	P9	128
I/O	7	P6	P136	D1	P10	131
GND	-	-	P135	E4	P11	-
V _{CCO}	7	-	-	-	P12	-
I/O	7	P7	P134	E3	P14	134
I/O	7	-	P133	E2	P15	137
I/O	7	-	-	-	P16	140
I/O	7	-	-	-	P17	143
I/O	7	-	-	-	P18	146
GND	-	-	-	-	P19	-
I/O, V _{REF}	7	P8	P132	E1	P20	149
I/O	7	P9	P131	F4	P21	152
I/O	7	-	P130	F3	P22	155
I/O	7	-	-	-	P23	158
I/O, IRDY	7	P10	P129	F2	P24	161
GND	-	P11	P128	F1	P25	-
V _{CCO}	7	P12	P127	G2	P26	-

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
V _{CCO}	6	P12	P127	G2	P26	-
I/O, TRDY	6	P13	P126	G1	P27	164
V _{CCINT}	-	P14	P125	G3	P28	-
I/O	6	-	P124	G4	P29	170
I/O	6	P15	P123	H1	P30	173
I/O, V _{REF}	6	P16	P122	H2	P31	176
GND	-	-	-	-	P32	-
I/O	6	-	-	-	P33	179
I/O	6	-	-	-	P34	182
I/O	6	-	-	-	P35	185
I/O	6	-	P121	H3	P36	188
I/O	6	P17	P120	H4	P37	191
V _{CCO}	6	-	-	-	P39	-
GND	-	-	P119	J1	P40	-
I/O	6	P18	P118	J2	P41	194
I/O	6	P19	P117	J3	P42	197
I/O	6	-	P116	J4	P43	200
I/O, V _{REF}	6	P20	P115	K1	P45	203
I/O	6	-	-	-	P46	206
I/O	6	-	P114	K2	P47	209
I/O	6	P21	P113	K3	P48	212
I/O	6	P22	P112	L1	P49	215
M1	-	P23	P111	L2	P50	218
GND	-	P24	P110	L3	P51	-
M0	-	P25	P109	M1	P52	219

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
V _{CCO}	6	P26	P108	M2	P53	-
V _{CCO}	5	P26	P107	N1	P53	-
M2	-	P27	P106	N2	P54	220
PWDN	-	P28	P105	M3	P55	-
STATUS	5	P29	P104	N3	P56	-
I/O	5	-	P103	K4	P57	227
I/O	5	-	-	-	P58	230
I/O, V _{REF}	5	P30	P102	L4	P59	233
I/O	5	-	P101	M4	P61	236
I/O	5	P31	P100	N4	P62	239
I/O	5	P32	P99	K5	P63	242
GND	-	-	P98	L5	P64	-
V _{CCO}	5	-	-	-	P65	-
V _{CCINT}	-	P33	P97	M5	P66	-
I/O	5	-	P96	N5	P67	245
I/O	5	-	P95	K6	P68	248
I/O	5	-	-	-	P69	251
I/O	5	-	-	-	P70	254
I/O	5	-	-	-	P71	257
GND	-	-	-	-	P72	-
I/O, V _{REF}	5	P34	P94	L6	P73	260
I/O	5	-	-	-	P74	263
I/O	5	-	P93	M6	P75	266
V _{CCINT}	-	P35	P92	N6	P76	-
GCK1	-	P36	P91	M7	P77	275
V _{CCO}	5	P37	P90	N7	P78	-
V _{CCO}	4	P37	P90	N7	P78	-
GND	-	P38	P89	L7	P79	-
GCK0	-	P39	P88	K7	P80	276
I/O	4	P40	P87	N8	P81	280
I/O	4	-	P86	M8	P82	283
I/O	4	-	-	-	P83	286
I/O, V _{REF}	4	P41	P85	L8	P84	289
GND	-	-	-	-	P85	-
I/O	4	-	-	-	P86	292
I/O	4	-	-	-	P87	295
I/O	4	-	-	-	P88	298
I/O	4	-	P84	K8	P89	301
I/O	4	-	P83	N9	P90	304
V _{CCINT}	-	P42	P82	M9	P91	-
V _{CCO}	4	-	-	-	P92	-
GND	-	-	P81	L9	P93	-
I/O	4	P43	P80	K9	P94	307
I/O	4	P44	P79	N10	P95	310
I/O	4	-	P78	M10	P96	313
I/O, V _{REF}	4	P45	P77	L10	P98	316
I/O	4	-	-	-	P99	319
I/O	4	-	P76	N11	P100	322
I/O	4	P46	P75	M11	P101	325
I/O	4	P47	P74	L11	P102	328
GND	-	P48	P73	N12	P103	-
DONE	3	P49	P72	M12	P104	331
V _{CCO}	4	P50	P71	N13	P105	-
V _{CCO}	3	P50	P70	M13	P105	-
PROGRAM	-	P51	P69	L12	P106	334
I/O (INIT)	3	P52	P68	L13	P107	335
I/O (D7)	3	P53	P67	K10	P108	338

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
I/O	3	-	P66	K11	P109	341
I/O	3	-	-	-	P110	344
I/O, V _{REF}	3	P54	P65	K12	P111	347
I/O	3	-	P64	K13	P113	350
I/O	3	P55	P63	J10	P114	353
I/O (D6)	3	P56	P62	J11	P115	356
GND	-	-	P61	J12	P116	-
V _{CCO}	3	-	-	-	P117	-
I/O (D5)	3	P57	P60	J13	P119	359
I/O	3	P58	P59	H10	P120	362
I/O	3	-	-	-	P121	365
I/O	3	-	-	-	P122	368
I/O	3	-	-	-	P123	371
GND	-	-	-	-	P124	-
I/O, V _{REF}	3	P59	P58	H11	P125	374
I/O (D4)	3	P60	P57	H12	P126	377
I/O	3	-	P56	H13	P127	380
V _{CCINT}	-	P61	P55	G12	P128	-
I/O, TRDY	3	P62	P54	G13	P129	386
V _{CCO}	3	P63	P53	G11	P130	-
V _{CCO}	2	P63	P53	G11	P130	-
GND	-	P64	P52	G10	P131	-
I/O, IRDY	2	P65	P51	F13	P132	389
I/O	2	-	-	-	P133	392
I/O	2	-	P50	F12	P134	395
I/O (D3)	2	P66	P49	F11	P135	398
I/O, V _{REF}	2	P67	P48	F10	P136	401
GND	-	-	-	-	P137	-
I/O	2	-	-	-	P138	404
I/O	2	-	-	-	P139	407
I/O	2	-	-	-	P140	410
I/O	2	P68	P47	E13	P141	413
I/O (D2)	2	P69	P46	E12	P142	416
V _{CCO}	2	-	-	-	P144	-
GND	-	-	P45	E11	P145	-
I/O (D1)	2	P70	P44	E10	P146	419
I/O	2	P71	P43	D13	P147	422
I/O	2	-	P42	D12	P148	425
I/O, V _{REF}	2	P72	P41	D11	P150	428
I/O	2	-	-	-	P151	431
I/O	2	-	P40	C13	P152	434
I/O (DIN, D0)	2	P73	P39	C12	P153	437
I/O (DOUT, BUSY)	2	P74	P38	C11	P154	440
CCLK	2	P75	P37	B13	P155	443
V _{CCO}	2	P76	-	-	P156	-
V _{CCO}	2	-	P36	B12	-	-
V _{CCO}	1	-	P35	A13	-	-
TDO	2	P77	P34	A12	P157	-
GND	-	P78	P33	B11	P158	-
TDI	-	P79	P32	A11	P159	-
I/O (CS)	1	P80	P31	D10	P160	0
I/O (WRITE)	1	P81	P30	C10	P161	3
I/O	1	-	P29	B10	P162	6
I/O	1	-	-	-	P163	9
I/O, V _{REF}	1	P82	P28	A10	P164	12
I/O	1	-	-	-	P166	15
I/O	1	P83	P27	D9	P167	18

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
I/O	1	P84	P26	C9	P168	21
GND	-	-	P25	B9	P169	-
V _{CCO}	1	-	-	-	P170	-
V _{CCINT}	-	P85	P24	A9	P171	-
I/O	1	-	P23	D8	P172	24
I/O	1	-	P22	C8	P173	27
I/O	1	-	-	-	P174	30
I/O	1	-	-	-	P175	33
I/O	1	-	-	-	P176	36
GND	-	-	-	-	P177	-
I/O, V _{REF}	1	P86	P21	B8	P178	39
I/O	1	-	-	-	P179	42
I/O	1	-	P20	A8	P180	45
I/O	1	P87	P19	B7	P181	48
GCK2	-	P88	P18	A7	P182	54
GND	-	P89	P17	C7	P183	-
V _{CCO}	1	P90	P16	P7	P184	-
V _{CCO}	0	P90	P16	D7	P184	-
GCK3	-	P91	P15	A6	P185	55
V _{CCINT}	-	P92	P14	B6	P186	-
I/O	0	-	P13	C6	P187	62
I/O	0	-	-	-	P188	65
I/O, V _{REF}	0	P93	P12	D6	P189	68
GND	-	-	-	-	P190	-
I/O	0	-	-	-	P191	71

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
I/O	0	-	-	-	P192	74
I/O	0	-	-	-	P193	77
I/O	0	-	P11	A5	P194	80
I/O	0	-	P10	B5	P195	83
V _{CCINT}	-	P94	P9	C5	P196	-
V _{CCO}	0	-	-	-	P197	-
GND	-	-	P8	D5	P198	-
I/O	0	P95	P7	A4	P199	86
I/O	0	P96	P6	B4	P200	89
I/O	0	-	-	-	P201	92
I/O, V _{REF}	0	P97	P5	C4	P203	95
I/O	0	-	-	-	P204	98
I/O	0	-	P4	A3	P205	101
I/O	0	P98	P3	B3	P206	104
TCK	-	P99	P2	C3	P207	-
V _{CCO}	0	P100	P1	A2	P208	-
V _{CCO}	7	P100	P144	B2	P208	-

3/1/00

Additional XC2S30 Package Pins

PQ208

No connected Pins					
P7	P13	P38	P44	P60	P97
P112	P118	P143	P149	P165	P202

3/1/00

XC2S50 Device Pinouts

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V _{REF}	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V _{CCO}	7	-	P12	V _{CCO} Bank 7*	-
V _{CCINT}	-	-	P13	V _{CCINT} *	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V _{REF}	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V _{CCO}	7	P127	P26	V _{CCO} Bank 7*	-
V _{CCO}	6	P127	P26	V _{CCO} Bank 6*	-
I/O, TRDY	6	P126	P27	J2	218
V _{CCINT}	-	P125	P28	V _{CCINT} *	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V _{REF}	6	P122	P31	J3	233
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V _{CCINT}	-	-	P38	V _{CCINT} *	-
V _{CCO}	6	-	P39	V _{CCO} Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V _{REF}	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	M3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
M0	-	P109	P52	N3	291
V _{CCO}	6	P108	P53	V _{CCO} Bank 6*	-
V _{CCO}	5	P107	P53	V _{CCO} Bank 5*	-
M2	-	P106	P54	R3	292
PWDN	-	P105	P55	P4	-
STATUS	5	P104	P56	R4	-
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	T3	308
GND	-	-	-	GND*	-
I/O, V _{REF}	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323
I/O	5	P99	P63	P6	326
GND	-	P98	P64	GND*	-
V _{CCO}	5	-	P65	V _{CCO} Bank 5*	-
V _{CCINT}	-	P97	P66	V _{CCINT} *	-
I/O	5	P96	P67	R6	329
I/O	5	P95	P68	M7	332
I/O	5	-	P69	N7	338
I/O	5	-	P70	T6	341
I/O	5	-	P71	P7	344
GND	-	-	P72	GND*	-
I/O, V _{REF}	5	P94	P73	P8	347
I/O	5	-	P74	R7	350
I/O	5	-	-	T7	353
I/O	5	P93	P75	T8	356
V _{CCINT}	-	P92	P76	V _{CCINT} *	-
GCK1	-	P91	P77	R8	365
V _{CCO}	5	P90	P78	V _{CCO} Bank 5*	-
V _{CCO}	4	P90	P78	V _{CCO} Bank 4*	-
GND	-	P89	P79	GND*	-
GCK0	-	P88	P80	N8	366
I/O	4	P87	P81	N9	370
I/O	4	P86	P82	R9	373
I/O	4	-	-	N10	376
I/O	4	-	P83	T9	379
I/O, V _{REF}	4	P85	P84	P9	382
GND	-	-	P85	GND*	-
I/O	4	-	P86	M10	385
I/O	4	-	P87	R10	388

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	4	-	P88	P10	391
I/O	4	P84	P89	T10	397
I/O	4	P83	P90	R11	400
V _{CCINT}	-	P82	P91	V _{CCINT} *	-
V _{CCO}	4	-	P92	V _{CCO} Bank 4*	-
GND	-	P81	P93	GND*	-
I/O	4	P80	P94	M11	403
I/O	4	P79	P95	T11	406
I/O	4	P78	P96	N11	409
I/O	4	-	-	R12	412
I/O	4	-	P97	P11	415
I/O, V _{REF}	4	P77	P98	T12	418
GND	-	-	-	GND*	-
I/O	4	-	P99	T13	421
I/O	4	-	-	N12	424
I/O	4	P76	P100	R13	427
I/O	4	-	-	P12	430
I/O	4	P75	P101	P13	433
I/O	4	P74	P102	T14	436
GND	-	P73	P103	GND*	-
DONE	3	P72	P104	R14	439
V _{CCO}	4	P71	P105	V _{CCO} Bank 4*	-
V _{CCO}	3	P70	P105	V _{CCO} Bank 3*	-
PROGRAM	-	P69	P106	P15	442
I/O (INIT)	3	P68	P107	N15	443
I/O (D7)	3	P67	P108	N14	446
I/O	3	-	-	T15	449
I/O	3	P66	P109	M13	452
I/O	3	-	-	R16	455
I/O	3	-	P110	M14	458
GND	-	-	-	GND*	-
I/O, V _{REF}	3	P65	P111	L14	461
I/O	3	-	P112	M15	464
I/O	3	-	-	L12	467
I/O	3	P64	P113	P16	470
I/O	3	P63	P114	L13	473
I/O (D6)	3	P62	P115	N16	476
GND	-	P61	P116	GND*	-
V _{CCO}	3	-	P117	V _{CCO} Bank 3*	-
V _{CCINT}	-	-	P118	V _{CCINT} *	-
I/O (D5)	3	P60	P119	M16	479
I/O	3	P59	P120	K14	482
I/O	3	-	-	L16	485
I/O	3	-	P121	K13	488
I/O	3	-	P122	L15	491
I/O	3	-	P123	K12	494
GND	-	-	P124	GND*	-
I/O, V _{REF}	3	P58	P125	K16	497
I/O (D4)	3	P57	P126	J16	500
I/O	3	-	-	J14	503
I/O	3	P56	P127	K15	506
V _{CCINT}	-	P55	P128	V _{CCINT} *	-
I/O, TRDY	3	P54	P129	J15	512
V _{CCO}	3	P53	P130	V _{CCO} Bank 3*	-
V _{CCO}	2	P53	P130	V _{CCO} Bank 2*	-
GND	-	P52	P131	GND*	-

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O, IRDY	2	P51	P132	H16	515
I/O	2	-	P133	H14	518
I/O	2	P50	P134	H15	521
I/O	2	-	-	J13	524
I/O (D3)	2	P49	P135	G16	527
I/O, V _{REF}	2	P48	P136	H13	530
GND	-	-	P137	GND*	-
I/O	2	-	P138	G14	533
I/O	2	-	P139	G15	536
I/O	2	-	P140	G12	539
I/O	2	-	-	F16	542
I/O	2	P47	P141	G13	545
I/O (D2)	2	P46	P142	F15	548
V _{CCINT}	-	-	P143	V _{CCINT} *	-
V _{CCO}	2	-	P144	V _{CCO} Bank 2*	-
GND	-	P45	P145	GND*	-
I/O (D1)	2	P44	P146	E16	551
I/O	2	P43	P147	F14	554
I/O	2	P42	P148	D16	557
I/O	2	-	-	F12	560
I/O	2	-	P149	E15	563
I/O, V _{REF}	2	P41	P150	F13	566
GND	-	-	-	GND*	-
I/O	2	-	P151	E14	569
I/O	2	-	-	C16	572
I/O	2	P40	P152	E13	575
I/O	2	-	-	B16	578
I/O (DIN, D0)	2	P39	P153	D14	581
I/O (DOUT, BUSY)	2	P38	P154	C15	584
CCLK	2	P37	P155	D15	587
V _{CCO}	2	P36	P156	V _{CCO} Bank 2*	-
V _{CCO}	1	P35	P156	V _{CCO} Bank 1*	-
TDO	2	P34	P157	B14	-
GND	-	P33	P158	GND*	-
TDI	-	P32	P159	A15	-
I/O (CS)	1	P31	P160	B13	0
I/O (WRITE)	1	P30	P161	C13	3
I/O	1	-	-	C12	6
I/O	1	P29	P162	A14	9
I/O	1	-	-	D12	12
I/O	1	-	P163	B12	15
V _{CCO}	1	-	-	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P28	P164	C11	18
I/O	1	-	P165	A13	21
I/O	1	-	-	D11	24
I/O	1	-	P166	A12	27
I/O	1	P27	P167	E11	30
I/O	1	P26	P168	B11	33
GND	-	P25	P169	GND*	-
V _{CCO}	1	-	P170	V _{CCO} Bank 1*	-

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
V _{CCINT}	-	P24	P171	V _{CCINT} *	-
I/O	1	P23	P172	A11	36
I/O	1	P22	P173	C10	39
I/O	1	-	P174	B10	45
I/O	1	-	P175	D10	48
I/O	1	-	P176	A10	51
GND	-	-	P177	GND*	-
I/O, V _{REF}	1	P21	P178	B9	54
I/O	1	-	P179	E10	57
I/O	1	-	-	A9	60
I/O	1	P20	P180	D9	63
I/O	1	P19	P181	A8	66
GCK2	-	P18	P182	C9	72
GND	-	P17	P183	GND*	-
V _{CCO}	1	P16	P184	V _{CCO} Bank 1*	-
V _{CCO}	0	P16	P184	V _{CCO} Bank 0*	-
GCK3	-	P15	P185	B8	73
V _{CCINT}	-	P14	P186	V _{CCINT} *	-
I/O	0	P13	P187	A7	80
I/O	0	-	-	D8	83
I/O	0	-	P188	A6	86
I/O, V _{REF}	0	P12	P189	B7	89
GND	-	-	P190	GND*	-
I/O	0	-	P191	C8	92
I/O	0	-	P192	D7	95
I/O	0	-	P193	E7	98
I/O	0	P11	P194	C7	104
I/O	0	P10	P195	B6	107
V _{CCINT}	-	P9	P196	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	-
I/O	0	P7	P199	A5	110
I/O	0	P6	P200	C6	113
I/O	0	-	P201	B5	116
I/O	0	-	-	D6	119
I/O	0	-	P202	A4	122
I/O, V _{REF}	0	P5	P203	B4	125
GND	-	-	-	GND*	-
I/O	0	-	P204	E6	128
I/O	0	-	-	D5	131
I/O	0	P4	P205	A3	134
I/O	0	-	-	C5	137
I/O	0	P3	P206	B3	140
TCK	-	P2	P207	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	-

3/1/00

* Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.

Additional XC2S50 Package Pins

FG256

V _{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V _{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V _{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V _{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V _{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V _{CCO} Bank 4 Pins					
L9	M9	-	-	-	-

V _{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V _{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V _{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16

3/1/00

XC2S100 Device Pinouts

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
GND	-	P143	P1	GND*	GND*	-
TMS	-	P142	P2	D3	D3	-
I/O	7	P141	P3	C2	B1	185
I/O	7	-	-	A2	F5	191
I/O	7	P140	P4	B1	D2	194
I/O	7	-	-	-	E3	197
I/O	7	-	-	E3	G5	200
I/O	7	-	P5	D2	F3	203
GND	-	-	-	GND*	GND*	-
V _{CCO}	7	-	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P139	P6	C1	E2	206
I/O	7	-	P7	F3	E1	209
I/O	7	-	-	E2	H5	215
I/O	7	P138	P8	E4	F2	218
I/O	7	-	-	-	F1	221
I/O, V _{REF}	7	P137	P9	D1	H4	224
I/O	7	P136	P10	E1	G1	227
GND	-	P135	P11	GND*	GND*	-
V _{CCO}	7	-	P12	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCINT}	-	-	P13	V _{CCINT} *	V _{CCINT} *	-
I/O	7	P134	P14	F2	H3	230
I/O	7	P133	P15	G3	H2	233
I/O	7	-	-	F1	J5	236
I/O	7	-	P16	F4	J2	239
I/O	7	-	P17	F5	K5	245
I/O	7	-	P18	G2	K1	248
GND	-	-	P19	GND*	GND*	-
I/O, V _{REF}	7	P132	P20	H3	K3	251
I/O	7	P131	P21	G4	K4	254
I/O	7	-	-	H2	L6	257
I/O	7	P130	P22	G5	L1	260
I/O	7	-	P23	H4	L4	266
I/O, IRDY	7	P129	P24	G1	L3	269
GND	-	P128	P25	GND*	GND*	-

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
V _{CCO}	7	P127	P26	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCO}	6	P127	P26	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
I/O, TRDY	6	P126	P27	J2	M1	272
V _{CCINT}	-	P125	P28	V _{CCINT} *	V _{CCINT} *	-
I/O	6	P124	P29	H1	M3	281
I/O	6	-	-	J4	M4	284
I/O	6	P123	P30	J1	M5	287
I/O, V _{REF}	6	P122	P31	J3	N2	290
GND	-	-	P32	GND*	GND*	-
I/O	6	-	P33	K5	N3	293
I/O	6	-	P34	K2	N4	296
I/O	6	-	P35	K1	P2	302
I/O	6	-	-	K3	P4	305
I/O	6	P121	P36	L1	P3	308
I/O	6	P120	P37	L2	R2	311
V _{CCINT}	-	-	P38	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	6	-	P39	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P119	P40	GND*	GND*	-
I/O	6	P118	P41	K4	T1	314
I/O, V _{REF}	6	P117	P42	M1	R4	317
I/O	6	-	-	-	T2	320
I/O	6	P116	P43	L4	U1	323
I/O	6	-	-	M2	R5	326
I/O	6	-	P44	L3	U2	332
I/O, V _{REF}	6	P115	P45	N1	T3	335
V _{CCO}	6	-	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	-	-	GND*	GND*	-
I/O	6	-	P46	P1	T4	338
I/O	6	-	-	L5	W1	341
I/O	6	-	-	-	U4	344
I/O	6	P114	P47	N2	Y1	347
I/O	6	-	-	M4	W2	350
I/O	6	P113	P48	R1	Y2	356

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O	6	P112	P49	M3	W3	359
M1	-	P111	P50	P2	U5	362
GND	-	P110	P51	GND*	GND*	-
M0	-	P109	P52	N3	AB2	363
V _{CCO}	6	P108	P53	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
V _{CCO}	5	P107	P53	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
M2	-	P106	P54	R3	Y4	364
PWDN	-	P105	P55	P4	V6	-
STATUS	5	P104	P56	R4	Y5	-
I/O	5	-	-	N5	V7	374
I/O	5	P103	P57	T2	Y6	377
I/O	5	-	-	-	AA4	380
I/O	5	-	-	P5	W6	383
I/O	5	-	P58	T3	Y7	386
GND	-	-	-	GND*	GND*	-
V _{CCO}	5	-	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P102	P59	T4	AA5	389
I/O	5	-	P60	M6	AB5	392
I/O	5	-	-	T5	AB6	398
I/O	5	P101	P61	N6	AA7	401
I/O	5	-	-	-	W7	404
I/O, V _{REF}	5	P100	P62	R5	W8	407
I/O	5	P99	P63	P6	Y8	410
GND	-	P98	P64	GND*	GND*	-
V _{CCO}	5	-	P65	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCINT}	-	P97	P66	V _{CCINT} *	V _{CCINT} *	-
I/O	5	P96	P67	R6	AA8	413
I/O	5	P95	P68	M7	V9	416
I/O	5	-	-	-	AB9	419
I/O	5	-	P69	N7	Y9	422
I/O	5	-	P70	T6	W10	428
I/O	5	-	P71	P7	AB10	431
GND	-	-	P72	GND*	GND*	-
I/O, V _{REF}	5	P94	P73	P8	Y10	434
I/O	5	-	P74	R7	V11	437
I/O	5	-	-	T7	W11	440
I/O	5	P93	P75	T8	AB11	443
V _{CCINT}	-	P92	P76	V _{CCINT} *	V _{CCINT} *	-
GCK1	-	P91	P77	R8	Y11	455
V _{CCO}	5	P90	P78	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCO}	4	P90	P78	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P89	P79	GND*	GND*	-
GCK0	-	P88	P80	N8	W12	456
I/O	4	P87	P81	N9	U12	460
I/O	4	P86	P82	R9	Y12	466
I/O	4	-	-	N10	AA12	469
I/O	4	-	P83	T9	AB13	472
I/O, V _{REF}	4	P85	P84	P9	AA13	475
GND	-	-	P85	GND*	GND*	-
I/O	4	-	P86	M10	Y13	478
I/O	4	-	P87	R10	V13	481
I/O	4	-	P88	P10	AA14	487
I/O	4	-	-	-	V14	490

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O	4	P84	P89	T10	AB15	493
I/O	4	P83	P90	R11	AA15	496
V _{CCINT}	-	P82	P91	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	4	-	P92	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P81	P93	GND*	GND*	-
I/O	4	P80	P94	M11	Y15	499
I/O, V _{REF}	4	P79	P95	T11	AB16	502
I/O	4	-	-	-	AB17	505
I/O	4	P78	P96	N11	V15	508
I/O	4	-	-	R12	Y16	511
I/O	4	-	P97	P11	AB18	517
I/O, V _{REF}	4	P77	P98	T12	AB19	520
V _{CCO}	4	-	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	-	-	GND*	GND*	-
I/O	4	-	P99	T13	Y17	523
I/O	4	-	-	N12	V16	526
I/O	4	-	-	-	W17	529
I/O	4	P76	P100	R13	AB20	532
I/O	4	-	-	P12	AA19	535
I/O	4	P75	P101	P13	AA20	541
I/O	4	P74	P102	T14	W18	544
GND	-	P73	P103	GND*	GND*	-
DONE	3	P72	P104	R14	Y19	547
V _{CCO}	4	P71	P105	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
V _{CCO}	3	P70	P105	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
PROGRAM	-	P69	P106	P15	W20	550
I/O (INIT)	3	P68	P107	N15	V19	551
I/O (D7)	3	P67	P108	N14	Y21	554
I/O	3	-	-	T15	W21	560
I/O	3	P66	P109	M13	U20	563
I/O	3	-	-	-	U19	566
I/O	3	-	-	R16	T18	569
I/O	3	-	P110	M14	W22	572
GND	-	-	-	GND*	GND*	-
V _{CCO}	3	-	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P65	P111	L14	U21	575
I/O	3	-	P112	M15	T20	578
I/O	3	-	-	L12	T21	584
I/O	3	P64	P113	P16	R18	587
I/O	3	-	-	-	U22	590
I/O, V _{REF}	3	P63	P114	L13	R19	593
I/O (D6)	3	P62	P115	N16	T22	596
GND	-	P61	P116	GND*	GND*	-
V _{CCO}	3	-	P117	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCINT}	-	-	P118	V _{CCINT} *	V _{CCINT} *	-
I/O (D5)	3	P60	P119	M16	R21	599
I/O	3	P59	P120	K14	P18	602
I/O	3	-	-	L16	P20	605
I/O	3	-	P121	K13	P21	608
I/O	3	-	P122	L15	N18	614
I/O	3	-	P123	K12	N20	617
GND	-	-	P124	GND*	GND*	-
I/O, V _{REF}	3	P58	P125	K16	N21	620

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O (D4)	3	P57	P126	J16	N22	623
I/O	3	-	-	J14	M19	626
I/O	3	P56	P127	K15	M20	629
V _{CCINT}	-	P55	P128	E5	V _{CCINT} *	-
I/O, TRDY	3	P54	P129	J15	M22	638
V _{CCO}	3	P53	P130	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCO}	2	P53	P130	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P52	P131	GND*	GND*	-
I/O, IRDY	2	P51	P132	H16	L20	641
I/O	2	-	P133	H14	L17	644
I/O	2	P50	P134	H15	L21	650
I/O	2	-	-	J13	L22	653
I/O (D3)	2	P49	P135	G16	K20	656
I/O, V _{REF}	2	P48	P136	H13	K21	659
GND	-	-	P137	GND*	GND*	-
I/O	2	-	P138	G14	K22	662
I/O	2	-	P139	G15	J21	665
I/O	2	-	P140	G12	J18	671
I/O	2	-	-	F16	J22	674
I/O	2	P47	P141	G13	H19	677
I/O (D2)	2	P46	P142	F15	H20	680
V _{CCINT}	-	-	P143	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	2	-	P144	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P45	P145	GND*	GND*	-
I/O (D1)	2	P44	P146	E16	H22	683
I/O, V _{REF}	2	P43	P147	F14	H18	686
I/O	2	-	-	-	G21	689
I/O	2	P42	P148	D16	G18	692
I/O	2	-	-	F12	G20	695
I/O	2	-	P149	E15	F19	701
I/O, V _{REF}	2	P41	P150	F13	F21	704
V _{CCO}	2	-	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	-	GND*	GND*	-
I/O	2	-	P151	E14	F20	707
I/O	2	-	-	C16	F18	710
I/O	2	-	-	-	E21	713
I/O	2	P40	P152	E13	D22	716
I/O	2	-	-	B16	E20	719
I/O (DIN, D0)	2	P39	P153	D14	D20	725
I/O (DOUT, BUSY)	2	P38	P154	C15	C21	728
CCLK	2	P37	P155	D15	B22	731
V _{CCO}	2	P36	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
V _{CCO}	1	P35	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P34	P157	B14	A21	-
GND	-	P33	P158	GND*	GND*	-
TDI	-	P32	P159	A15	B20	-
I/O (CS)	1	P31	P160	B13	C19	0
I/O (WRITE)	1	P30	P161	C13	A20	3
I/O	1	-	-	C12	D17	9
I/O	1	P29	P162	A14	A19	12
I/O	1	-	-	-	B18	15
I/O	1	-	-	D12	C17	18

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O	1	-	P163	B12	D16	21
GND	-	-	-	GND*	GND*	-
V _{CCO}	1	-	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P28	P164	C11	A18	24
I/O	1	-	P165	A13	B17	27
I/O	1	-	-	D11	D15	33
I/O	1	-	P166	A12	C16	36
I/O	1	-	-	-	D14	39
I/O, V _{REF}	1	P27	P167	E11	E14	42
I/O	1	P26	P168	B11	A16	45
GND	-	P25	P169	GND*	GND*	-
V _{CCO}	1	-	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P24	P171	V _{CCINT} *	V _{CCINT} *	-
I/O	1	P23	P172	A11	C15	48
I/O	1	P22	P173	C10	B15	51
I/O	1	-	-	-	F12	54
I/O	1	-	P174	B10	C14	57
I/O	1	-	P175	D10	D13	63
I/O	1	-	P176	A10	C13	66
GND	-	-	P177	GND*	GND*	-
I/O, V _{REF}	1	P21	P178	B9	B13	69
I/O	1	-	P179	E10	E12	72
I/O	1	-	-	A9	B12	75
I/O	1	P20	P180	D9	D12	78
I/O	1	P19	P181	A8	D11	84
GCK2	-	P18	P182	C9	A11	90
GND	-	P17	P183	GND*	GND*	-
V _{CCO}	1	P16	P184	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCO}	0	P16	P184	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GCK3	-	P15	P185	B8	C11	91
V _{CCINT}	-	P14	P186	V _{CCINT} *	V _{CCINT} *	-
I/O	0	P13	P187	A7	A10	101
I/O	0	-	-	D8	B10	104
I/O	0	-	P188	A6	C10	107
I/O, V _{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V _{CCINT}	-	P9	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V _{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V _{REF}	0	P5	P203	B4	C6	155
V _{CCO}	0	-	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
TCK	-	P2	P207	C4	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

3/1/00

* Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.

Additional XC2S100 Package Pins

FG256

V _{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V _{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V _{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V _{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V _{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V _{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V _{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V _{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V _{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16

FG456

V _{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16

U6	U17	V5	V18	-	-
V _{CCO} Bank 0 Pins					
F10	F7	F8	F9	G10	G11
V _{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V _{CCO} Bank 3 Pins					
G17	H17	J17	K16	K17	L16
V _{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V _{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V _{CCO} Bank 5 Pins					
T10	T11	U10	U7	U8	U9
V _{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V _{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A4	A5	A6	A12	A13
A14	A15	A17	B3	B6	B8
B11	B14	B16	B19	C1	C2
C8	C9	C12	C18	C22	D1
D4	D5	D10	D18	D19	D21
E4	E11	E13	E15	E16	E17
E19	E22	F4	F11	F22	G2
G3	G4	G19	G22	H1	H21
J1	J3	J4	J19	J20	K2
K18	K19	L2	L5	L18	L19
M2	M6	M17	M18	M21	N1
N5	N19	P1	P5	P19	P22
R1	R3	R20	R22	T5	T19
U3	U11	U18	V1	V2	V10
V12	V17	V3	V4	V8	V20
V21	V22	W4	W5	W9	W13
W14	W15	W16	W19	Y14	Y18
Y22	AA1	AA3	AA6	AA9	AA10
AA11	AA16	AA17	AA18	AA22	AB3
AB4	AB7	AB8	AB12	AB14	AB21

3/1/00

XC2S150 Device Pinouts

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	221
I/O	7	-	-	E4	224
I/O	7	-	-	C1	227
I/O	7	-	A2	F5	230
GND	-	-	GND*	GND*	-
I/O	7	P4	B1	D2	233
I/O	7	-	-	E3	236
I/O	7	-	-	F4	239
I/O	7	-	E3	G5	242
I/O	7	P5	D2	F3	245
GND	-	-	GND*	GND*	-
V _{CCO}	7	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P6	C1	E2	248
I/O	7	P7	F3	E1	251
I/O	7	-	-	G4	254
I/O	7	-	-	G3	257
I/O	7	-	E2	H5	260
I/O	7	P8	E4	F2	263
I/O	7	-	-	F1	266
I/O, V _{REF}	7	P9	D1	H4	269
I/O	7	P10	E1	G1	272
GND	-	P11	GND*	GND*	-
V _{CCO}	7	P12	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCINT}	-	P13	V _{CCINT} *	V _{CCINT} *	-
I/O	7	P14	F2	H3	275
I/O	7	P15	G3	H2	278
I/O	7	-	-	H1	284
I/O	7	-	F1	J5	287
I/O	7	P16	F4	J2	290
I/O	7	-	-	J3	293
I/O	7	P17	F5	K5	299
I/O	7	P18	G2	K1	302
GND	-	P19	GND*	GND*	-
V _{CCO}	7	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P20	H3	K3	305
I/O	7	P21	G4	K4	308
I/O	7	-	H2	L6	311
I/O	7	P22	G5	L1	314
I/O	7	-	-	L5	317
I/O	7	P23	H4	L4	320
I/O, IRDY	7	P24	G1	L3	323
GND	-	P25	GND*	GND*	-
V _{CCO}	7	P26	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCO}	6	P26	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
I/O, TRDY	6	P27	J2	M1	326
V _{CCINT}	-	P28	V _{CCINT} *	V _{CCINT} *	-
I/O	6	-	-	M6	332
I/O	6	P29	H1	M3	335

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	J4	M4	338
I/O	6	P30	J1	M5	341
I/O, V _{REF}	6	P31	J3	N2	344
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	347
I/O	6	P34	K2	N4	350
I/O	6	-	-	N5	356
I/O	6	P35	K1	P2	359
I/O	6	-	K3	P4	362
I/O	6	-	-	R1	365
I/O	6	P36	L1	P3	371
I/O	6	P37	L2	R2	374
V _{CCINT}	-	P38	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	6	P39	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	377
I/O, V _{REF}	6	P42	M1	R4	380
I/O	6	-	-	T2	383
I/O	6	P43	L4	U1	386
I/O	6	-	M2	R5	389
I/O	6	-	-	V1	392
I/O	6	-	-	T5	395
I/O	6	P44	L3	U2	398
I/O, V _{REF}	6	P45	N1	T3	401
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	404
I/O	6	-	L5	W1	407
I/O	6	-	-	V2	410
I/O	6	-	-	U4	413
I/O	6	P47	N2	Y1	416
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	419
I/O	6	-	-	V3	422
I/O	6	-	-	V4	425
I/O	6	P48	R1	Y2	428
I/O	6	P49	M3	W3	431
M1	-	P50	P2	U5	434
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	435
V _{CCO}	6	P53	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
V _{CCO}	5	P53	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
M2	-	P54	R3	Y4	436
PW _{DN}	-	P55	P4	V6	-
STATUS	5	P56	R4	Y5	-
I/O	5	-	-	W5	443
I/O	5	-	-	AB3	446
I/O	5	-	N5	V7	449
GND	-	-	GND*	GND*	-
I/O	5	P57	T2	Y6	452

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	5	-	-	AA4	455
I/O	5	-	-	AB4	458
I/O	5	-	P5	W6	461
I/O	5	P58	T3	Y7	464
GND	-	-	GND*	GND*	-
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P59	T4	AA5	467
I/O	5	P60	M6	AB5	470
I/O	5	-	-	V8	473
I/O	5	-	-	AA6	476
I/O	5	-	T5	AB6	479
I/O	5	P61	N6	AA7	482
I/O	5	-	-	W7	485
I/O, V _{REF}	5	P62	R5	W8	488
I/O	5	P63	P6	Y8	491
GND	-	P64	GND*	GND*	-
V _{CCO}	5	P65	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCINT}	-	P66	V _{CCINT} *	V _{CCINT} *	-
I/O	5	P67	R6	AA8	494
I/O	5	P68	M7	V9	497
I/O	5	-	-	W9	503
I/O	5	-	-	AB9	506
I/O	5	P69	N7	Y9	509
I/O	5	-	-	V10	512
I/O	5	P70	T6	W10	518
I/O	5	P71	P7	AB10	521
GND	-	P72	GND*	GND*	-
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P73	P8	Y10	524
I/O	5	P74	R7	V11	527
I/O	5	-	T7	W11	530
I/O	5	P75	T8	AB11	533
I/O	5	-	-	U11	536
V _{CCINT}	-	P76	V _{CCINT} *	V _{CCINT} *	-
GCK1	-	P77	R8	Y11	545
V _{CCO}	5	P78	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCO}	4	P78	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-
GCK0	-	P80	N8	W12	546
I/O	4	P81	N9	U12	550
I/O	4	-	-	V12	553
I/O	4	P82	R9	Y12	556
I/O	4	-	N10	AA12	559
I/O	4	P83	T9	AB13	562
I/O, V _{REF}	4	P84	P9	AA13	565
V _{CCO}	4	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	568
I/O	4	P87	R10	V13	571
I/O	4	-	-	W14	577
I/O	4	P88	P10	AA14	580
I/O	4	-	-	V14	583

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	4	-	-	Y14	586
I/O	4	P89	T10	AB15	592
I/O	4	P90	R11	AA15	595
V _{CCINT}	-	P91	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	4	P92	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P93	GND*	GND*	-
I/O	4	P94	M11	Y15	598
I/O, V _{REF}	4	P95	T11	AB16	601
I/O	4	-	-	AB17	604
I/O	4	P96	N11	V15	607
I/O	4	-	R12	Y16	610
I/O	4	-	-	AA17	613
I/O	4	-	-	W16	616
I/O	4	P97	P11	AB18	619
I/O, V _{REF}	4	P98	T12	AB19	622
V _{CCO}	4	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	-	GND*	GND*	-
I/O	4	P99	T13	Y17	625
I/O	4	-	N12	V16	628
I/O	4	-	-	AA18	631
I/O	4	-	-	W17	634
I/O	4	P100	R13	AB20	637
GND	-	-	GND*	GND*	-
I/O	4	-	P12	AA19	640
I/O	4	-	-	V17	643
I/O	4	-	-	Y18	646
I/O	4	P101	P13	AA20	649
I/O	4	P102	T14	W18	652
GND	-	P103	GND*	GND*	-
DONE	3	P104	R14	Y19	655
V _{CCO}	4	P105	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
V _{CCO}	3	P105	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
PROGRAM	-	P106	P15	W20	658
I/O (INIT)	3	P107	N15	V19	659
I/O (D7)	3	P108	N14	Y21	662
I/O	3	-	-	V20	665
I/O	3	-	-	AA22	668
I/O	3	-	T15	W21	671
GND	3	-	GND*	GND*	-
I/O	3	P109	M13	U20	674
I/O	3	-	-	U19	677
I/O	3	-	-	V21	680
I/O	3	-	R16	T18	683
I/O	3	P110	M14	W22	686
GND	-	-	GND*	GND*	-
V _{CCO}	3	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P111	L14	U21	689
I/O	3	P112	M15	T20	692
I/O	3	-	-	T19	695
I/O	3	-	-	V22	698
I/O	3	-	L12	T21	701
I/O	3	P113	P16	R18	704
I/O	3	-	-	U22	707

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O, V _{REF}	3	P114	L13	R19	710
I/O (D6)	3	P115	N16	T22	713
GND	-	P116	GND*	GND*	-
V _{CCO}	3	P117	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCINT}	-	P118	V _{CCINT} *	V _{CCINT} *	-
I/O (D5)	3	P119	M16	R21	716
I/O	3	P120	K14	P18	719
I/O	3	-	-	P19	725
I/O	3	-	L16	P20	728
I/O	3	P121	K13	P21	731
I/O	3	-	-	N19	734
I/O	3	P122	L15	N18	740
I/O	3	P123	K12	N20	743
GND	-	P124	GND*	GND*	-
V _{CCO}	3	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P125	K16	N21	746
I/O (D4)	3	P126	J16	N22	749
I/O	3	-	J14	M19	752
I/O	3	P127	K15	M20	755
I/O	3	-	-	M18	758
V _{CCINT}	-	P128	V _{CCINT} *	V _{CCINT} *	-
I/O, TRDY	3	P129	J15	M22	764
V _{CCO}	3	P130	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCO}	2	P130	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P131	GND*	GND*	-
I/O, IRDY	2	P132	H16	L20	767
I/O	2	P133	H14	L17	770
I/O	2	-	-	L18	773
I/O	2	P134	H15	L21	776
I/O	2	-	J13	L22	779
I/O (D3)	2	P135	G16	K20	782
I/O, V _{REF}	2	P136	H13	K21	785
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P137	GND*	GND*	-
I/O	2	P138	G14	K22	788
I/O	2	P139	G15	J21	791
I/O	2	-	-	J20	797
I/O	2	P140	G12	J18	800
I/O	2	-	F16	J22	803
I/O	2	-	-	J19	806
I/O	2	P141	G13	H19	812
I/O (D2)	2	P142	F15	H20	815
V _{CCINT}	-	P143	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	2	P144	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P145	GND*	GND*	-
I/O (D1)	2	P146	E16	H22	818
I/O, V _{REF}	2	P147	F14	H18	821
I/O	2	-	-	G21	824
I/O	2	P148	D16	G18	827
I/O	2	-	F12	G20	830
I/O	2	-	-	G19	833
I/O	2	-	-	F22	836

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	2	P149	E15	F19	839
I/O, V _{REF}	2	P150	F13	F21	842
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	GND*	GND*	-
I/O	2	P151	E14	F20	845
I/O	2	-	C16	F18	848
I/O	2	-	-	E22	851
I/O	2	-	-	E21	854
I/O	2	P152	E13	D22	857
GND	-	-	GND*	GND*	-
I/O	2	-	B16	E20	860
I/O	2	-	-	D21	863
I/O	2	-	-	C22	866
I/O (DIN, D0)	2	P153	D14	D20	869
I/O (DOUT, BUSY)	2	P154	C15	C21	872
CCLK	2	P155	D15	B22	875
V _{CCO}	2	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
V _{CCO}	1	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O (CS)	1	P160	B13	C19	0
I/O (WRITE)	1	P161	C13	A20	3
I/O	1	-	-	B19	6
I/O	1	-	-	C18	9
I/O	1	-	C12	D17	12
GND	-	-	GND*	GND*	-
I/O	1	P162	A14	A19	15
I/O	1	-	-	B18	18
I/O	1	-	-	E16	21
I/O	1	-	D12	C17	24
I/O	1	P163	B12	D16	27
GND	-	-	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P164	C11	A18	30
I/O	1	P165	A13	B17	33
I/O	1	-	-	E15	36
I/O	1	-	-	A17	39
I/O	1	-	D11	D15	42
I/O	1	P166	A12	C16	45
I/O	1	-	-	D14	48
I/O, V _{REF}	1	P167	E11	E14	51
I/O	1	P168	B11	A16	54
GND	-	P169	GND*	GND*	-
V _{CCO}	1	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P171	V _{CCINT} *	V _{CCINT} *	-
I/O	1	P172	A11	C15	57
I/O	1	P173	C10	B15	60
I/O	1	-	-	A15	66
I/O	1	-	-	F12	69
I/O	1	P174	B10	C14	72
I/O	1	-	-	B14	75
I/O	1	P175	D10	D13	81

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	1	P176	A10	C13	84
GND	-	P177	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P178	B9	B13	87
I/O	1	P179	E10	E12	90
I/O	1	-	A9	B12	93
I/O	1	P180	D9	D12	96
I/O	1	-	-	C12	99
I/O	1	P181	A8	D11	102
GCK2	-	P182	C9	A11	108
GND	-	P183	GND*	GND*	-
V _{CCO}	1	P184	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCO}	0	P184	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GCK3	-	P185	B8	C11	109
V _{CCINT}	-	P186	V _{CCINT} *	V _{CCINT} *	-
I/O	0	-	-	E11	116
I/O	0	P187	A7	A10	119
I/O	0	-	D8	B10	122
I/O	0	P188	A6	C10	125
I/O, V _{REF}	0	P189	B7	A9	128
V _{CCO}	0	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	131
I/O	0	P192	D7	E10	134
I/O	0	-	-	D10	140
I/O	0	P193	E7	A8	143
I/O	0	-	-	D9	146
I/O	0	-	-	B8	149
I/O	0	P194	C7	E9	155
I/O	0	P195	B6	A7	158
V _{CCINT}	-	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P198	GND*	GND*	-
I/O	0	P199	A5	B7	161
I/O, V _{REF}	0	P200	C6	E8	164
I/O	0	-	-	D8	167
I/O	0	P201	B5	C7	170
I/O	0	-	D6	D7	173
I/O	0	-	-	B6	176
I/O	0	-	-	A5	179
I/O	0	P202	A4	D6	182
I/O, V _{REF}	0	P203	B4	C6	185
V _{CCO}	0	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	-	GND*	GND*	-
I/O	0	P204	E6	B5	188
I/O	0	-	D5	E7	191
I/O	0	-	-	A4	194
I/O	0	-	-	E6	197
I/O	0	P205	A3	B4	200
GND	-	-	GND*	GND*	-
I/O	0	-	C5	A3	203
I/O	0	-	-	B3	206

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	0	-	-	D5	209
I/O	0	P206	B3	C5	212
TCK	-	P207	C4	C4	-
V _{CCO}	0	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

3/1/00

* Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.

Additional XC2S150 Package Pins

FG256

V _{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V _{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V _{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V _{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V _{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V _{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V _{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V _{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V _{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16

3/1/00

FG456

V _{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V _{CCO} BANK 0 Pins					
F7	F8	F9	F10	G10	G11
V _{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V _{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16

V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	B11	B16	C2
D1	D4	D18	D19	E5	E6
E17	E19	F6	G7	G14	G16
H6	J16	L2	L19	M2	M21
P7	R3	R7	R20	T7	T9
T14	T16	U3	U17	U18	V18
W4	W19	Y22	AA1	AA3	AA11
AA16	AB7	AB12	AB21		

Spartan-II Product Availability

Table 37 shows the package and speed grades available for Spartan-II family devices. Table 38 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 37: Spartan-II Package and Speed Grade Availability

Device	Pins	100	144	144	208	256	456
	Type	Plast. VQFP	Plast. TQFP	Chip Scale BGA	Plast. PQFP	Fine Pitch BGA	Fine Pitch BGA
	Code	VQ100	TQ144	CS144	PQ208	FG256	FG456
XC2S15	-5	(C)	(C)	(C)	-	-	-
	-6	(C)	(C)	(C)	-	-	-
XC2S30	-5	(C)	(C)	(C)	(C)	-	-
	-6	(C)	(C)	(C)	(C)	-	-
XC2S50	-5	-	C	-	C	C	-
	-6	-	(C)	-	(C)	(C)	-
XC2S100	-5	-	C	-	C	C	C
	-6	-	(C)	-	(C)	(C)	(C)
XC2S150	-5	-	-	-	C	C	C
	-6	-	-	-	(C)	(C)	(C)
XC2S200	-5	-	-	-	C	C	C
	-6	-	-	-	(C)	(C)	(C)

3/14/00

C = Commercial $T_J = 0^\circ$ to $+85^\circ\text{C}$

I = Industrial $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$

() Parentheses indicate future product plans

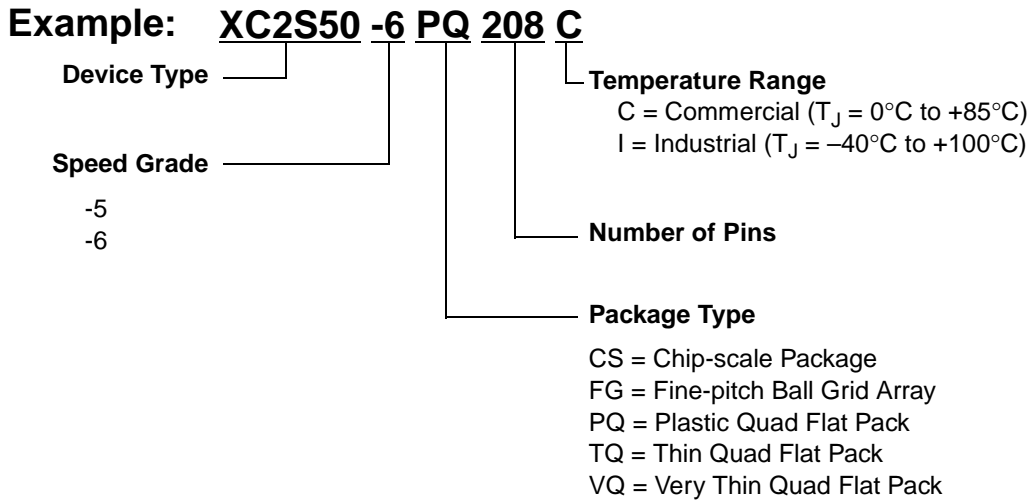
Table 38: Spartan-II Maximum User I/O Availability

Device	Max I/O		Package Type					
	SW*	Pkg.*	VQ100	TQ144	CS144	PQ208	FG256	FG456
XC2S15	96	86	60	86	86	-	-	-
XC2S30	144	132	60	92	92	132	-	-
XC2S50	192	176	-	92	-	140	176	-
XC2S100	240	196	-	92	-	140	176	196
XC2S150	288	260	-	-	-	140	176	260
XC2S200	336	284	-	-	-	140	176	284

3/14/00

**SW" indicates the max number of IOs on Die including buried IOs, "PKG" indicates the max number of IOs available to the user in the largest packages.

Ordering Code Format



Revision History

Version No.	Date	Description
	6/29/99	Initial Review Version
	7/2/99	Corrected I/O Count Errors, Misc. Errors
	8/15/99	Corrected CLB count & BGA legend
	9/28/99	Major Update - Speed, packages, architecture, etc.
	10/15/99	Added Proposed TQ144 pinouts & minor corrections
0.6	11/8/99	Corrections to TQ144 and other tables
0.7	11/30/99	Update Arch Section, misc fixes
0.8	1/17/00	No. of RAM blocks/device, V_{CCO} bank assignments on XC2S50 and XC2S100, misc.
0.9	3/3/00	Added bank associations to pinout tables, changed XC2S15 VQ100 pin 33 from I/O to V_{CCINT} . Added Delay-Locked Loop, Block RAM, and Versatile I/O Design Considerations section.
1.0	3/14/00	Added XC2S200. Updated -5 timing numbers to reflect v1.8 speed file. Reduced number of V_{REF} lines per bank on XC2S15, XC2S30 and XC2S50. Removed buried register listings in pinout tables.