XCR3256XL: 256 Macrocell CPLD

DS013 (v1.1) February 10, 2000 Preliminary Product Specification

Features

- 7.5 ns pin-to-pin logic delays
- System frequencies up to 140 MHz
- 256 macrocells with 6,000 usable gates
- Available in small footprint packages
  - 144-pin TQFP (116 user I/O pins)
  - 208-pin PQFP (160 user I/O)
  - 280-pin CS BGA (160 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer re-programmable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to family data sheet for architecture description

Description

The XCR3256XL is a 3.3V, 256 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 logic blocks provide 6,000 usable gates. Pin-to-pin propagation delays are 7.5 ns with a maximum system frequency of 140 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3256XL TotalCMOS CPLD (data taken with 16 up/down, loadable 16-bit counters at 3.3V, 25°C).

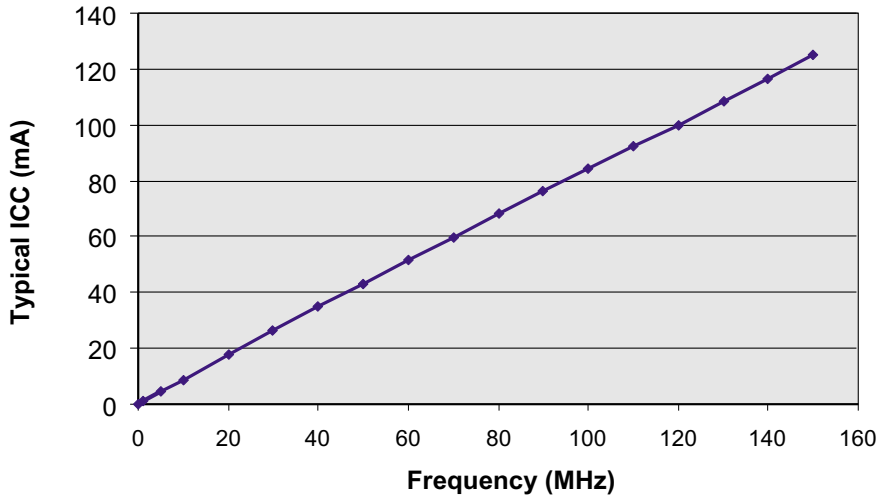


Figure 1: XCR3256XL Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C

Table 1: Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C

Frequency (MHz)	0	1	10	20	40	60	80	100	120	140	150
Typical I_{CC} (mA)	0.02	0.91	8.87	17.7	34.8	51.5	68	84.2	100.1	116.6	124.8

DC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output High voltage for 3.3V outputs	I_{OH} = –8 mA	2.4	-	V
V_{OL}	Output Low voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC}	–10	10	µA
I_{CCSB}	Standby current (1)	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current (1, 2)	f = 1 MHz	-	2	mA
		f = 50 MHz	-	60	mA
C_{IN}	Input pin capacitance (3)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance (3)	f = 1 MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance (3)	f = 1 MHz	-	10	pF

Notes:
1. See Table 1, Figure 1 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values not tested.

AC Electrical Characteristics(1)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	7.0	-	9.0	-	10.8	ns
T_{PD2}	Propagation delay time (OR array)	-	7.5	-	10.0	-	12.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	4.5	-	5.8	-	6.9	ns
T_{SUF}	Setup time fast	2.0	-	2.5	-	3.0	-	ns
T_{SU}	Setup time	4.8	-	6.5	-	7.9	-	ns
T_{H}	Hold time	0	-	0	-	0	-	ns
T_{WLH}	Global clock pulse width (High or Low)	3.0	-	4.0	-	5.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	4.5	-	6.0	-	7.5	-	ns
T_{R}	Input rise time	-	20	-	20	-	20	ns
T_{L}	Input fall time	-	20	-	20	-	20	ns
f_{SYSTEM}	Maximum internal frequency	140	-	105	-	88	-	MHz
T_{INIT}	Delay from valid Vcc to valid reset	-	TBD	-	TBD	-	TBD	
T_{POE}	P-term OE to output enabled	-	9.0	-	11.0	-	13.0	ns
T_{POD}	P-term OE to output disabled (2)	-	9.0	-	11.0	-	13.0	ns
T_{PCO}	Global set/reset to output valid	-	8.0	-	10.3	-	12.4	ns
T_{PAO}	P-term set/reset to output valid	-	9.0	-	11.0	-	13.0	ns
		Preliminary						

Notes:
1. Specifications measured with one output switching. See Figure 4 for derating.
2. Output C_L = 5 pF.

Timing Model

The XPLA3 architecture follows a simple timing model that allows deterministic timing in design and redesign. The basic timing model is shown in Figure 2. One key feature of the XPLA3 CPLD is the ability to have up to 48 product term inputs into a single macrocell and maintain consistent timing. This is achieved through the use of a fully populated PLA (Programmable AND Programmable OR Array) which also has the ability to share product terms and only use the required amount of product terms per macrocell. There is a fast path (T_{LOGI1}) into the macrocell which is used if there is a single product term. The T_{LOGI2} path is used for multiple product term timing. For optimization of logic, the XPLA3 CPLD architecture includes a Fold-back NAND path (T_{LOGI3}). There is a fast input path to each macrocell if used as an Input Register (T_{FIN}). XPLA3 also includes universal control terms (T_{UDA}) that can be used for synchronization of the macrocell registers in different logic blocks. There is also slew rate control and output enable control on a per macrocell basis.

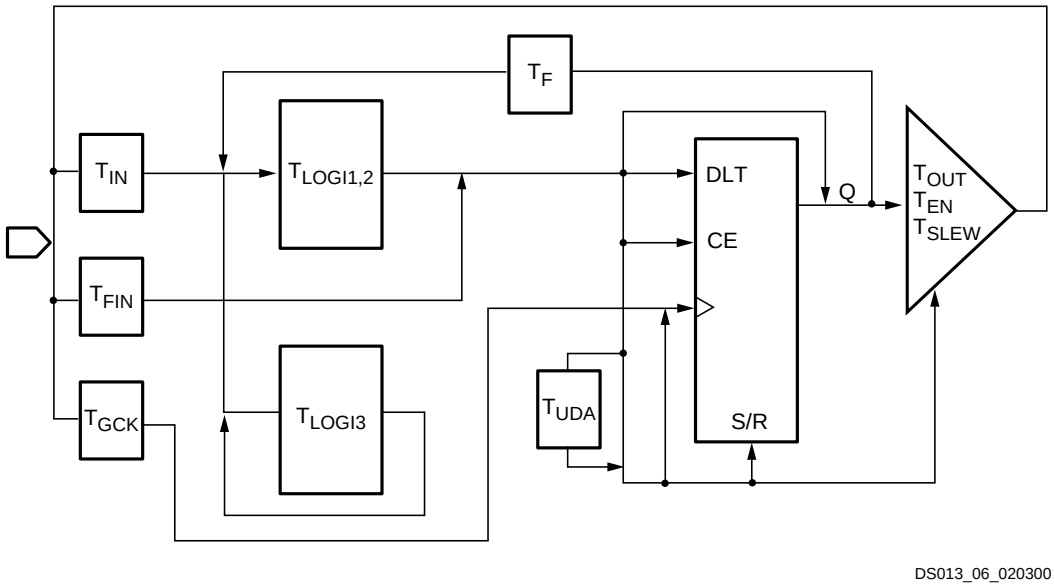
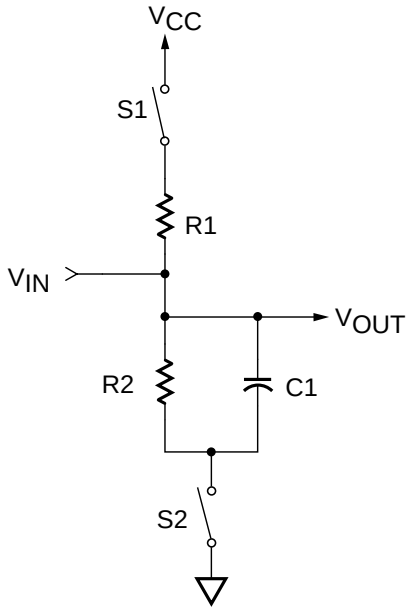


Figure 2: XPLA3 Timing Model

Internal Timing Parameters

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.3	-	4.0	ns
T_{FIN}	Fast input buffer delay	-	2.2	-	2.8	-	3.3	ns
T_{GCK}	Global clock buffer delay	-	1.0	-	1.3	-	1.5	ns
T_{OUT}	Output buffer delay	-	2.5	-	2.8	-	3.3	ns
T_{EN}	Output buffer enable/disable delay	-	4.5	-	5.2	-	6.0	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	0.4	-	0.5	-	0.6	-	ns
T_{SUI}	Register setup time	0.8	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	4.0	-	5.5	-	6.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.0	-	2.0	-	2.2	ns
T_{RAI}	Register async. recovery	-	5.0	-	7.0	-	8.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.5	-	3.0	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.5	-	4.2	ns
Feedback Delays								
T_{F}	ZIA delay	-	2.8	-	3.7	-	4.4	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	6.0	-	8.0	-	9.5	ns
T_{UDA}	Universal delay	-	2.0	-	2.5	-	3.0	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns
		Preliminary						

Switching Characteristics



Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{PZH}	Open	Closed
T_{PZL}	Closed	Open
T_P	Closed	Closed

Note: For T_{PZH} and T_{PZL}, C = 5 pF

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Figure 3: AC Load Circuit

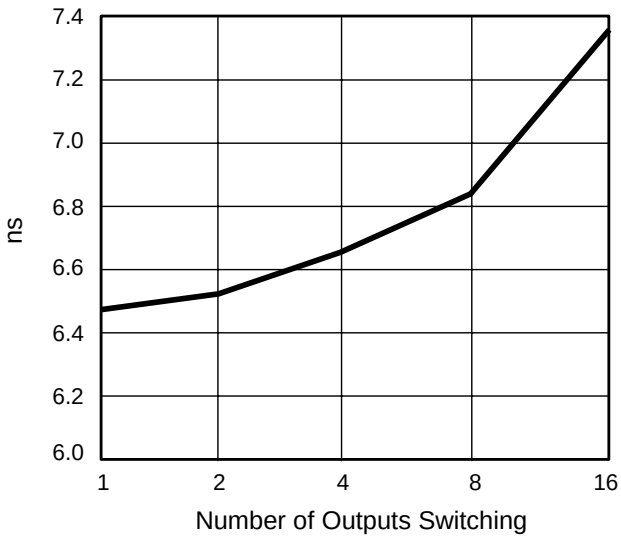

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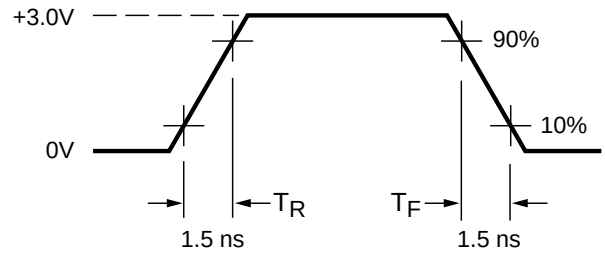
Figure 4: T_{PD2} Outputs Switching



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS013_04_011700

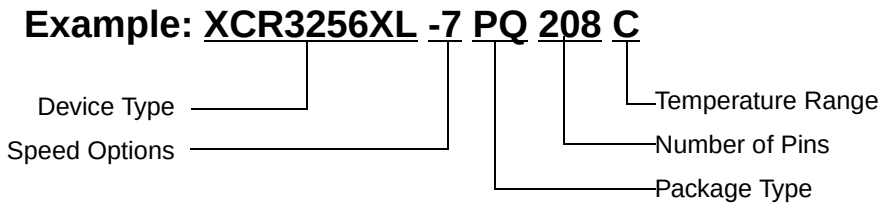
Figure 5: Voltage Waveform

Pin Descriptions

Function	CS280	PQ208	TQ144
A0	E18	6	106
A1	E19	7	
A2	F15	8	104 (TDO)
A3	F17	9	103
A4	F18	10	102
A11	F19	11	101
A12	G16	12	100
A13	G17	13	99
A14	G19	15	
A15	H16	16	
B0	B19	4	107
B1	B18	3	108
B2	B17	206	
B3	A18	205	
B4	A17	204	109
B11	C16	203	110
B12	A16	202	111
B13	E15	201	
B14	D15	199	112
B15	A15	198	113
C0	H17	17	98
C1	H18	18	97
C2	H19	19	96
C3	J16	20	94
C4	J17	21	93
C11	J18	22	92
C12	K16	24	
C13	K17	25	91
C14	K18	26	90
C15	L16	27	
CLK0/IN0	A10	181	128
CLK1/IN1	D11	182	127
CLK2/IN2	C11	183	126
CLK3/IN3	B11	184	125
D0	E14	197	114
D1	D14	196	116
D2	A14	195	117
D3	C13	194	
D4	B13	193	118
D11	A13	192	119
D12	A12	190	120
D13	C12 (TDO)	189 (TDO)	121
D14	B12	188	
D15	D12	187	122
E0	L17	28	89 (TCK)
E1	L18	29	
E2	L19 (TCK)	30 (TCK)	88
E3	M16	31	87
E4	M18	33	86
E11	M17	34	84
E12	N16	35	
E13	N19	36	83
E14	N18	37	82
E15	N17	38	
F0	U10	78	
F1	T10	77	55
F2	W11	76	56
F3	U11	73	
F4	T11	71	60
F11	W12	70	61
F12	U12	69	62
F13	T12	68	63
F14	V13	67	
F15	U13	66	65
G0	P16	39	81
G1	P18	40	
G2	R19	42	80
G3	R16	43	79
G4	R18	44	78
G11	R17	45	77
G12	R15	46	
G13	T17	47	75
G14	T16	48	74
G15	U19	49	
GND	E10	82	52
GND	E11	75	57
GND	E12	185	124
GND	E13	180	129
GND	E5	152	3
GND	E7	134	17
GND	E8	94	33
GND	E9	72	59
GND	G15	50	64
GND	G5	32	85
GND	H15	14	105
GND	H5	200	135
GND	J15	174	
GND	J5		
GND	K15		
GND	K5		
GND	L15		
GND	L5		
GND	M15		
GND	M5		
GND	N15		
GND	N5		
GND	R7		
GND	R8		
GND	R9		
GND	R10		
GND	R11		
GND	R12		
GND	R13		
H0	T13	65	66
H1	W14	64	67
H2	T14	62	68

Function	CS280	PQ208	TQ144
H3	R14	61	69
H4	W15	60	
H11	U15	59	70
H12	V15	58	
H13	T15	57	71
H14	V16	56	
H15	W17	55	72
I0	B1	153	2
I1	C3	154	1
I2	A4	159	
I3	B5	160	
I4	C5	161	143
I11	A5	162	
I12	E6	163	142
I13	D6	164	141
I14	B6	166	140
I15	A6	167	139
J0	D2	151	4 (TDI)
J1	D1	150	
J2	E3	149	5
J3	E2	148	6
J4	E4	147	7
J11	E1	146	8
J12	F5	145	
J13	F3	144	9
J14	F4	142	10
J15	G3	141	11
K0	D7	168	
K1	C7	169	
K2	B7	170	138
K3	A7	171	
K4	C8	172	137
K11	B8	173	136
K12	C9	175	134
K13	B9 (TDI)	176 (TDI)	133
K14	D10	177	132
K15	C10	178	131
L0	G2	140	
L1	G1	139	
L2	G4	138	12
L3	H1	137	14
L4	H3	136	15
L11	H2	135	16
L12	J2	133	
L13	J3	132	18
L14	K2	131	19
L15	K3	130	
M0	W10	79	
M1	T9	80	54
M2	U9	81	53
M3	T8	84	
M4	T7	86	49
M11	W7	87	48
M12	V7	88	47
M13	U7	89	46
M14	W6	90	
M15	T6	91	45
N0	K4	129	20 (TMS)
N1	L1	128	
N2	L2 (TMS)	127 (TMS)	21
N3	L3	126	22
N4	M1	124	23
N11	M3	123	25
N12	M4	122	
N13	N1	121	26
N14	N2	120	27
N15	N3	119	28
O0	V6	92	44
O1	U6	93	43
O2	R6	95	42
O3	W5	96	41
O4	T5	97	40
O11	V5	98	
O12	U5	99	39
O13	W4	100	38
O14	U4	101	
O15	W3	102	37
P0	P1	118	
P1	P2	117	
P2	P4	115	29
P3	R3	114	30
P4	R2	113	31
P11	R4	112	32
P12	T3	111	
P13	U1	110	34
P14	V1	109	35
P15	U2	108	36
PORT_EN	P3	116	13
VCC	V9	83	51
VCC	V11	74	58
VCC	A11	186	123
VCC	B10	179	130
VCC	F2	143	24
VCC	L4	125	50
VCC	V2	107	73
VCC	U8	85	76
VCC	U14	63	95
VCC	T18	41	115
VCC	P15	23	144
VCC	J19	5	
VCC	D17	191	
VCC	C14	165	
VCC	D13		
VCC	C6		

Ordering Information



Speed Options
-12: 12 ns pin-to-pin delay
-10: 10 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
TQ144: 144-pin Thin Quad Flat Package
PQ208: 208-pin Plastic Quad Flat Package
CS280: 280-pin Chip Scale Package

Table 2: XCR3256XL JTAG Pinout by Package Type

Device XCR3256XL	(Pin Number)				
	TCK	Port Enable	TMS	TDI	TDO
144-pin TQ	89	13	20	4	104
208-pin PQ	30	116	127	176	189
280-pin CS	L19	P3	L2	B9	C12

Component Compatibility

Pins		144	208	280
Type		Plastic TQFP	Plastic PQFP	Plastic BGA
Code		TQ144	PQ208	CS280
XCR3256XL	-7	C	C	C
	-10	C, I	C, I	C, I
	-12	C, I	C, I	C, I

Revision History

Date	Version #	Revision
01/21/00	1.0	Initial Xilinx release.
02/10/00	1.1	Updated Pinout table.