Single Event Effects Testing of Xilinx FPGAs

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Introduction

Advanced Field Programmable Gate Arrays (FPGAs) operating at 3.3V were tested for single event effects (SEE) by using the Tandem Van de Graaff accelerator at the Single Event Effects Facility of Brookhaven National Laboratory, Upton, New York. The objective of this experiment was to evaluate the upset and latchup sensitivity of the Xilinx XQR4036XL FPGA fabricated with a 0.35 μm (L_{drawn}) epitaxial CMOS process.

Experimental Setup

At the ion accelerator a beam of monoenergetic particles was selected, namely, fluorine, silicon, titanium, nickel, chlorine, or gold. As shown in Figure 1 these particles are stripped of their charge, accelerated by the Van de Graaff machine, steered and focused into the single event effects (SEE) test chamber.

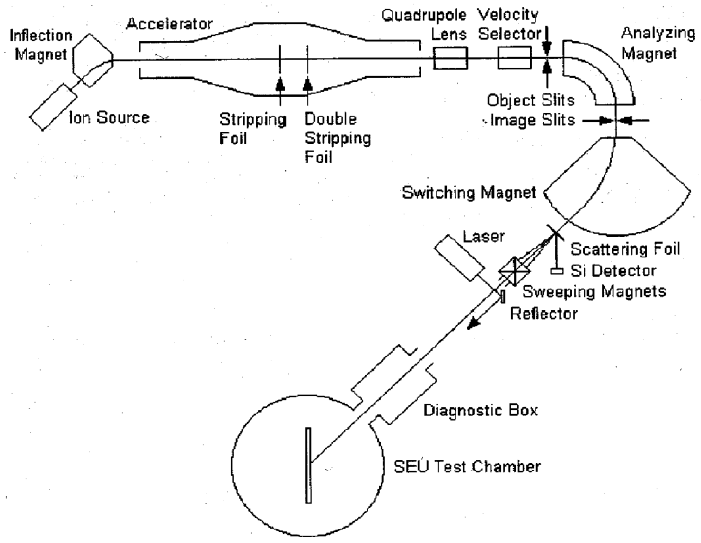

Figure 1. Layout of the beam line.

Inside the test vacuum chamber these ions bombard the device under test (DUT) to characterize and simulate the radiation effects that electronic parts may exhibit in space. The Linear Energy Transfers (LETs) of these particles lie within the range of 3.4 to 120 MeVcm^2/mg. The effects examined include latchup, upset, breakdown, total dose ionization, total dose displacement damage, transients and gate rupture. However, for the devices considered, the attention was focused on upsets and latchup. No parts failed from total dose ionization. In the vacuum chamber the delidded FPGA was mounted on a X-Y-Z translating, rotatable platform. In front of the X-Y-Z platform is an adjustable iris for controlling the spot size. The opening of the iris was set to cover the entire die. A typical run consisted of irradiating an FPGA chip with a beam of selected monoenergetic ions to a flux intensity between 1,000 to 400,000 ions per cm^2 per sec. The lower flux intensity was used for upset measurements, while the higher flux was for latchup testing. During a run, upsets were obtained by irradiating a device to a preselected fluence level before the content of the SRAM was read.

The accumulated fluence per run varied between 10,000 to 1,000,000 ions/cm^2. By dividing the number of single events by the fluence, a value for the cross section at that LET is obtained. In the event that no upsets or latchup are observed, a value of one is used to establish an upper limit to the cross section versus LET curve.

To vary the LET value of the ions, the die was rotated between 0^o to about 50^o with respect to the ion beam. Beyond 50^o the beam began to be shadowed by the walls of the package. Rotation of the part effectively increases the charge deposited by the impinging ions, thus increasing the effective LET. These ions were accelerated to certain maximum energies. To obtain a higher LET measurement, ions of a higher atomic number were chosen. The accelerator has the capability of accelerating helium to gold ions such that a LET range of 1 to 180 MeVcm^2/mg can be achieved.

In the Xilinx FPGA architecture, there is user circuitry and additional built-in control circuitry that is configured to define the user's circuitry and interconnects. In this report the user circuitry will be called the "1 st level or top level circuitry", while the controlling circuitry will be referred as the "basement circuitry." In the "basement circuitry" there are a number of switches that are controlled by 832,472 distributed latches. Accordingly, two types of measurements were made.

The FPGAs were tested on a Xilinx designed fixture board. The parts were powered to 3.3V as measured at the part. Three test configuration, "Empty", "XNOR" and "CRC", were used. The "Empty" configuration is simply a design that loads the configuration latches ("basement circuitry") such that no user logic ("1st level circuitry") is connected. Still the 832,472 distributed "basement" latches are sensitive to SEU in this configuration. In most of the runs, either the "XNOR" or the "Empty" configurations were used. The "XNOR" configuration was representative of a typical, highly combinatorial logic design, while the "Empty" configuration was much more useful for longer exposures or higher fluences such as in the latchup testing. The devices drew about 2 mA in the "Empty" configuration while in the other configurations, the supply current was in the range of 100 - 200 mA.

Results

Parts were tested at an elevated temperature of 125°C to provide the worst case condition for latchup. The XQR parts did not latchup even at a LET of 110 MeVcm^2/mg. The upset cross section for SEUs versus LET data is plotted in Figure 2.

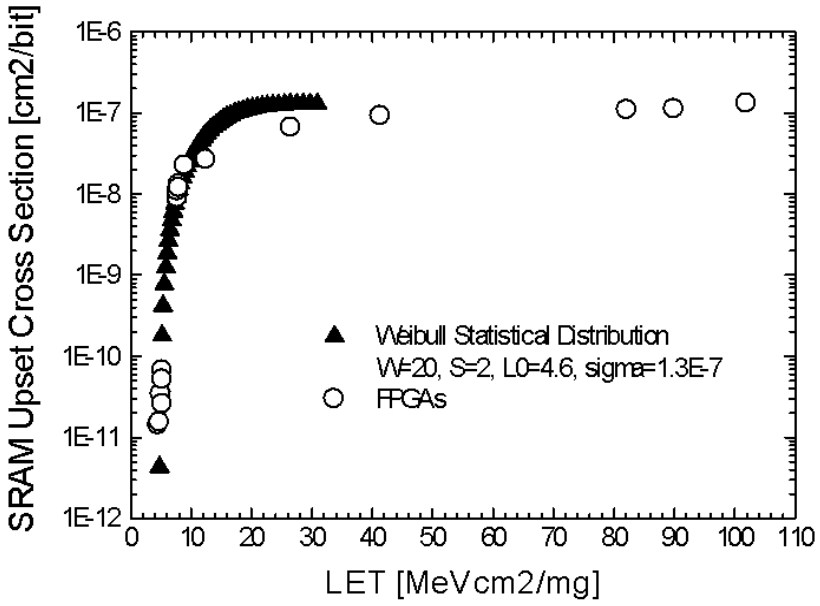

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Figure 2. Xilinx XQR4036XL RAM upset cross section versus LET. The dashed curve uses the Weibull model.

Proton Upset Cross Section Modeling

A proton upset cross section curve was predicted[1] based on the Weibull statistical distribution curve of the heavy ion data in Figure 2. The result is shown in Figure 3.

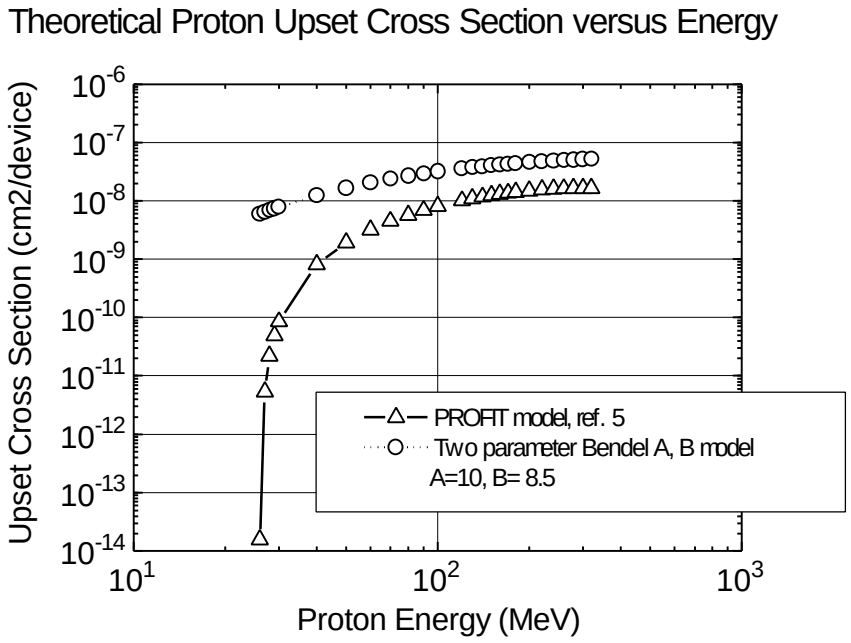

Figure 3. Predicted proton upset cross section versus proton energy from the PROFIT and the two-parameter Bendel models.

According to Figure 3, the two-parameter Bendel model is on the conservative side by a factor of 5. In the PROFIT model, one of the uncertainties is the charge collection depth and also the average diffusion angle of the recoil nucleus. For the plot in Figure 3, although the space charge region is about 0.2 μm, a charge collection depth of 0.6 μm was used.

Upset Rates and Probability of Success Calculations

In order to determine the upset rates for several orbital conditions, Table 1 summarizes the parameters, values and models used in conjunction with the data plotted in Figures 2 and 3.

Table 1. Assumptions used in the single event calculations

- Data shown in Figure 2 was used to calculate the heavy ion upsets from the galactic cosmic and solar flare environments
- Space Radiation 2.5 and CHIME models were used for the galactic and solar flare conditions
- Space Radiation 2.5 was used for the trapped radiation and proton contribution from the flares
- $Bendel_A = 10$, $Bendel_B = 8.5$

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The total probability of success is calculated by using Poisson's probability distribution, $P(k;\lambda t) = e^{-\lambda t} (\lambda t)^k/k!$. In particular, the probability of no upsets in the time interval t is $P(0;\lambda t) = e^{-\lambda t}$, where λ is the upset rate and the total number of bits. The probability of success then becomes:

$$P(\text{success}) = \exp^{(-\text{upset rate x no. of devices x no. of bits/device x mission duration})}.$$

Example, $P\text{success}(\text{trapped protons}) = \exp^{(-2.5\text{E-}7 \text{ x one FPGA x } 832{,}472 \text{ bits/device x 5 yrs x 365 da/yr x } 1/12)}$ where 1/12 is the fraction of the orbit time that the part is exposed to the South Atlantic Anomaly region. Also the full memory was assumed to be sensitive as a worst case rather than 67.5% of which had LETs<15MeVcm^2/mg. The upset rates, the probability of success and the estimated number of upsets over an entire mission are shown in Tables 2 and 3 for a low earth orbit (LEO) at 680 km, 98° inclination. Also, a launch mission from Vandenberg Air Force base is calculated for a 2 hour mission. In the launch mission, it is assumed that the launch will be delayed in the event of a flare sighting, so calculations were not done for that situation. The results show that for the LEO mission of five years, upsets will occur in the SRAM of the FPGA. Table 4 shows the upset rates for a geosynchronous earth orbit (GEO) at 35,000 km, 0^o inclination.

Table 2. Upset rates for several orbital environments

LEO, 680 km, 98° inclination, 100 mil Al shielding						
Trapped p+	Galactic p+	90% w/c p+	ALSF p+	Galactic H.I.	90% w/c H.I.	ALSF H.I.
(ups/bit-day)	(ups/bit-day)	(ups/bit)	(ups/bit)	(ups/bit-day)	(ups/bit)	(ups/bit)
2.50E-7	2.43E-8	2.78E-6	1.78E-4	9.54E-8	1.46E-6	1.44E-6
Launch vehicle from Vandenberg, 100 mil Al shielding						
1.38E-6	2.26E-8	-	-	7.74E-8	-	-

Table 3. Probability of success and total upsets predicted for a LEO 5 year mission

Assumptions: LEO mission = 5 years, two 90% worst case flares per year, one ALSF per mission, 832,472 bits per device, 100 mil Al shielding, (upsets per mission)						
Trapped p+	Galactic p+	90% w/c p+	ALSF p+	Galactic H.I.	90% w/c H.I.	ALSF H.I.
0	0	0	0	0	5.3E-6	0.30
(32 upsets)	(37 upsets)	(23 upsets)	(148 upsets)	(145 upsets)	(12 upsets)	(1 upset)
Launch vehicle from Vandenberg, 100 mil Al shielding, assume a 2 hr mission, a launch is delayed in the event of a flare event						
0.909	0.9984	-	-	0.9945	-	-
(0.096 upsets)	(1.57E-3 upsets)	-	-	(5.4E-3 upsets)	-	-

Table 4. Upset rates for geosynchronous orbital environment

GEO, 35,000 km, 0° inclination, 100 mil Al shielding						
Trapped p+	Galactic p+	90% w/c p+	ALSF p+	Galactic H.I.	90% w/c H.I.	ALSF H.I.
(ups/bit-day)	(ups/bit-day)	(ups/bit)	(ups/bit)	(ups/bit-day)	(ups/bit)	(ups/bit)
-	5.62E-8	3.9E-6	2.49E-4	2.34E-7	7.20E-6	6.98E-6

Recommendations

- Because of upsets in the SRAM, it is recommended that an error detection and correction circuitry be considered. For the LEO example stated above, the worst case bit error rate would be during an anomalous large solar flare (ALSF) of 1/(1.78E-4) = 5.62E3 days-bit/upset / 832,472 bits = 6.7E-3 days per upset = 9.7 minutes between upsets. If one were to scrub every few minutes, this should handle the upsets in the XQR4036XL FPGA.

- It should be noted that according to the analysis the upsets in the above examples are contributed mainly by the protons. Proton cross sections were derived from heavy ion data using two models. There are uncertainties to these calculations, and it would be of importance to verify these numbers in the future if necessary by conducting a proton experiment to measure the proton cross section.

- In our experiment there is an uncertainty in the upset sensitivity between a sequential logic versus a combinatorial logic circuitry. In the future a separate sequential circuit such as a long serial shift register is recommended and a separate combinatorial logic should be tested. By learning about the SEU hardness of the sequential and combinatorial circuitry, other SEU mitigating techniques may be used.

Conclusion

Advanced Field Programmable Gate Arrays (FPGAs) of 3.3V operation were tested for single event effects (SEE) by using the Tandem Van de Graaff accelerator at the Single Event Effects Facility of Brookhaven National Laboratory, Upton, New York. The objective of this experiment was to determine the upset and latchup sensitivity of the Xilinx XQR4036XL FPGAs, fabricated in the submicron range with a L_{drawn} of 0.35 μm using an epitaxial CMOS process. The results showed that no latchup was observed in the XQR devices at elevated temperatures up to 125°C and a LET of 100 MeVcm^2/mg. Upsets were observed in the SRAM of the "basement" logic circuitry. However, the "1st level logic" architecture showed no upsets until about 80 upsets were induced in the "basement" logic circuitry. Upset predictions were made for a LEO and GEO orbit and results indicate that if an EDAC or checksum were implemented with scrubtimes within minutes, it should be sufficient for mitigating single event upsets.

References

[1] P. Calvel, C. Barillot, P. Lamothe, R. Ecoffet, S. Duzellier, D. Falguare, "An Empirical Model for Predicting Proton Induced Upset," IEEE Trans. Nucl. Sci. Vol. 43, No. 6, December 1996.