Radiation Tolerance of High-Density FPGAs

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Abstract

SRAM-based high-density FPGAs offer many advantages in satellite and other aerospace applications. A perceived drawback is the susceptibility of configuration latches to radiation-induced upsets. Heavy-ion testing at Brookhaven have established that the specially processed Xilinx XQR4000XL-family devices exhibited latch-up immunity at LET>100 MeVcm^2/mg at 125 degrees C and a very low probability of soft errors in their configuration-storage latches and user flip-flops.

Xilinx FPGAs offer a unique "readback" capability that can monitor all storage cells on the chip without interfering with the operation of the device in the system. This makes it possible to build triple-redundant systems that can detect and repair a soft error within a fraction of a second, and thus avoid any accumulation of errors.

Field-Programmable Gate Arrays that are customized by the content of latches, so-called "SRAM-based" FPGAs, dominate the high-density commercial, industrial, and military applications of programmable logic. These devices combine the advantages of user programmability (no NRE, fast time-to-market, much lower risk than with mask-programmed ASICs) with specific advantages over EEPROM, Flash, and antifuse-based programmable logic.

SRAM-based FPGAs offer the highest gate capacity (>100,000 gates) and high speed (>100 MHz), very low standby current, and reasonable operating power. This is the result of rapid improvements ("Moore's law") in the standard logic manufacturing processes that these FPGAs have in common with microprocessors. Unlimited reprogrammability in the system is another feature that is gaining importance as users get accustomed to such possibilities, and as system modifications and upgrades become more important and more common.

Xilinx is the leader in the FPGA market, shipping over 20 million FPGAs per year. Xilinx devices are known for excellent quality and reliability, and they are being designed in by over 30,000 designers worldwide.

Despite this commercial success, and despite a significant presence in the Hi-Rel and avionics market, Xilinx has in the past captured few designs destined for space applications. This can be attributed to Fear, Uncertainty, and Doubt (F.U.D.) on the part of the potential users, who are, however, very interested in higher-density and reprogrammable FPGAs. There was F.U.D. about the stability and reliability of configuration data stored in latches, since Xilinx offered no specially hardened devices, and data about latch-up immunity and single-event upset rate was not readily available. Designers had accepted antifuse-based FPGAs, because their logic and routing is determined by open or closed antifuses, which are considered fairly immune to radiation-induced upsets. The latches and flip-flops in these antifuse devices are, of course, equally sensitive to radiation-induced upsets (soft errors) as the latches in SRAM-based FPGAs.

In late 1997, Xilinx decided to investigate the probability of radiation-induced upsets as well as the likelihood of latch-up problems in XC4000-series devices. Ericsson Saab Avionics, the Swedish manufacturer of advanced fighter plane electronics, conducted a series of neutron-radiation tests, with help from Xilinx. They tested XC4010E and XC4010XL commercial devices at three increasingly higher levels of neutron radiation, from 10 to 100 MeV. They found no latch-up and a total of six single-event upsets only at the highest radiation test levels. The SEU cross-section was calculated as 1.3 to $4.4 \cdot 10^{-15}$ cm^2/bit, which is an order of magnitude below the lowest limit reported for commercial SRAMs.

SAAB concluded that:

"An estimated SEU frequency at aircraft altitudes can be calculated. At 10 km altitude at 60 degrees north (Sweden) the SEU rate is on average one bit error per 1.3 million flight hours for the XC4010E, and one bit-error per 275,000 hours for the XC4010XL. SRAM-based FPGAs show a low susceptibility to single event upsets caused by high-energy neutrons. No permanent effects were detected, reconfiguration of the device was sufficient to regain full functionality after the occurrence of a single event upset. We conclude that these SRAM-based FPGAs can be used without limitation in the atmospheric radiation environment, contrary to SRAM memories where precaution in the use is necessary because of neutron induced SEU."

Encouraged by these results, Xilinx aimed for the more demanding applications in Low Earth Orbiting Satellites (LEOs). To avoid any possibility of latch-up or micro latch-up, Xilinx made some processing modifications : All rad-hard devices in the XQR series are now manufactured on wafers with a 7 micron epitaxial layer, and the subsequent implant levels are adjusted to achieve the desired CMOS threshold

levels and performance. There is no change in the structure, logic or circuit design, compared to standard devices.

Total-dose testing of the newer, larger and faster 3.3-V XQR4036XL devices at Lockheed, Sunnyvale, CA proved hardness beyond 60,000 rads of total ionizing dose (TID).

In May 1998 heavy-ion tests were performed at the Brookhaven National Laboratories, with Dr. Gary Lum of Lockheed in Sunnyvale, CA assisting in the planning and the interpretation of the tests.

The Xilinx devices were programmed (configured) with a defined pattern. During exposure to radiation, this pattern was read back again and again, and all readbacks were compared. Any change in the readback data was recorded as an SEU error. There was not a single case of latch-up or micro-latch-up, even at 125 degrees C.

The devices were exposed to LETs up to 120 MeVcm^2/mg. For a five-year LEO mission at 680 km, 98 degr. inclination, with two 90%-worst-case flares per year, and one anomalous large solar flare, and with 100 mil Al shielding, a total of 398 single-event upsets were calculated (148 due to the ALSF, 145 due to galactic heavy ions, 35 due to the ten 90% worst-case flares). Space Radiation 2.5 and CHIME models were used for the galactic and solar flare conditions. Space Radiation 2.5 was used for the trapped radiation and proton contribution from the flares. Statistically, this means one SEU bit-upset (out of the 832,528 bits in the XQR4036XL) every 110 hours.

For more information, see
http://www.xilinx.com/products/hirel_qml.htm,
and click on *Radiation Hardened Products.*

The Swedish MTBF results of >275,000 hours at 33,000 feet are perhaps acceptable without additional enhancement, but the MTBF of 110 hours in the space environment will most likely require some kind of error-correction.

The following paragraphs describe one out of many different methods to mitigate the effect of single-event upsets.

Xilinx FPGAs allow the sequential read-out (Readback) of all configuration data, even the original or the present state of the user latches or flip-flops. This full readback operation takes only a fraction of a second, and does not interfere with the normal operation of the device. Running a continuous sequence of readback operations makes it thus very easy to detect any soft or hard errors, either by comparing the readback bitstream against a known-good stream, or against the readback from another FPGA with identical configuration, operating in synchronism.

Two FPGAs can thus be used to detect the bitstream position of any random error, but it takes three FPGAs to identify the error.

Triple-Redundancy Error Detection:

Three FPGAs are connected in parallel, but with individual output enable pins, and only one of the FPGAs is output-enabled at any time. The three FPGAs are configured identically and operate in synchronism. A small controller initiates simultaneous bit-serial readback from all three FPGAs, and it compares the three bitstreams. If no error is found in any bit position, there was no SEU, and a new readback is started immediately. The readback is transparent to system operation, which, therefore, continues at full speed. When, for any bit position, only two readback streams are identical, the third device is flagged, and, if it is the active device, its outputs are immediately disabled, and one of the redundant devices is enabled instead.

Error checking continues with all devices, even the flagged one(s) participating in the voting. At the next convenient breakpoint, system operation is then stopped, and the error is corrected. This simple strategy covers 100% of all single and double upsets, 78% of all triple, and even 55% of all quadruple upsets that occur before the errors are corrected. (Assuming that errors occur at random locations in the chip and thus the bitstream.)

Triple-Redundancy Error Correction:

After detecting an error, the device operation continues for seconds or minutes until it reaches an appropriate breakpoint. Then the error is corrected in one of two ways:

Alt. 1: All devices are configured from the original source. This loses the content of all user-flip-flops.

Alt. 2: The faulty device is reconfigured through readback from the others. The system thus restarts with identical configuration and user data in all three devices. The whole repair operation can take as little as one second.

Conclusion:

Xilinx now offers radiation-hardened devices of up to 62,000 gate complexity. These devices tolerate a total dose of 60,000 rad, are immune to latchup at 100 MeV (125 degrees C), and are resistant to single-event upsets. Xilinx FPGAs offer efficient ways to detect and correct soft errors caused by single event upsets:

- *Readback for error detection,*
- *Reconfiguration for error correction*

In late 1998, Xilinx will introduce a family of substantially larger and faster devices (one million gates, 160 MHz), called Virtex. Radiation-hardened versions of this family are planned for 1999.

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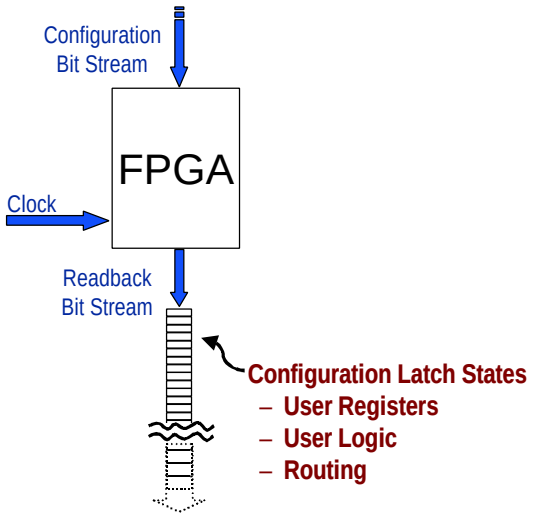
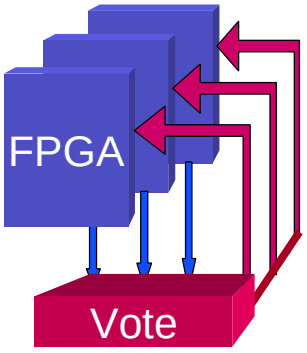
Technical Data for XC4010, XQR4013, XQR4036, XQR4062

Device	Gate Count	LUTs	User Flip-Flops	Configuration Bits
XC4010	10,000	800	1120	178,144
XC4010XL	10,000	800	1120	284,421
XQR4013XL	13,000	1152	1536	393,632
XQR4036XL	36,000	2592	3168	832,528
XQR4062XL	62,000	4608	5376	1,433,864

Readback Error Detection



Readback Error Detection



Readback Error Detection