Gamma-ray Large Area Space Telescope (GLAST) Tower CPU

Sapphire Computers Inc. recently designed the prototype Tower CPU for the GLAST space telescope program, using XC4000XL FPGAs.

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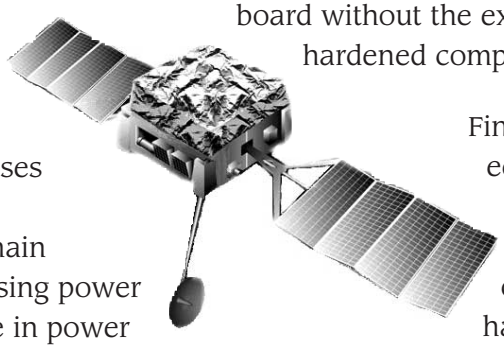
GLAST will provide astronomers and physicists a direct view of galactic gamma-ray sources in the 10MeV to 300GeV range (such as black holes, neutron stars, blazars, and pulsars). The 16 Tower CPU (TCPU) cards planned for the telescope will provide high-speed parallel processing of the vast amount of data captured by each of 16 sensor arrays.

The GLAST TCPU provides a very high level of computing power for a space processor board design, to handle the bandwidth of the data stream from the sensor arrays. It incorporates a 100MHZ PowerPC 603e with 64-bit data paths to the level 2 (L2) cache and main DRAM memory. A split-level bus architecture ensures fast accesses to the L2 cache while allowing simultaneous DMA access to the main memory array. This level of processing power does not come without an increase in power consumption, so the TCPU design includes power saving sleep modes and allows programmable reduction of the bus clock rates. To provide solid operation in a space environment, the L2 cache, the flash program store, and the DRAM memory are all error correction coded.



Specifications

The prototype TCPU is a VME card running the VxWorks operating system, with one megabyte of L2 cache, 256 megabytes of 64-bit-wide Reed-Solomon corrected DRAM, Flash memory, serial I/O, and Ethernet capability. The prototype board's goal is to give the GLAST software developers a development platform that is a functional equivalent to the final space-qualified board without the expense of using radiation hardened components.

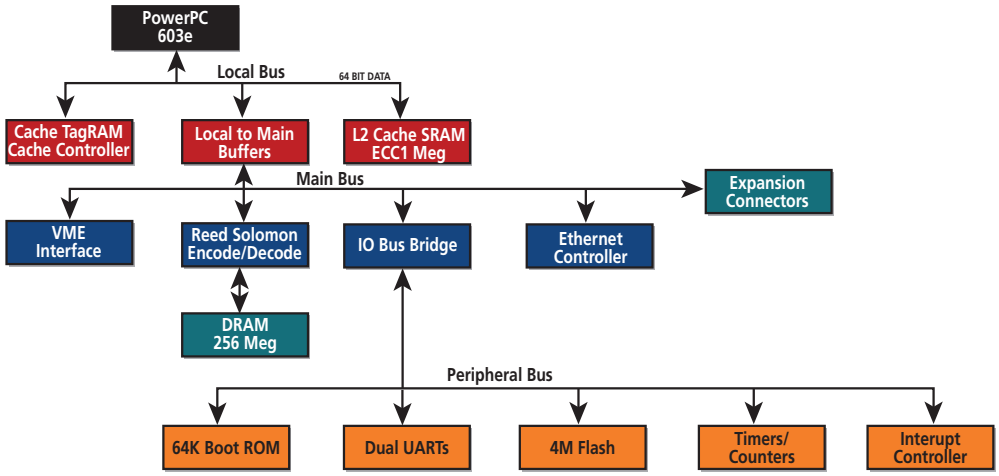
Finding space-qualified device equivalents turned out to be one of the more challenging aspects of this design. There are few rad-hard component vendors and very few high integration devices available in radiation hardened versions. As a result, a number of system functions that are normally available in ASICs had to be custom designed in FPGAs. One of these is the

About Sapphire Computers

Sapphire Computers Inc. specializes in high performance digital microprocessor and FPGA design. Xilinx FPGAs are used to reduce system cost, to shorten the time to market, and to allow flexibility for updates and modifications. We are a Xilinx XPERT partner delivering solutions that range from optimizing a module in an FPGA design to a complete turnkey system. We also offer Xilinx-certified training in FPGA and advanced FPGA design.

PowerPC's companion L2 and cache memory controller, the MPC106. While the 603e processor is relatively rad-hard, the MPC106 is not.

All the memory and cache control functions had to be implemented in programmable logic. Additionally the interrupt controller, the system timers, the DRAM error corrector, and the DMA arbiter all had to be custom designed in FPGAs. Xilinx XC4000XL FPGAs were chosen because of their flexibility and ease of debugging.



TCPV Block Diagram

The functions were divided into three FPGAs on the board. An XC4036XL is used to implement the L2 cache and memory controller which also does sleep and clock speed control. Another XC4036XL is used to implement the peripheral bus controller incorporating system timers, interrupt controller, and DMA arbiter. The third FPGA is an XC4062XL which does the Reed-Solomon EDAC (Error Detector And Corrector) function for the 96-bit-wide DRAM array. The EDAC is capable of correcting up to two four-bit errors in each 96-bit word.

Conclusion

The typical development flow for a space design is to prototype the system using commercial grade parts and RAM-based FPGAs to allow low development cost, easy debugging, and easy upgrading. The next step traditionally was to migrate to space grade parts and away from RAM-based FPGAs. The recent availability of Xilinx QPRO™ devices means that GLAST may be able to stay with RAM-based FPGAs for flight as well. This would allow unprecedented flexibility, allowing during-mission hardware updates and system failure workarounds.

For more information on GLAST please see the Stanford GLAST website: http://glast.stanford.edu.