How Spartan Series FPGAs Compete for Gate Array Production

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Application Note by Ashok Chotai

Summary

This application note discusses the enormous progress made by FPGAs in the areas of technology, low-price and performance. It discusses the major advantages of using FPGAs over traditional gate arrays, which makes FPGAs the best high-volume production solution available today.

Xilinx Families

Spartan and SpartanXL

Introduction

The ASIC industry's claim that gate arrays are always more cost–effective than FPGAs in production has been reversed. The current generation "ASIC Replacement" FPGAs offer competitive production pricing in addition to providing the benefits of fast development-to-production and in-system reprogrammability. Gate array users must now analyze the latest FPGAs to determine the best ASIC technology for their upcoming design and production needs.

FPGAs Contend for Mass Production

The Xilinx Spartan Series (see Table 1) was created to displace low-end (up to 40K system gates) ASICs in volume production by providing the advantages of FPGAs at competitive prices. Using an advanced logic-process technology, the Spartan Series substantially reduced die size over the previous generation FPGAs while measurably improving gate-area density and performance. Although FPGAs have historically lagged the ASIC industry by one or two process generations, the current Spartan series FPGAs surpass most of today's gate arrays by using a multi-feature size 0.35/0.25 µm (submicron) technology. In the past a larger die size prevented FPGAs from being cost competitive.

Future Xilinx FPGAs will use an even more advanced 0.18 µm process and attain 1 million system gates. Because FPGAs contain more transistors (75 million) than the Pentium II microprocessor (about 8 million), independent wafer foundries have chosen these complex devices to debug new fab processes, replacing formerly used DRAMs. This should ensure that Xilinx FPGAs remain on the leading edge of process technology for years to come. (See Figure 1).

SpartanXL Closes the Price Gap of FPGAs & ASICs

The 3.3-Volt SpartanXL family is the lowest cost FPGA series in the industry. It incorporates ASIC-like features such as dual-port synchronous RAM and supports system frequencies over 80 MHz. With competitive volume pricing, the SpartanXL family attains a pad-limited die size and cost equivalence to gate arrays of up to 205 I/O pins. The term "pad-limited" refers to a die that is shrunk to the limits imposed by the bonding pads. Although gate arrays still maintain a denser architecture than FPGAs, the Spartan series is able to effectively compete for production based upon I/O count. For example, the 160 I/O SpartanXL XCS20XL, shown in Figure 2, has the same die size and cost as a 160-pin I/O 0.5 µm gate array.

Because of very low power consumption, SpartanXL devices can achieve a low manufacturing cost by using the less expensive high-volume plastic packages. In addition, the test methodology has been streamlined with more efficient test hardware, built-in self-test features and shorter test times. The manufacturing and die savings eliminate former cost barriers and provide the means for SpartanXL devices to move beyond prototyping and provide a compelling alternative for mass production.

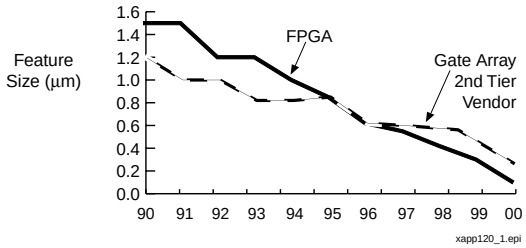

Figure 1: Spartan Series Surpasses Gate Arrays in Process Feature Size

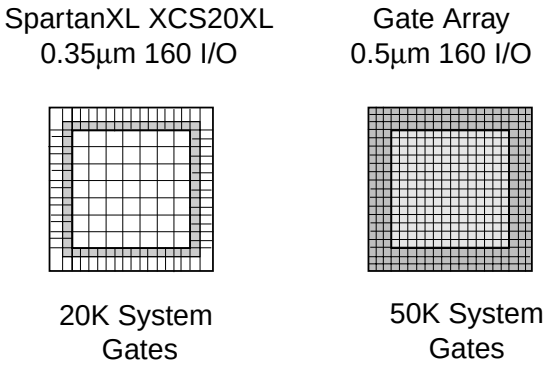

Figure 2: SpartanXL Device Matches Die Size With Gate Array for Pad-Limited Devices

Advanced Process Penalizes Gate Arrays

Mask gate arrays incur a large penalty when migrating to deep submicron processes. Because transistors have shrunk much faster than metal lines, smaller transistors drive larger and longer metal lines. The result is that interconnect delay now dominates gate delay. (See Figure 3) Minimizing interconnect delay requires adding metal mask layers to create more routing resources. As an example, each additional mask layer for the 0.35 µm process, unfortunately, costs the ASIC supplier up to $15K, and it also

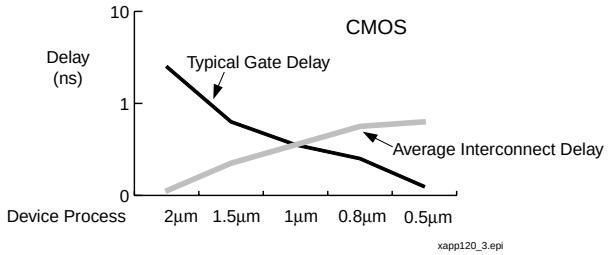

Figure 3: Relative Importance of Interconnect vs. Gate Delay

extends the prototype fab time. Since most ASICs today are fabricated with 4-5 metal layers, a $60-75K cost for masks easily results in over $100K non-recurring engineering (NRE) charges to the customer! In contrast, the 0.35 µm FPGA does not incur the same penalties of higher cost or longer turnaround time because each mask is created only once to serve hundreds of different customers over the life-time of the device. A deep submicron gate array loses much of its value when NREs are more than $100K and prototype time is extended by a few weeks.

As process technology increases wafer and mask costs, the gate array industry is undergoing a fundamental transition. Some major suppliers, like Motorola and LSI Logic, have left the gate array business to re-focus on high-end standard cell products that support system-on-chip designs. Dataquest forecasts gate array revenues will decline substantially over the next several years, while PLDs and standard cells are projected to be the primary growth technologies.

Table 1: Xilinx Spartan Series FPGAs

5-Volt Devices	**XCS05**	**XCS10**	**XCS20**	**XCS30**	**XCS40**
3.3-Volt Devices	**XCS05XL**	**XCS10XL**	**XCS20XL**	**XCS30XL**	**XCS40XL**
System Gates	2K-5K	3K-10K	7K-20K	10K-30K	13K-40K
Logic Cells	238	466	950	1368	1862
Max Logic Gates	3,000	5,000	10,000	13,000	20,000
Flip-Flops	360	616	1120	1536	2016
Max RAM bits	3,200	6,272	12,800	18,432	25,088
Max User I/O	77	112	160	192	205
System Performance	80MHz	80MHz	80MHz	80MHz	80MHz

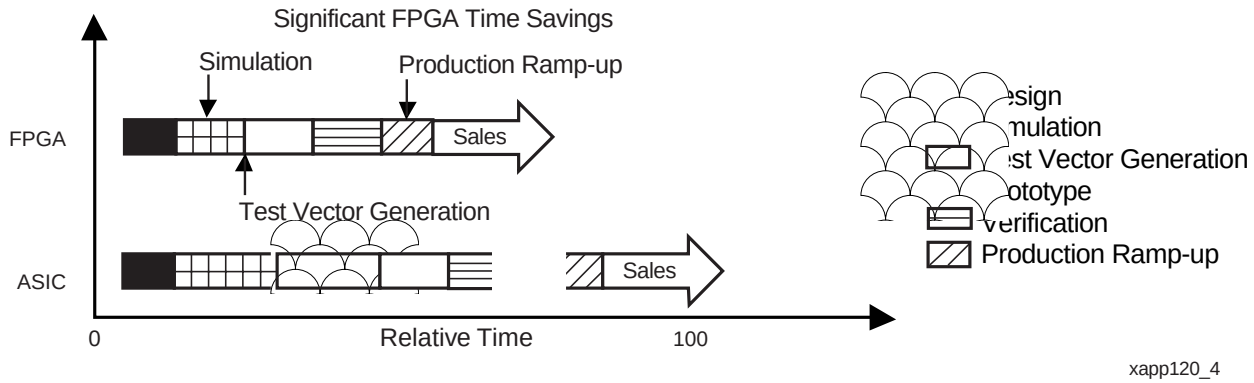

Figure 4: FPGAs Versus ASICs Design Time Savings

Spartan Series Advantages Over Gate Arrays

Because today's product life cycles are so brief (12-18 months), it is vital to attain the best development-to-production cycle time. Programmable logic provides both rapid prototyping and a quick ramp to full production.

With in-system reprogrammability, FPGAs demonstrate the fastest development time of any ASIC technology. Early availability of prototype hardware means less time spent in extensive simulation. Rapid prototyping also facilitates concurrent engineering and real-time debugging of applications such as video, graphics, and sound cards. Prototyping with FPGAs enables bugs to be eliminated before they reach costly silicon. And since Xilinx FPGAs are 100% factory tested, the usual scan insertion, test vector generation and Automatic Test Pattern Generation (ATPG) services are optional for lower density FPGAs. (Xilinx recommends test vectors, however, for the higher density FPGAs.)

Production Parts Available When Development is Complete

Fast ramp-to-production is another primary advantage of programmable logic. (See Figure 4) After development and beta testing, early initial production can be critical to product acceptance. Sales channels can be quickly stocked to satisfy initial customer demand and start the new product revenue flow. With the standard ASIC 8-16 week production schedule, a 2-4 months sales delay may substantially decrease revenues and profits throughout the life of the product. Because the lead-time for FPGA production quantities is typically only 0-4 weeks, market penetration is immediate. The well-known McKinsey study found that a 6 month delay costs one third of the profits over the life time of the product.

Supply–Chain Management

In full production, programmable logic provides the additional advantage of Just-In-Time (JIT) deliveries from distribution stock or manufacturer's inventory. Because masked ASICs are "custom" products, supply-chain management is more complex and expensive. ASIC distribution stocking arrangements can also be expensive and ASIC factory deliveries can sometimes be affected by fab yields, assembly mishaps, and tester down time.

FPGAs eliminate the risk of missed deliveries and safeguard inventory and work-in-process if design changes occur or demand is weak. Many ASIC users find that an FPGA with a slightly higher unit cost may provide more value and lower overall system costs than the masked ASICs. A lower unit cost does not necessarily reduce total system costs.

Costly FPGA to ASIC Conversions

It is more difficult today to cost justify FPGA to ASIC conversions because of low cost FPGAs and quickly changing markets. Conversion to an ASIC means losing FPGA advantages and incurring design risks. Added costs such as NREs, conversion fees, silicon iterations, test vector creation for adequate fault coverage, board re-layout, new device characterization, loss of capability for quick changes, and the delay of engineering on a new project likely negates a slight unit cost difference.

FPGA to ASIC conversion time to production typically exceeds 4 months. The conversion time frame is often: conversion - 3 weeks, prototype - 3 weeks, full production - 10 weeks. Therefore a total of 16 weeks is needed before production is ramped and the transition from programmable to masked ASIC may begin. With either a short product life or a required mid-life product enhancement, many conversions cannot be cost justified.

In addition, FPGA users have no minimum order quantity. Cash and credit availability is preserved when there are no large gate array order commitments and the IC stock levels

are minimal. Small and emerging companies will appreciate conserving their credit availability and valuable working capital for product development, test and marketing.

There are compelling advantages to use programmable logic in both development and in production. Today's FPGAs support standard Verilog and VHDL design flows that help in the transition of ASIC designs to programmable logic. Advanced process technology has leveled the playing field, and allowed FPGAs to be very competitive with low-density gate arrays. When ASIC users now consider competitive pricing, time-to-production, and reprogrammability, the preferred ASIC technology becomes the FPGA!

Refer to the Xilinx web site (http://www.xilinx.com) for latest product information.

Additional Information

- Spartan Series datasheet on the Xilinx web site (http://www.xilinx.com/partinfo/spartan.pdf)
- Xilinx Application Note: XAPP119 Adapting ASIC Designs for Use WIth Spartan FPGAs (http://www.xilinx.com/xapp/xapp119.pdf)

The Programmable Logic Company℠

Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
U.S.A.
Tel: 1 (800) 255-7778
or 1 (408) 559-7778
Fax: 1 (408) 559-7114
Email: hotline@xilinx.com
Web: http://www.xilinx.com

North America

Irvine, California
Tel: (949) 727-0780

Englewood, Colorado
Tel: (303) 220-7541

Sunnyvale, California
Tel: (408) 245-9850

Schaumburg, Illinois
Tel: (847) 605-1972

Nashua, New Hampshire
Tel: (603) 891-1098

Raleigh, North Carolina
Tel: (919) 846-3922

West Chester, Pennsylvania
Tel: (610) 430-3300

Dallas, Texas
Tel: (972) 960-1043

Europe

Xilinx Sarl
Jouy en Josas, France
Tel: (33) 1-34-63-01-01
Email: frhelp@xilinx.com

Xilinx GmbH
München, Germany
Tel: (49) 89-93088-0
Email: dlhelp@xilinx.com

Xilinx, Ltd.
Byfleet, United Kingdom
Tel: (44) 1-932-3494013
Email: ukhelp@xilinx.com

XILINX Italia
Via Alberto Mario 26
20149 Milano
Italia
Tel: (39) 02-49-877-16
FAX: (39) 02-49-877-27
Email: roberto.rosaia@xilinx.com

Japan

Xilinx, K.K.
Tokyo, Japan
Tel: (81) 3-5321-7711
Email: jhotline@xilinx.com

Asia Pacific

XILINX Asia Pacific
Unit 4312, Tower II
Metroplaza
Hing Fong Road
Kwai Fong, N.T.
Hong Kong
Tel: 852-2-424-5200
FAX: 852-2-494-7159
Email: hongkong@xilinx.com

XILINX Korea
Rm. 901, Sambo-Hojung Bldg.
14-24, Yoido-Dong,
Youngdeungpo-Ku
Seoul, 150-715, Korea
Tel : 822-761-4277
FAX : 822-761-4278
Email: korea@xilinx.com

Xilinx Taiwan
Rm. 1006, 10F, No.2. Lane 150
Sec. 5, Hsin Yin Rd.
Taipei, Taiwan, R.O.C.
Tel: 886-2-2758-8373
Tel: 886-2-2758-8353
Fax: 886-2-2758-8367