

KAT GmbH *Using Xilinx XC5210 FPGAs For a Dual Incremental Encoder and Synchronous Serial Interface Controller (DISSIC)*

KAT GmbH recently used the Xilinx XC5210-PC84 FPGAs to create a Dual Incremental Encoder and Synchronous Serial Interface Controller. DISSIC interfaces to two encoder types — **incremental and absolute**.

The incremental encoder interface takes in A, B, and R pulses from an encoder, filters the spikes, decodes, and counts. The up/down counter is 32 bits wide and can be preloaded with a user value for a reference position. The position value in the counter can be stored into a register either via a software command or a hardware signal. Other registers can be used to store the counter values on the activation of some external signals.

The incremental encoder interface can also be used for digitizing. In this case one axis moves to a target position, while the other axes store the position of their respective counters. The maximum input frequency of the A, B pulses is around 950 KHz.

The absolute encoder interface implements the Synchronous Serial Interface. DISSIC provides the

clock for the position data transfer; the position data can be 32 bits wide. When the position data is less than 32 bits, the remaining bits can be used to receive information such as parity, power fail, or other check bits. The position data can be located anywhere within the 32 bit data and can be coded in either binary or gray codes. The data transfer can be initiated either by a software command or a hardware signal. Maximum clock frequency is 400 KHz.

DISSIC has a 16 bit, Intel-style microprocessor interface and is available in two implementation versions — V2.0 has one absolute and two incremental encoder interfaces, and V2.1 which has two absolute encoder interfaces.

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