Ten-Digit Fully Synchronous BCD Counter Runs at 87 MHz

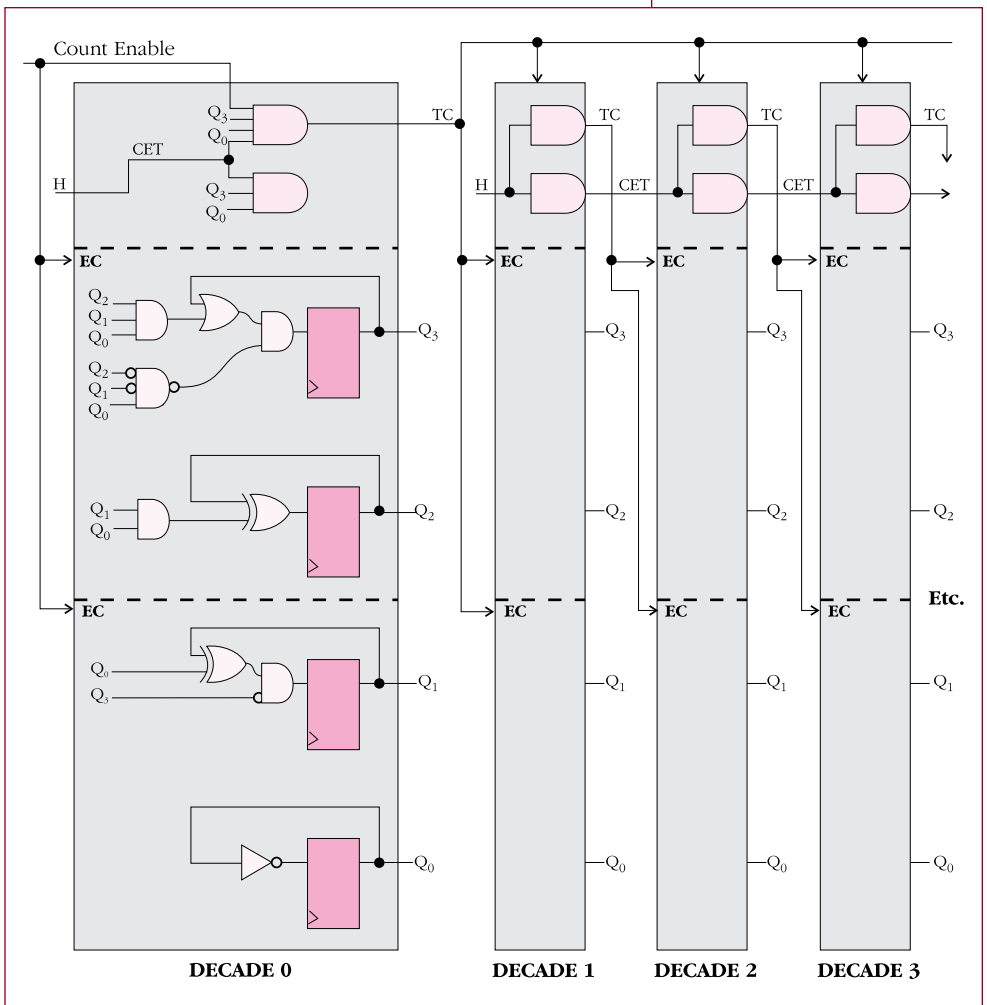
A binary-coded-decimal (BCD) counter design that operates at an impressive 87 MHz under worst-case conditions has been implemented in an XC3100A-09 FPGA device.

This synchronous BCD counter uses the count-enable-parallel/count-enable-trickle (CEP/CET) method of fast carry expansion *(as first introduced in 1969 in the Fairchild 9310, and made popular by the 74160-series of TTL-MSI counters.)* The decoded terminal count of the least-significant decade, ANDed with the incoming count enable control signal, drives the count-enable-parallel (CEP) inputs of all higher-order decades in parallel, effectively preventing them from incrementing while CEP is Low. This gives the conventional ripple-carry CET-chain nine full clock periods to settle. The count enable control input can start and stop this counter on any clock.

However, this design cannot be modified to be loadable, and even a modification to down-count results in slower speed. *(For more complex counters, the XC4000E family is a better choice.)*

The 10-digit counter occupies 29 CLBs. When floorplanned on three horizontal rows of CLBs, one BCD digit per column, using a horizontal longline for distributing CEP, this fully synchronous counter has been simulated to operate under worst-case conditions at

- A maximum of 87 MHz in an XC3130A-09 device
- A maximum of 41.5 MHz in any XC3100A-5 device
- A maximum of 40.0 MHz in any XC3000A-6 device



The design was also bench-tested in an XC3142-09 device, and ran at a clock rate of up to 146 MHz at room temperature and nominal V_{CC}. ◆

Look for the design files on the Xilinx technical Bulletin Board (applications area, filename BCDCNT.ZIP).