What's New in V2.1i for XC9500 CPLDS?

Our latest Alliance Series and Foundation Series software, v2.1i, offers an uncompromising level of performance while improving ease of use.

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The Xilinx Alliance Series™ and Foundation Series™ software provides a complete development environment for Xilinx CPLDs (and FPGAs). The v2.1i improvements for CPLDs include:

Ease of use enhancements

- ChipViewer - the new, interactive, graphical device constraints editor
- Implementation template enhancements

Performance enhancements

- New "Balanced" optimization for even logic distribution and pin placement
- More aggressive "Speed" optimization for the fastest clock speeds possible
- Complete XC9500/XL/XV fitting and programming file support
- XC9500XL-based tutorials along with CPLD quick install
- STAMP models and XFLOW support
- XPORT capability in Foundation

Ease of Use Enhancements

There are many new ease-of-use improvements in the v2.1i release, including the following.

ChipViewer

ChipViewer is our new graphical constraints editor; an interactive way to view and control the logic design routing within a Xilinx CPLD. It also allows you to either pre-assign the pinout or see exactly how the design is routed in your selected device. This provides a more intuitive approach to assigning constraints within a CPLD. Additionally, it allows you to verify and trace the actual design's routing and resource usage. See the companion article on page 48.

Implementation Templates

Xilinx makes it easy for you to select how your design should be routed, by using a new GUI conveniently located under the Options menu in the Alliance Series and Foundation Series Design Managers, as shown in Figure 1. This GUI offers you a choice of four different optimizations, and each forces the fitter to route the design with different end objectives:

- Area - Provides the best density optimization.
- Speed - Provides the best possible clock frequency response.
- Balanced - Provides even logic distribution and best pin-locking; new in v2.1i.
- User Defined - Provides full control over design implementation options.

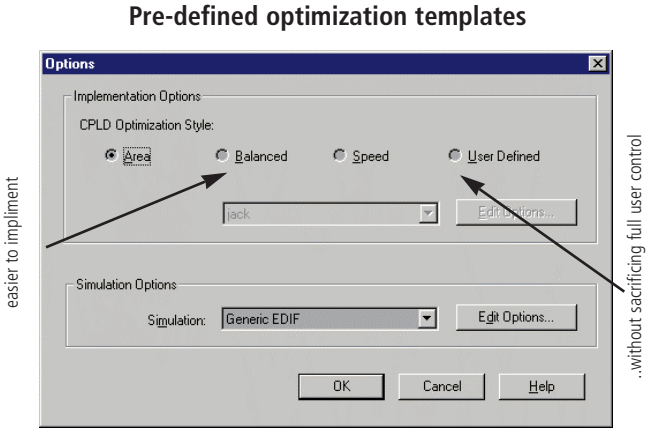


Figure 1 - CPLD Implementation Template Settings Under "Options"

Performance Enhancements

There are many new performance improvements in the v2.1i release, including the following.

Complete XC9500/XL/XV Fitting and Programming File Support

The v2.1i software now includes full fitting, programming, and file support, not only for the XC9500/XL families but also for the newer 2.5V XC9500XV product.

XC9500XL-based Tutorials Along with CPLD Quick Install

The XC9500XL is now being used as the basis for Xilinx CPLD tutorials. Additionally, The Alliance Series and Foundation Series software provide the option for a "CPLD-only" quick install (without the FPGA tools) to help speed you on your way.

STAMP Models

STAMP models are useful in specifying pin-to-pin timing delay and constraint information for components. Xilinx is the first PLD supplier to output the Stamp file format from its implementation software.

XFLOW Support

XFlow is a non-graphical tool that encapsulates the latest implementation and simulation flows. It is device independent and has a simple interface to the Xilinx tools that is flexible, extensible, and user customizable.

XPORT Capability in the Foundation Series

XPort 4.1 converts ABEL designs to Verilog or VHDL format. ABEL test vectors are converted as well and put in a separate test bench file. XPort 4.1 also converts AHDL designs to Verilog or VHDL format. Hierarchical AHDL designs are also supported. Each AHDL module file will have a resulting Verilog or VHDL output file.

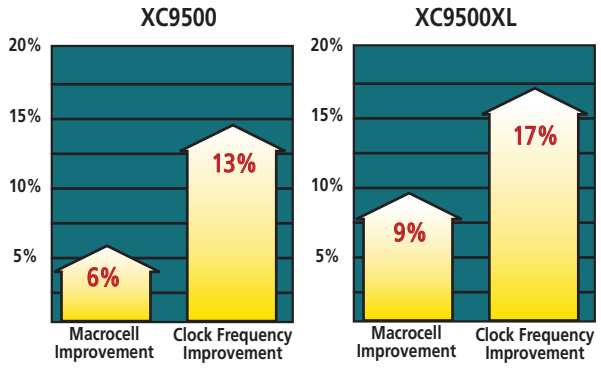
New v2.1i Benchmark Tests

Xilinx recently completed a benchmark study comparing our previous implementation tools (v1.5i) with our latest v2.1i release. These benchmarks clearly show that the new v2.1i software has once again raised the industry standard in both ease-of-use and performance improvements.

Fifty-seven VHDL and Verilog designs were compiled and benchmarked. No additional timing constraints were used during the EDIF netlist creation. The various design EDIFs were used as the input files to both the v1.5i (service pack 2) and v2.1i fitter tools. Two different implementations were run using v1.5i. The first implementation attempted to fit the EDIF file using an area optimization algorithm. The second implementation used a speed optimization algorithm. In v2.1i the same two implementations were run along with a third, the balanced implementation.

The output results were compared for area, speed, and default settings. The implementation comparisons were performed for both the 5V CPLD device families (XC9500) and again for the 3.3V /2.5V device families (XC9500XL/XV).

The results were impressive; the 57 designs were compared on a design-by-design basis with the difference between them computed as a percentage. The range of improvement in clock frequency was 3% to 96%. Figure 2 shows the average change for both the XC9500 and XC9500XL/XV. As you can see, the new v2.1i software generated fewer macrocells and product terms while increasing the design speed.



New aggressive speed optimization dramatically improves clock frequency response.

Notes:
- Average % improvement for designs affected using the speed template
- Range of improvement in clock frequency: 3% to 96%
- 57 test designs, 13 affected by V2.1i improvement

Figure 2 - v2.1i vs. v1.5i Software Benchmark Results

Conclusion

The new v2.1i release of Xilinx Alliance Series and Foundation Series software sets new standards of excellence in quality of results, ease-of-use, and features. Partnered with an XC9500 architecture rich in features, and the industry's lowest CPLD prices, Xilinx clearly provides the industry's best CPLD solution.