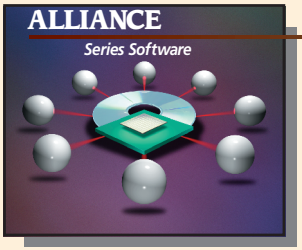

XILINX®

Cadence•Xilinx Concept-HDL (PIC) Design Flow

Concept Unified Schematic Library

Schematic Design

HDL Design

Design Entry
Concept-HDL

Verilog
UNIFIED
Simulation Library

Verify Logic
CFG_Verilog

Verilog

Mixed Design

Timing Requirements

Simulator
Verilog-XL

SYNTHESIS
Synplify

Verilog
Testbench

Verify Synthesis
CFG_Synth

Verilog

EDIF

Timing Simulation Flow

Verilog
SIMPRIM
Library

Verify Place & Route
CFG_Routed

Verilog

SDF

BIT JEDEC

Bottom-Up Flow
Schematic Designs

Top-Down Flow
HDL Designs

Reports

Verilog

SYM

Board-Level Simulation

Build Physical

User Constraints File

Xilinx Implementation Tools

PIN

PKG

Place and Route

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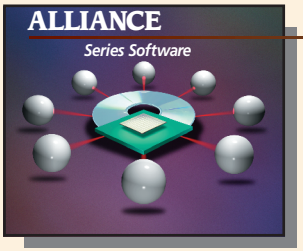

Cadence•Xilinx Design Guide

Device Architecture Support

FPGA Product Family
- Spartan
- Virtex
- XC4000X

CPLD Product Family
- XC9500

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com
United Kingdom
44 1932-820821
ukhelp@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com
Japan
81 3-3297-9163
jhotline@xilinx.com

Recommended Settings

UNIX

```
setenv CDS_INST_DIR <path for Cadence Software>

set path =
($CDS_INST_DIR/tools/bin \
$CDS_INST_DIR/tools/fet/bin \
$CDS_INST_DIR/tools/fet/concept/bin \
$CDS_INST_DIR/tools/verilog/bin \
$path)

setenv LM_LICENSE_FILE <path for Cadence LM_License File>

setenv LD_LIBRARY_PATH $CDS_INST_DIR/tools.sun4v/lib:$LD_LIBRARY_PATH

setenv VERILOGEXE $CDS_INST_DIR/tools.sun4v/verilog/bin/verilog
```

Guide Overview

1 Invoke the Design Manager

UNIX projmgr
PC Invoke Cadence Project Manager

2 Schematic Design Flow

- Use **Design Entry** to create schematic design.
- Generate Verilog Design output from **Design Entry**. Select Verify_Logic to launch Verilog-XL simulator and conduct Functional Simulation.
- Select **Place and Route** in the Cadence Project Manager. Set Bottom-up flow and click run to invoke Xilinx Design Manager.
- Select **Verify P&R** to launch Verilog-XL simulator and conduct post-routed timing simulation using Verilog and SDF files.
- Use **Build Physical** to generate Verilog and Symbols files for Board-Level simulation.

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