Sine/Cosine Look Up Table V1.0.2

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Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
E-mail: coregen@xilinx.com
URL: www.xilinx.com/ipcenter

Features

- Drop-in modules for the XC4000E, EX, XL, XV, Spartan, Spartan2, Virtex, and Virtex-E families
- Fully parameterizable sin/cos look-up table
- Input address widths from 3 to 10 bits
- Output data widths from 4 to 16 bits
- User can determine the accuracy of the result by selecting the desired output width
- Utilizes fast internal distributed ROM
- Easy to use: any table size and output resolution can be specified
- Efficient: calculates full 360 degree table from 90 degree segment
- Useful in high-speed modulation/demodulation applications
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- To be used with Xilinx Core Generator V2.1i System and later versions

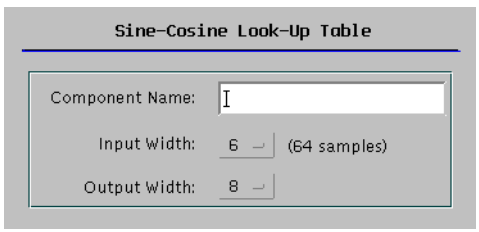

Figure 1: Sine-Cosine LUT Parameterization Window

Functional Description

The Sine/Cosine module returns the value **sin(theta)** when the control input (CTRL) is High and the value **cos(theta)** when the control input is Low.

The module contains an internal ROM look-up table that stores only the values for the first quarter of the sine wave. Values of sin(theta) or cos(theta) are derived from this stored data by appropriate negations of the input value and the value fetched from the internal table. The decisions to negate are based on the state of the two most significant bits of theta and the CTRL input.

Support for Signed and Unsigned Theta

The values generated by this module are always expressed in a signed, twos-complement fractional data format. However, values for theta may be provided in either magnitude-only unsigned or twos-complement signed data formats. The format used to express theta has an impact on the precise function performed by the module.

In the case where theta is expressed in an unsigned format, values for theta may range from 0 to 2^{input_width} -1. In the case where theta is expressed in a signed format, values for theta may range from $-2^{(input\_width-1)}$ to $2^{(input\_width-1)}$ -1. In either case, for the purpose of calculating the sine or cosine of theta, the input value is converted to radians as follows:

For signed theta:

$$\theta_{signed} = \frac{2\pi * theta}{2^{(input\_width - 1)}}$$

For unsigned theta:

$$\theta_{unsigned} = \frac{2\pi * theta}{2^{input\_width}}$$

Therefore, the precise function performed by this module, see Figure 2, is determined by the data format used to express the value of theta.

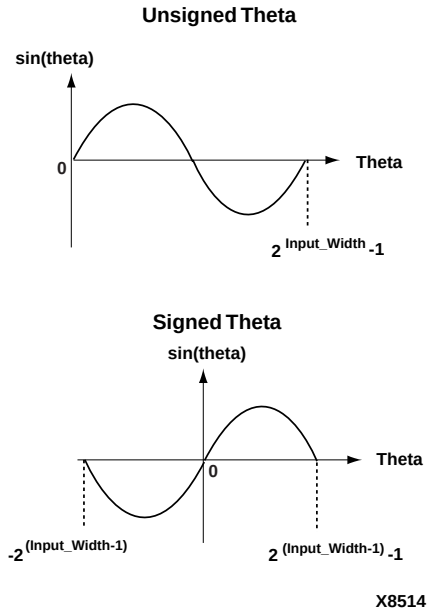

Figure 2: Relationship between Output Function and Input Data Format

Pinout

Port names for the schematic symbol are shown in Figure 3 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Theta [n:0]	Input	INPUT VALUE.
Ctrl	Input	CONTROL – when high, returns the sine of theta; when low, returns the cosine.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Output [m:0]	Output	OUTPUT VALUE – the sine or cosine of theta.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 1. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Input Width**: Select the width of the theta input bus. The valid range is 3 to 10. This value is also used to specify the depth of the required internal look-up table. The number of sample data points in the look-up table is $2^{Input\_Width-2}$ since only the values for the first quarter of the sine wave are stored.
- **Output Width**: Select the width of the look-up table from the pull-down menu. The valid range is 4 to 16. This value determines the precision of the output sin(theta) or cos(theta).

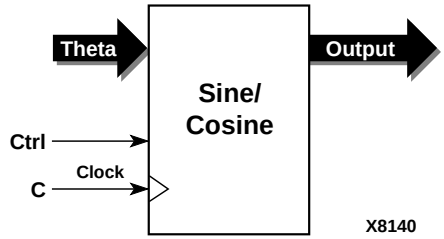

Figure 3: Core Schematic Symbol

Latency

The module has a pipeline latency that depends on the size of the input address width, see Table 2.

Table 2: Latency

Input Width	Latency (# Clocks)
3 to 4 bits	1
5 bits	2
6 to 10 bits	3

Core Resource Utilization

The number of CLBs/slices required for the look-up table depends on the size of the input address width and output data widths selected in the CORE Generator parameterization window.

Table 3 shows the equations to calculate the maximum number of CLBs/slices required for each available input address width. In these equations **m** is the output bit width. (When using these equations, round down to the nearest integer.)

For example, if the input address width is 10 (generating 1024 locations) and the output width is 8 bits, the look-up table requires 74 CLBs/slices.

Ordering Information

This core is downloadable free of charge from the Xilinx IP Center (www.xilinx.com/ipcenter), for use with the Xilinx Core Generator System version 2.1i and later. The Core Generator System 2.1iSystem is bundled with the Alliance 2.1i and Foundation 2.1i implementation tools.

To order Xilinx software contact your local Xilinx sales representative at www.xilinx.com/company/sales.htm.

Table 3: Bit Width versus CLB/Slice Count

Input Address Width	X4K CLB Count	Virtex Slice Count
3	(m+1)/2	(m+1)/2
4	m	m
5	m + (m+1)/2	2m
6	m + 4	3m/2+6
7	2m + 4	2m+6
8	2m + 5 + (m+1)/2	3m+8
9	4m + 6 + (m+1)/2	5m+4(m+1)/2
10	8m + 6 + (m+1)/2	8m+6(m+1)/2

Note:
m=output bit width

Parameter File Information

Component Name	Type	Notes
Component_Name	String	
Input_Width	Integer	3 -10
Output_Width	Integer	4 -16