CONV_ENC Convolutional Encoder

CSELT S.p.A

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Features

- Supports Spartan, Spartan™-II, Virtex™, and Virtex™-E devices
- Encoder for convolutional codes
- Customizable VHDL source code available, allowing generation of different netlist versions
- Customized testbench for pre- and post-synthesis verification supplied with the module
- Core customization:
  - Convolutional code definition parameters: Code rate; Code generation vectors; Code constraint length
  - Input data bus width
  - Output data period

Applications

- Encoding of convolutional codes

AllianceCORE™ Facts

Core Specifics[1]		
Supported Family	Spartan	Virtex
Device Tested	S10-3	V50-6
CLB Slices[2]	12	16
Clock IOBs	1	1
IOBs[3]	11	11
Performance (MHz)	67	144
Xilinx Tools	M1.5i/M2.1i	M1.5i/M2.1i
Special Features	None	None
Provided with Core		
Documentation		User Manual
Design File Formats		EDIF netlist, XNF netlist, VHDL source available extra
Constraints File		TOP_CONV_ENC_nl.ncf
Verification		VHDL testbench
Instantiation Templates		VHDL, Verilog
Reference Designs & Application Notes		None
Additional Items		None
Simulation Tool Used		
Synopsys VSS		
Support		
Design and customization support provided by CSELT		

Notes:
1. Data refer to the following customization:
   - Code parameters: rate = 1/2, constraint length = 5, generation vectors = $(23)_8$,$(33)_8$;
   - Input data bus width = 4;
   - Output data period = 2 clock cycles.
2. Utilization numbers for Virtex are in CLB slices
3. Assuming all core I/Os are routed off-chip

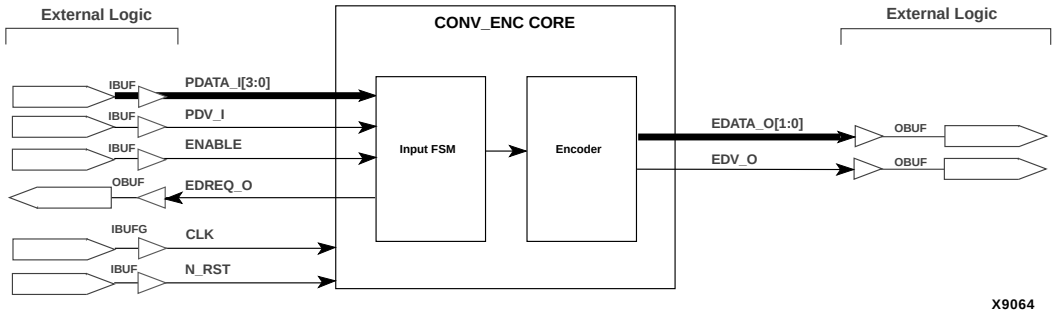

Figure 1: Convolutional Encoder Block Diagram

General Description

This core implements an encoder for convolutional codes. The core encodes a specific convolutional code, with user defined constraint length, rate and generation vectors. User customizable core features also include the input bus width and the encoder output period.

The Absolute Maximum ratings, Operating Conditions, DC Electrical Specifications and Capacitances depend on the Xilinx device selected for implementation and can be retrieved from the corresponding Xilinx datasheet.

Functional Description

The internal architecture of the Convolutional Encoder core is shown in Figure 1. A brief description of the operation of each module follows.

Input FSM

The input FSM handles the serialization of the incoming parallel data flow and the data request signal.

Encoder

The encoder performs convolutional encoding of the serialized data flow.

Pinout

The pinout of this core has not been fixed to a specific FPGA I/O allowing flexibility with a user's application. Signal names are shown in the block diagram in Figure 1 and described in Table 1.

Core Modifications

CSELT provides netlist customized to user's requirements. The Convolutional Encoder core source code is parametric. Parameters shown in Table 2 are implemented as a set of generics in the synthesizable VHDL source code of the core. Parameters allow the user to specify some architectural and functional features, so as to adapt the netlist to a specific design or application.

Verification Methods

Extensive functional (pre-synthesis) and timing (post-synthesis) simulation has been performed for different values of the core parameters, using the Synopsys VSS simulator. Simulation scenarios (including data and command files) and parametric test bench used for design verification are provided with the core.

Recommended Design Experience

Experience with the Xilinx design flow is recommended to the users of the netlist version of the core. For the source code version, users should also be familiar with the Synopsys FPGA synthesis tools (VHDL Compiler, FPGA Compiler) and simulator (VSS).

Ordering Information

The CONV_ENC core is provided under license by CSELT S.p.A. for use in Xilinx programmable logic devices. Please contact CSELT S.p.A. for information about pricing, terms and conditions of sale.

CSELT S.p.A. reserves the right to change any specification detailed in this document at any time without notice, and assumes no responsibility for any error in this document.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
PDATA_I[3:0]	Input	Parallel data input: Port size equal to DSIZE, where DSIZE is a generic
PDV_I	Input	Data valid input
ENABLE	Input	Encoder enable
EDREQ_O	Output	Encoder data request
EDATA_O[1:0]	Output	Encoded data output: Port size is equal to N, where N is a generic
EDV_O	Output	Data valid output
CLK	Input	Master clock
N_RST	Input	Asynchronous reset

Table 2: Core Parameters (VHDL Generics)

Parameter	Description
N	Inverse code rate
CONST_LENGTH	Code constraint length
POLGENx (x=0,1,2,3)	Code generation vectors
DSIZE	Input data size
OUTPUT_PERIOD	Output period

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Convolutional Encoder Implementation Request Form

To: CSELT S.p.A.

FAX: +39 011 228 7003

E-mail: viplibrary@cselt.it

CSELT configures and ships Xilinx netlist versions of the Convolutional Encoder core customized to your specification. Please fill out and fax this form so CSELT can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA.

From: _____

Company:_____

Address:_____

City,State,Zip:_____

Country:_____

Phone:_____

FAX:_____

E-mail:_____

Implementation Issues

1. Code rate:

2. Constraint length:

3. Coding polynomial:

4. Input data size:

5. Output period:

Business Issues

1. Indicate timescales of requirement:
_____ date for decision
_____ date for placing order
_____ date of delivery

2. Indicate your area of responsibility:
_____ decision maker
_____ budget holder
_____ recommender

3. Has a budget been allocated for the purchase?
Yes _____ No _____

4. What volume do you expect to ship of the product that will use this core? _____

5. What major factors will influence your decision?
_____ cost
_____ customization
_____ testing
_____ implementation size

6. Are you considering any other solutions?