HDLC Protocol Core

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Features

- Single and double byte address recognition
- 16 Bit (CRC-16) and 32 Bit (CRC-32) frame check sequence
- Asynchronous 8 bit input data interface, suitable for a wide range of FIFOs
- Compatible with ITU recommendation Q.921
- Serial interface with external clocking for interfacing to the PCM-highway
- Transmission is synchronous to network interface with back pressure mechanism. Buffering at the network interface not required.
- Supports transparent mode
- Supports modular scaling of multiple HDLC channels through parallel cores or core multiplexing
- Supports data rate up to 50 Mbits/s

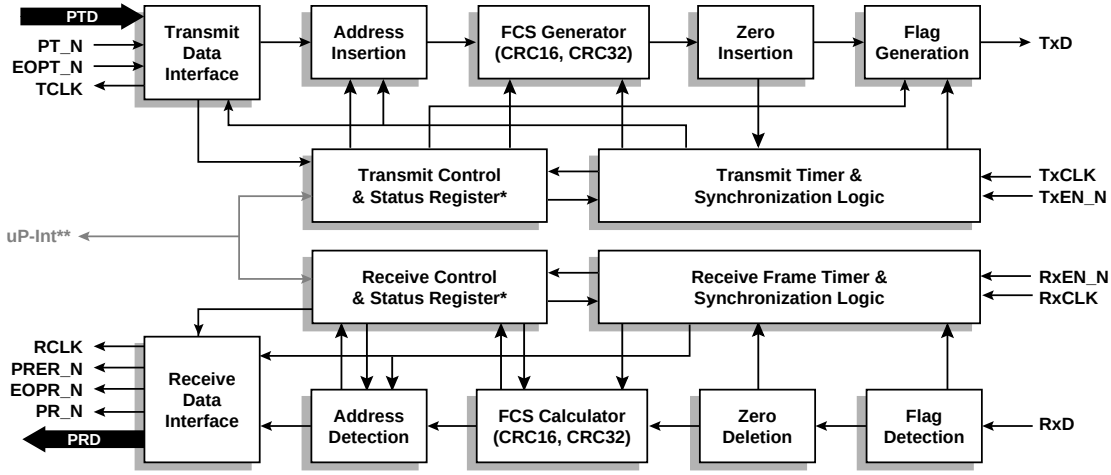
Applications

The ISS HDLC Protocol core is a high performance implementation suitable for a range of applications, including X.25, Frame Relay and ISDN B-channel and D-channel.

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000XL	
CLBs Used	Area optimized: 129[1] Speed optimized: 151[1]	
IOBs Used	27[2]	
CLKIOBs Used	2	
System Clock fmax	Area optimized: 20 MHz Speed optimized: 42 MHz	
Device Features Used	N/A	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4013XL-3 (area) XC4013XL-2 (speed)	167[1] 167[1]	447 425
Provided with Core		
Documentation	Core Documentation	
Design File Formats	.xnf or.ngd netlist VHDL source available extra	
Constraint Files	.cst	
Verification Tool	Test Vectors	
Schematic Symbols	VHDL, Verilog	
Evaluation Model	None	
Reference designs & application notes	None	
Additional Items	None	
Design Tool Requirements		
Xilinx Core Tools	Alliance 1.3	
Entry/Verification Tool	Synopsys VSS	
Support		
Support provided by ISS.		

Notes:
1. CLB counts are for the example implementation described in Table 1.
2. Assuming all core signals are routed off-chip.



*** Status Register Blocks are typically customized by ISS for each application.**
**** Microprocessor Interface does not come standard with core, but can be customized and added by ISS.**

Figure 1: HDLC Protocol Core Block Diagram

Table 1: Specification for Example Implementation

Parameter	Value
# of channels	1 duplex
Data Rate	Area optimized: 20 Mbps Speed optimized: 42 Mbps
Max frame size	Unlimited
FIFO Size	External
Protocols	HDLC
Additional	8-bit broadcast only address, not inserted16-bit FCS

General Description

The ISS HDLC Protocol Core is a high performance, third-level soft core module for bit-oriented packet transmission mode systems. It is suitable for Frame-Relay, X.25, ISDN B-Channel (64 KBit/s) and D-Channel (16 Kbit/s). The core fulfills the specification according to ITU Q.921, X.25 Level 2 recommendation.

The data stream and transmission rate is controlled from the network node (PCM highway clock) with a back pressure mechanism. This eliminates additional synchronization and buffering of the data at the network interface.

The data interface is 8 bit wide and asynchronous, and includes an 8 bit synchronization buffer. It provides basic adaptation for a wide range of FIFOs. The core can be used as a single channel HDLC protocol controller or switched parallel cores used to implement an N multiple channel controller. The high throughput and modular structure also enables multiplexing of the core between channels for low data rate applications.

Functional Description

The HDLC Protocol core is divided into blocks as shown in Figure 1. Operation of the core is described below.

Transmit Operation

The Transmit Data Interface provides a byte wide interface between the transmission buffer and the HDLC Protocol core. Transmit data is latched on the rising edge of TCLK when the packet transmit (PT) input is asserted. The last

byte of a packet is identified by the end of packet (EOPT) input control signal.

Subsequent blocks in the HDLC Protocol transmit controller insert the address, which may be either single or double byte, into the frame, calculate the Frame Check Sequence (FCS), which may be either a 16 or 32 bit CRC, perform zero insertion on the bit stream to ensure that the flag sequence does not occur in the data stream and add the start and end flags to the frame. The transmit bit stream is clocked out on the rising edges of TxCLK under the control of the enable signal TxEN.

The required configuration of the transmit controller may be defined using the control registers which are accessed via a microprocessor interface. The status register enables the transmit section operation to be monitored

Receive Operation

The HDLC Protocol core receiver accepts a bit stream on port RxD. The data is latched on the rising edges of RxCLK under the control of the enable input RxEN. The Flag Detection block searches the bit stream for the flag sequence in order to determine the frame boundaries. Any stuffed zeros are detected and removed and the FCS is calculated and checked. The core can be set-up, via the receiver control register, to either discard or pass errored frames. Address detection is performed and the relevant frames are made available to the system on the byte wide Received Data Interface.

Microprocessor Interface

The required microprocessor interface can be implemented as part of the provision of any HDLC core. It is not included in the standard core since it is likely to be different for every system in which the core is used.

Core Modifications

The information contained in this datasheet describes the basic HDLC Protocol core provided by ISS. Additional parts of the users system may be developed by ISS and integrated with this core to provide an application specific solution matched directly to the requirements. Typical additional features include microprocessor interface functions, buffers, multichannel capability and channel multiplexers. Contact ISS directly to discuss any specific requirements. See also the HDLC Protocol Core Implementation Request Form at the end of this data sheet.

Pinout

The pinout is not fixed to any specific device I/O. Signal names are provided in the block diagram shown in Figure 1, and described in Table 1. Unless otherwise stated all signals are active high and bit(0) is the least significant bit.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
Transmitter Interface		
PTD	Input	Packet Transmit Data (7: 0) - for data transfer between transmission buffer and HDLC Protocol core.
PT_N	Input	Packet Transmit - initiates packet transmission sequence by core. Falling edge of signal synchronizes transmission sequence as start of packet; must stay low for duration of packet, if not transmission sequence will be aborted with an abort flag pattern; active low.
EOPT_N	Input	End of Packet Transmit - indicates end of current transmitted packet; must be asserted during last byte period; active low.
TCLK	Output	Transmit Data Clock - byte clock with variable pulse width; loads (on rising edge) 8 bit transmission data into transmission shift register. Rising edge generated when last bit of previous data has been shifted. Shifting is not synchronous and can vary, depending on zero insertion.
TxD	Output	Transmission data - serial data out line, driven by tri-state buffer; may be directly connected to PCM high-way.
TxCLK	Input	Transmission Clock, - 16 kHz to 50 MHz (2.048, 4.096 MHz typical); uses 1 FPGA CLKIOB pin.
TxEN_N	Input	Transmission Enable - enables transmission data and tri-state driver. May be generated from channel multiplexer; active low.

Signal	Signal Direction	Description
Receiver Interface		
RCLK	Output	Receiver Data Clock - byte clock with variable pulse width; pushes, on rising edge, 8 bit received data out of receiver shift register. Rising edge generated when first bit of next byte is received.
PRER_N	Output	Packet Receive Error - indicates frame error. It is CRC results of received packet; active low.
EOPR_N	Output	End of Packet Received - indicates end of received packet, set during last received byte; active low.
PR_N	Output	Packet Received - indicates receipt of valid correct packet; stays low, until received packet is transferred; active low.
PRD	Output	Packet Receive Data (7:0) - provides data transfer between receiver of HDLC Protocol Core and receive buffer.
RxEN_N	Input	Receive Enable - enables masking of received data, may be generated by channel multiplexer; active low.
RxCLK	Input	Receiver Clock, - 16 kHz up to 50 MHz (2.048, 4.096 MHz typical)
RxD	Input	Receive Data - is serial data in, latched with rising edge of RxCLK if RxEN is low.

Verification Methods

The core has been verified in Xilinx devices using post layout simulation across a wide range of configurations by using input vector sequences compatible with many international standards.

Available Support Products

Also available from ISS is a bit parallel (byte stuffed) version of this core for PPP applications.

Ordering Information

For information on this or other products mentioned in this specification, contact Integrated Silicon Systems directly from the information provided on the front page.

Related Information

International Telecommunications Union

International Telecommunications Union
Place des Nations
CH-1211Geneve 20
Switzerland
Phone: +41 22 730 51 11
Fax: +41 22 733 72 56

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95214
Phone: 408-559-7778
Fax: 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: 800-231-3386 (inside the US)
408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE specific information, contact:

Phone: 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

HDLC Protocol Core Implementation Request Form

To: **Integrated Silicon Systems, Inc.**
FAX: **+44 1232 669664**
E-mail: **info@iss-dsp.com**

From: _____

Company: _____

Name: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

E-mail: _____

ISS configures and ships Xilinx netlist versions of the HDLC Protocol core customized to your specification. Please fill out and fax this form so ISS can respond with an appropriate quotation that includes performance and density metrics for the target Xilinx FPGA

1. Number of required channels: _____
   If more than one channel, storage is required for inactive channel state. Is this storage to be on-chip or off-chip?

2. Please indicate:
   ____ Serial data stream output with Zero-bit stuffed transparency
   ____ Byte parallel data output with Octet stuffed transparency?

3. Data rate (per channel): _____

4. Available clocks: _____

5. The bare core provides separate input, output and enable ports for each configurable register. If a specific host bus interface is required, please specify the interface below.

6. The bare core provides byte-wide data ports with ByteTaken and ByteAvailable signals for use with external data FIFOs. If on-chip FIFOs are required with the core, please indicate which and specify their required size. Appropriate control and error condition signals will then be available.

   - Tx FIFO Size: _____

   - Rx FIFO Size: _____

7. If there are any specific protocol requirements or deviations from the HDLC specification, please detail them below.

8. Indicate required HDLC frame address field size:
   ____ 8 bits fixed
   ____ 16 bits fixed
   ____ Programmable by control register bit

9. Indicate how address should be inserted into transmitted HDLC frames:
   ____ Always
   ____ Never
   ____ Programmable by control register bit

10. Indicate if a programmable address is to be matched against incoming frames:
    ____ Always
    ____ Never
    ____ Programmable by control register bit

11. Indicate if the broadcast (all ones) address is recognized:
    ____ Always
    ____ Never
    ____ Programmable by control register bit

12. Indicate if the broadcast address is recognized
    ____ Yes
    ____ No

13. Indicate if an all addresses mode (where all frames are accepted and passed to the host
    ____ Always (Note: this effectively disables all other forms of address recognition.)
    ____ Never
    ____ Programmable by control register bit

14. Indicate if incoming address is stripped out of the packet before the data is passed through to the host:
    ____ Always
    ____ Never
    ____ Programmable by control register bit

15. Indicate HDLC Frame Check Sequence (CRC) size:
    ____ 16 bits fixed
    ____ 32 bits fixed
    ____ Programmable by control register bit

16. The default FCS polynomials are as follows. If alternative polynomials are required, specify them in the space below.
    16 bit: $X^{16}+X1^{2}+X^{5}+1$
    32 bit: $X^{32}+X^{26}+X2^{3}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$

17. Specify any additional requirements: