XF-TWSI-MS Two-Wire Serial Interface Master-Slave

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AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Datasheet, Implementation instructions
Design File Formats	VHDL Source RTL
Constraints File	.ucf
Verification	VHDL Testbench
Instantiation Templates	VHDL, Verilog
Reference designs & Application notes	None
Additional Items	Warranty by MDS
Simulation Tool Used	
Model Technology	
Support	
Support provided by Memec Design Services.	

Features

- I²C-compatible two-wire serial interface core; *I²C is a trademark of Philips, Inc.*
- Multi-master operation with arbitration and clock synchronization
- Slave transmit and receive operation
- Support for reads, writes, burst reads, burst writes, and repeated start
- User-defined timing and clock frequency
- Fast mode and standard mode operation

Applications

- Embedded microprocessor boards and any circuit needing I²C peripherals.

Table 1: Core Implementation Data

Supported Family	Device Tested	CLBs[2]		Clock IOBs	IOBs[1]		Performance (MHz)	Xilinx Tools	Special Features
		Core	Core+ Ext logic		Core	Core+ Ext logic			
4000XL	4005XL-1	156	156	2	31	29	31	M1.5i	TBUFs
Spartan	S10-4	164	164	2	31	29	30	M1.5i	TBUFs
Virtex	V50-4	185[2]	185[2]	2	31	29	59	M1.5i	TBUFs

Notes:
1. Assuming all core I/O are routed off-chip.
2. Utilization numbers for Virtex are in CLB slices.

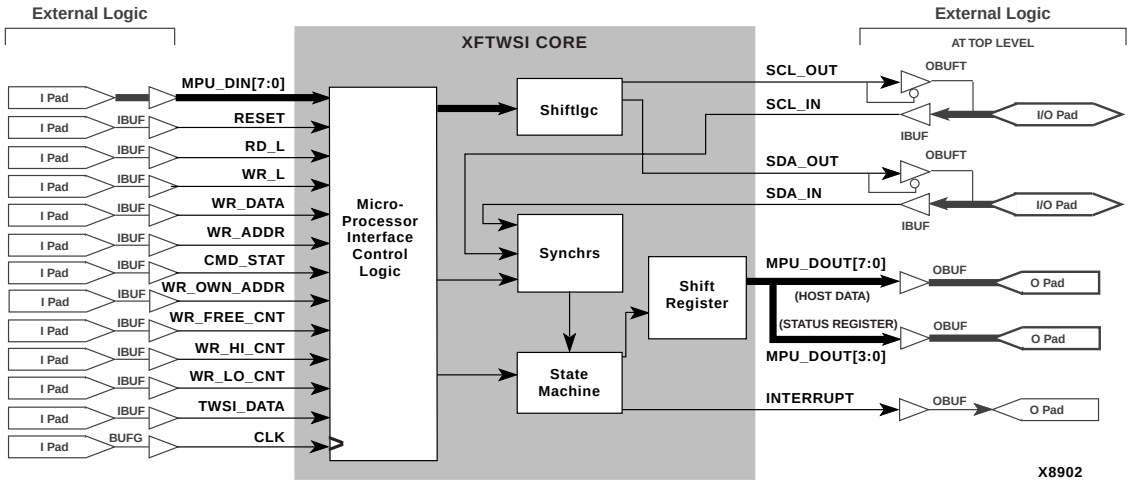

Figure 1: XF-TWSI Block Diagram

General Description

XF-TWSI-MS is an industry standard two-wire serial interface supporting multiple masters. This core will operate as a master or a slave. This core does not support General Call Addressing, 10-bit slave addressing, or START byte data transfers.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core inorder to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

The Absolute Maximum Ratings, Operating Conditions, DC Electrical Specifications, and Capacitance are device dependent and can be found in the Xilinx datasheet for the target device.

Functional Description

The XF-TWSI-MS is partitioned into modules as shown in Figure 1 and described below.

Microprocessor Interface Control Logic

There are four registers used to interface to the host: the Data Register, the Address Register, the Own_Address Register, and the Command Register. The Own_Address Register is used for slave operations to set the unique address of the device on the IIC bus. The strobes WR_DATA, WR_ADDR, WR_OWN_ADDR, and CMD_STAT are directly connected to the clock enable pins of these register flip-flops for ease of interface.

Shiftlgc

The basic cycle on the XF-TWSI-MS serial interface consists of an address cycle followed by a data cycle. The address consists of seven bits and the read/write bit (the LSB). The MSB is always transmitted first on the SDA line. The data cycle can either be a read or a write. For a write operation the macro shifts the data from the Data Register onto the SDA line. For a read operation the macro captures the data into the Shift Register. The data cycle can end in three different ways:

1. A stop can be generated which terminates the current cycle.
2. Another data cycle can take place (a burst).

3. A repeated start can be generated by the inter-face.

There is always one interrupt generated for each data cycle independent of the type of cycle. For example, for a burst read cycle an interrupt will be generated for each byte read. For a burst write cycle an interrupt will be generated when each byte transfer is completed.

A repeated start is used to turn the bus around; when a read cycle must be followed directly by a write cycle without a stop in-between. Since the READ bit is a part of the address, if a read followed by write is desired without a stop command, a second address must be issued following the data cycle. The sequence of events in a repeated start cycle is: start, address cycle, data cycle, repeated start, address cycle, data cycle, stop. Each of the data cycles can be repeated if bursting is desired, and the stop cycle could actually be another repeated start, if desired.

Synchrs

The SDA and SCL inputs are passed through this module that performs a dual-rank synchronization and glitch filtering when enabled by the FILTER_EN signal. The synchronized versions of the SDA and SCL signals are used in all macro modules.

The XF-TWSI-MS macro treats both the SDA and SCL lines as data lines. The SDA line is actually sampled some number of clocks after the rising edge of SCL is detected. This allows for greater noise immunity and more robust operation.

State Machine

The control for the serial interface comes from the state machine. This state machine controls the loading and enabling of all shift registers and counters, and is responsible for implementing the basic interface protocol.

Shift Register

There is a single parallel-in, parallel-out, serial-in, serial-out shift register called NUPSHIFT_MS, which performs the shifting of data for address cycles, write cycles, and read cycles. The parallel output drives the macro interface pins MPU_DOUT which are used to return read data to the host.

Core Modifications

With minor exception, the XF-TWSI-MS meets or exceeds the industry standard. However, in most cases the Timespecs can be tightened significantly. Proper operation with 100ns bus cycles has been verified. In all cases, a post-route timing analysis should be performed to verify performance. Implementation beyond specified performance and other customizing is available through Memec Design Services at additional cost.

External Crystal Support

This core does not support connection of a crystal directly to the device; a clock input is required.

Pinout

Due to the open collector nature of the Serial Data (SDA_IN and SDA_OUT) and Serial Clock (SCL_IN and SCL_OUT) pins, the XF-TWSI-MS must be implemented internally with the user's design using an OBUFT and IBUF combination. Signal names are provided in the block diagram shown in Figure 1 and Table 2.

Verification Methods

Complete functional and timing simulation has been performed on the XF-TWSI-MS using Model Technology VSIM. (Simulation command files and test bench used for verification are provided with the core.)

Recommended Design Experience

Users should be familiar with VHDL, Xilinx design flows and have experience with microprocessor systems and peripherals. For the source code version, users should also be familiar with Synplicity's synthesis and Model Technology's simulation tools.

Ordering Information

The XF-TWSI Two Wire Serial Interface Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec De-sign Services for the Design License Agreement with complete Terms and Conditions of Sale.

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Table 2: Core Signal Pinout

Signal	Signal Direction	Description
MPU_DIN[7:0]	Input	Microprocessor Data In lines; used to program Data, Address, and Command Registers.
RESET	Input	Reset; active high.
RD_L	Input	Allows reads on MPU_DOUT when active "0" with proper read buffer/ register is selected.
WR_L	Input	Rising edge of this signal registers data in internal registers when proper address is selected.
WR_DATA	Input	When active "1" with WR_L strobes 8-bits from MPU_DIN into Data Register for serial bus write cycle.
WR_ADDR	Input	When active "1" with WR_L strobes least significant 7-bits of MPU_DIN into Address Register for all Serial Bus Operations.
WR_OWN_ADDR	Input	When active "1" with WR_L strobes 8-bits from the MPU_DIN into OWN_ADDR register to set address of device on I2C bus.
CMD_STAT	Input	When active "1" with WR_L strobes least significant 5-bits from MPU_DIN into Command Register, initiates serial bus cycle and clears the Interrupt line. When active "1" with RD_L reads status register.
WR_FREE_CNT	Input	When active "1" with WR_L strobes 8-bits from MPU_DIN into BUSFREE_COUNT register, used to set the bus free period.
WR_HI_CNT	Input	When active "1" with WR_L strobes 8-bits from MPU_DIN into HI_COUNT register, used to set number of CLK clock periods for low period of SCL and setup time for repeated start operation.
WR_LO_CNT	Input	When active "1" with WR_L strobes 8-bits from the MPU_DIN into LO_COUNT register used to set number of CLK clock periods for high count of SCL, hold time for start command, and setup time for stop command.
TWSI_DATA	Input	Allows reads on MPU_DOUT when active "1" with RD_L.
CLK	Input	Primary clock.
SCL_OUT	Output	Serial clock with open collector output.
SCL_IN	Input	Serial clock with open collector input.
SDA_OUT	Output	Serial data with open collector output.
SDA_IN	Input	Serial data with open collector input.
MPU_DOUT[7:0]	Output	Returns read data after activation of Interrupt pin and error free status; lower three bits are also Status Register.
INTERRUPT	Output	Interrupt line set upon completion or abort of serial cycle; active high.

Related Information

The I2C-Bus And How To Use It

Contact:

Philips Semiconductors
URL: www-eu.semiconductors.philips.com/i2c/

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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