Virtex-E LVDS Drivers & Receivers: Interface Guidelines

XAPP232 (Version 1.0) October 4, 1999 Application Note: Jon Brunetti & Brian Von Herzen

Summary

This application note describes how to use the new Virtex-E™ LVDS (low-voltage differential signaling) drivers and receivers for high-performance LVDS interfaces to industry-standard LVDS devices. LVDS provides higher noise immunity than single-ended techniques, allowing for higher transmission speeds, smaller signal swings, lower power consumption, and less electro-magnetic interference than single-ended signaling. Differential data can be transmitted at these rates using inexpensive connectors and cables. Virtex-E LVDS drivers offer improved signal integrity over other LVDS drivers because they absorb reflected signals unlike other LVDS drivers.

Introduction

Virtex-E FPGAs offer new high-speed LVDS receivers and drivers as part of their standard I/O. This new capability enables high-speed differential signaling that previously was not possible in programmable logic devices. Low-voltage differential signaling (LVDS) has emerged as a leading standard for differential signaling between boards, chassis and other peripherals. For the first time, FPGAs can directly receive and drive these signals between boards, chassis and other peripherals.

Virtex-E LVDS drivers use standard terminators that are commercially available from Bourns, CTS, and other vendors in miniature 8-pin and 16-pin surface-mount packages. The Virtex-E LVDS driver actually improves the LVDS signal quality over other LVDS drivers because it absorbs any reflections coming back to the source.

The Virtex-E drivers and receivers provide several benefits:

- Direct board-to-board high-speed interface,
- Much higher signaling speeds than with single-ended interfaces,
- Better signal integrity due to source termination than with other LVDS drivers,
- Elimination of costly TTL-LVDS drivers and LVDS-TTL receivers,
- Reduced board area,
- Reduced signal delay/skew.

For a detailed discussion on the benefits of LVDS, including comprehensive system analyses, please see the National Semiconductor LVDS Owner's Manual and Design Guide, located at:

http://www.national.com/appinfo/lvds/lvdstotal.pdf

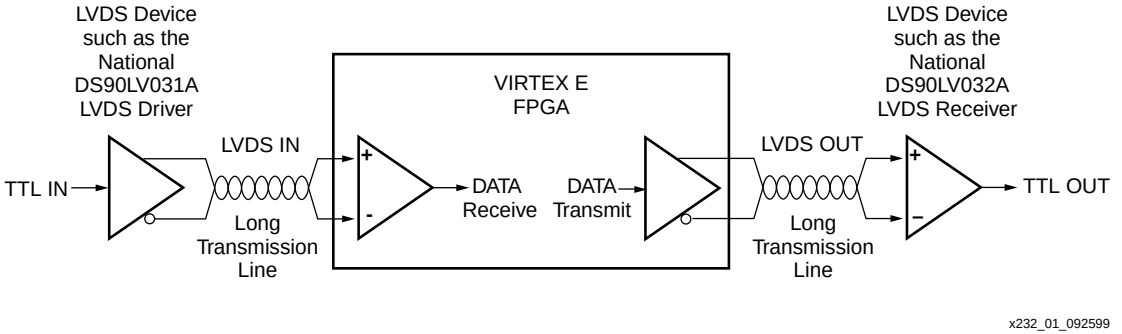

Figure 1: Virtex-E LVDS Interface for Long Distance I/O

Figure 1 shows how Virtex-E devices drive and receive LVDS signals. This example shows an LVDS source on the left, in this case a National Semiconductor DS90LV031A LVDS line driver. These signals pass directly onto the Virtex-E device without needing any translator chips. On the right, outputs from the Virtex-E FPGA drive an LVDS receiver, in this case a National Semiconductor DS90LV032A LVDS line receiver, without any translator chips. The National devices serve as an illustration. Any LVDS device works in this role, including other Virtex-E devices.

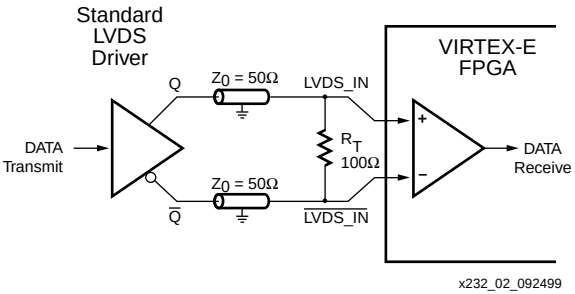

Figure 2: A Standard LVDS Driver Driving a Virtex-E LVDS Receiver

Receiving LVDS on Virtex-E Devices

Figure 2 shows the complete schematic of an LVDS driver driving the Virtex-E LVDS receiver. An LVDS driver on the left drives the two 50 Ω transmission lines into a Virtex-E LVDS receiver on the right. The two 50 Ω single-ended transmission lines can be microstrip, stripline, or a 100 Ω differential twisted pair or similar balanced differential transmission line. Figure 3 shows how to implement the 50 Ω lines using microstrip techniques on a PC board. Many combinations are possible, but these geometries allow for a compact 50 Ω line using standard 8-mil wide traces on the PC board. See application note XAPP230: The LVDS I/O Standard for a discussion of transmission lines and terminations used in LVDS. The 100 Ω termination resistor R_T terminates the LVDS_IN and $\overline{\text{LVDS\_IN}}$ nodes close to the Virtex-E device. A differential termination like the 100 Ω termination resistor dissipates much less power than two 50 Ω resistors to ground. The Virtex-E LVDS receiver, on the right in

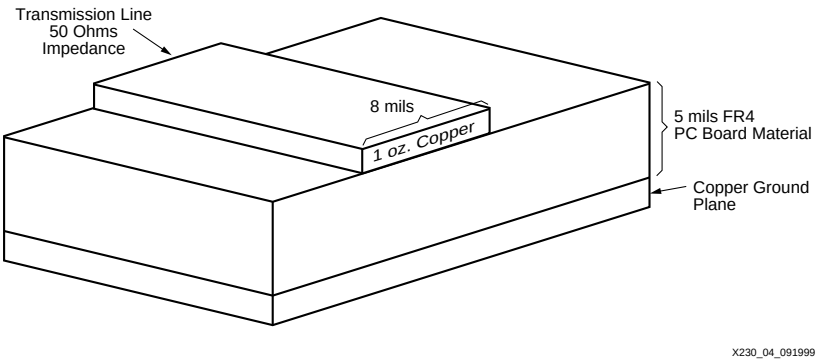

Figure 3: A 50 Ω Transmission Line Construction in Microstrip

Figure 2, adheres to all the standard LVDS DC input levels specified in XAPP230: The LVDS I/O Standard.

Figure 4 shows the typical pulse and 622 Mb/s burst data response for a standard LVDS driver driving the Virtex-E LVDS receiver in a 432-pin BGA package using short transmission lines (three inches on an FR4 PCB, or about 500 ps propagation delay). The voltages plotted are the voltages at the differential input on the FPGA. The package parasitics are included in these plots. LVDS can switch from low frequency to 622 Mb/s. The signal integrity remains good throughout the entire band as long as proper termination lines and termination resistors are used in the design. See XAPP233: Virtex-E LVDS at 622 Mb/s for a reference design describing the internal FPGA configuration for achieving 622 Mb/s signaling. The external design is exactly as described in Figure 5.

Figure 7 shows the typical pulse and burst data response for a standard LVDS driver driving the Virtex-E LVDS receiver in a 432-pin BGA package using long transmission lines (30 inches on an FR4 PCB, or about 5 ns propagation delay). Note that the reflections appearing on both the single-ended and differential signals every 10 ns, which is the round-trip delay of the transmission line interconnect. The reflections are caused by the capacitive load of the Virtex-E LVDS receiver, on the right in Figure 2. They bounce off the high-impedance source of the standard LVDS driver, on the left in Figure 2. These reflections add when transmitting data bursts or clocks, resulting in undershoot and signal swing reduction. This undershoot can be seen on the bottom two graphs in Figure 7. Signal swing reduction at high frequencies is common with the standard LVDS driver since it has a high output impedance, and does not absorb reflections from the capacitive load at the LVDS destination. The resulting 220 mV signal swing is sufficient for driving the Virtex-E LVDS receiver. Data and clocks can pass over longer cables as well, limited only by the quality of the cable. The cable quality is limited mainly by the cable attenuation due to skin effect losses at high frequencies.

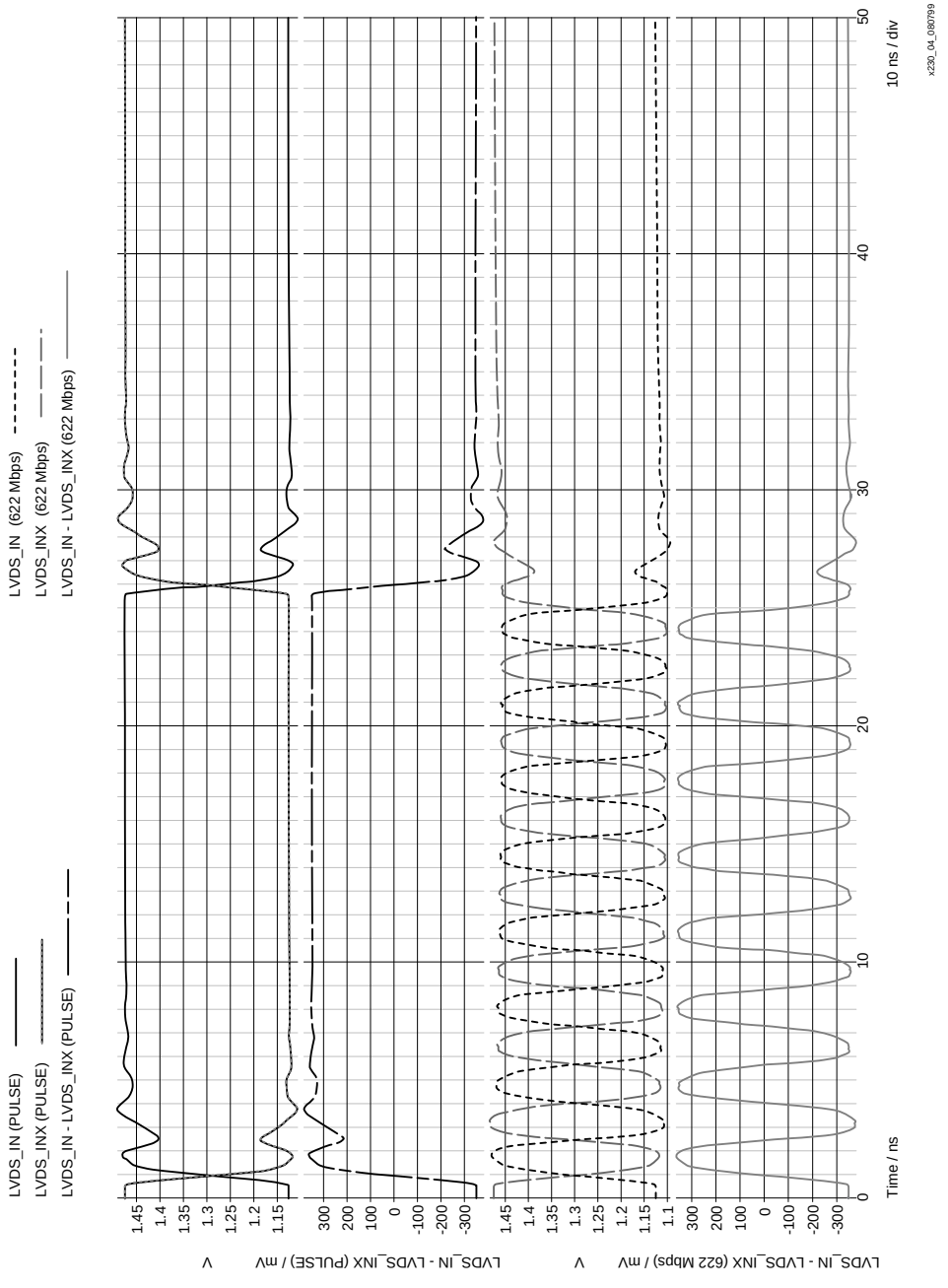

Figure 4: Short Line (500 ps) Pulse and High-Speed Data Response for Generic LVDS Input to the Virtex-E Circuit of Figure 2.

The 622 Mb/s data rate, or 311 MHz clock, is achievable in the -7 speed grade of the Virtex-E series. The Virtex-E 622 Mb/s receive data rate is not limited by the signal integrity of the interconnect or package parasitics and will run faster with higher speed grades of Virtex devices. See "XAPP233: LVDS at 622 Mb/s with Virtex-E FPGAs" for additional details.

Driving LVDS from Virtex-E Devices

Figure 5 shows the complete schematic of the Virtex-E LVDS line driver. It is capable of driving any LVDS receiver, including the National Semiconductor DS90LV032A LVDS line receiver in the 16-pin SOIC package or the Virtex-E LVDS line receiver in the 432-pin BGA package. Standard termination packs are available from Bourns and other vendors that provide termination networks with up to 16 pins per pack.

When driving a Virtex-E LVDS line receiver, connect the LVDS_OUT node in Figure 5 to a Virtex-E input (LVDS_IN) and the $\overline{\text{LVDS\_OUT}}$ node to the complementary Virtex-E input ($\overline{\text{LVDS\_IN}}$) of the true-differential input. Note the 100 Ω differential parallel termination resistor R_T across the LVDS_OUT and $\overline{\text{LVDS\_OUT}}$ outputs at the end of the transmission line. This is the standard LVDS termination. Resistors R_S and R_{DIV} attenuate the signals coming out of the Virtex-E LVDS drivers with V_{CCO} = 2.5V and provide a matched source impedance (series termination) to the transmission lines. The output common-mode voltage is approximately equal to $V_{CCO}/2$. Component value derivations for R_S and R_{DIV} are found in Appendix A on page 9. The Virtex-E LVDS driver meets or exceeds all of the LVDS specifications listed in XAPP230: The LVDS I/O Standard.

Although the Virtex-E LVDS line driver circuit in Figure 5 is different from a standard LVDS line driver, the voltages at LVDS_OUT and $\overline{\text{LVDS\_OUT}}$ are within the standard LVDS output levels shown in application note XAPP230, "The LVDS I/O Standard". A generic LVDS driver behaves approximately like a current source and has a high output impedance. The Virtex-E LVDS line driver behaves like a current source in parallel with a 50 Ω resistor, thereby providing a well-matched source impedance to differential signals. The 50 Ω source impedance of the Virtex-E LVDS driver absorbs nearly all differential reflections from the capacitive load at the LVDS destination, which reduces standing waves, undershoot, and signal swing reduction on data bursts or clocks.

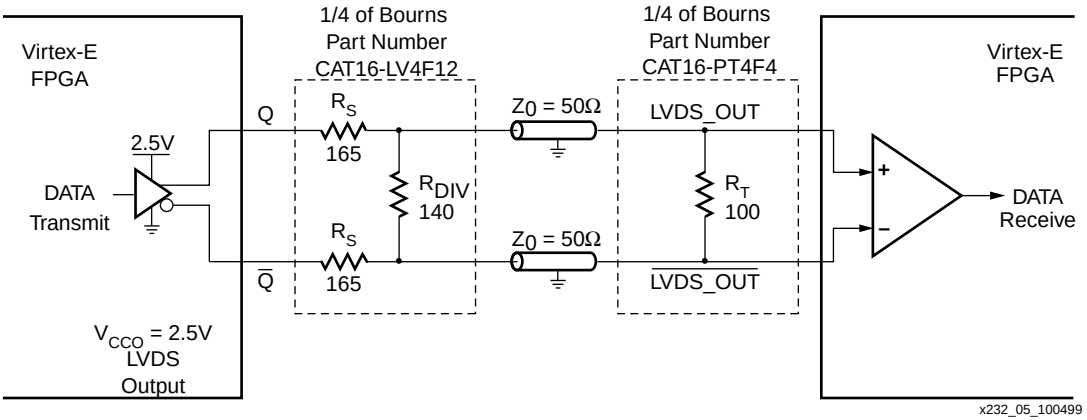

Figure 5: Virtex-E LVDS Line Driver and Receiver Schematic.

Figure 6 shows how 64 LVDS pins will fit neatly along one side of a BG432 package.The layout shows locations for eight termination packs, which are capable of terminating 32 LVDS channels. The ground plane is shown in gray and the microstrip and component pads in black. The 32 LVDS pairs are routed from the 432-pin BGA on the left through the termination packs in the center, and onto two 34-pin standard headers with 100 mil pin spacing. Notice the center pin pair of each header is connected to the ground plane. This center ground on each connector provides a current return path for any common-mode currents introduced by external system noise and layout/load mismatches.

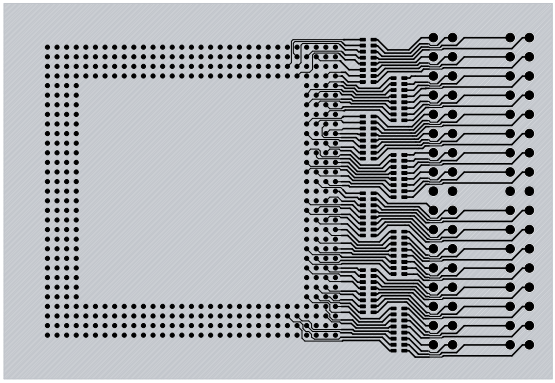

Figure 6: BG432 with 64 LVDS Pins and Eight Termination Packs.

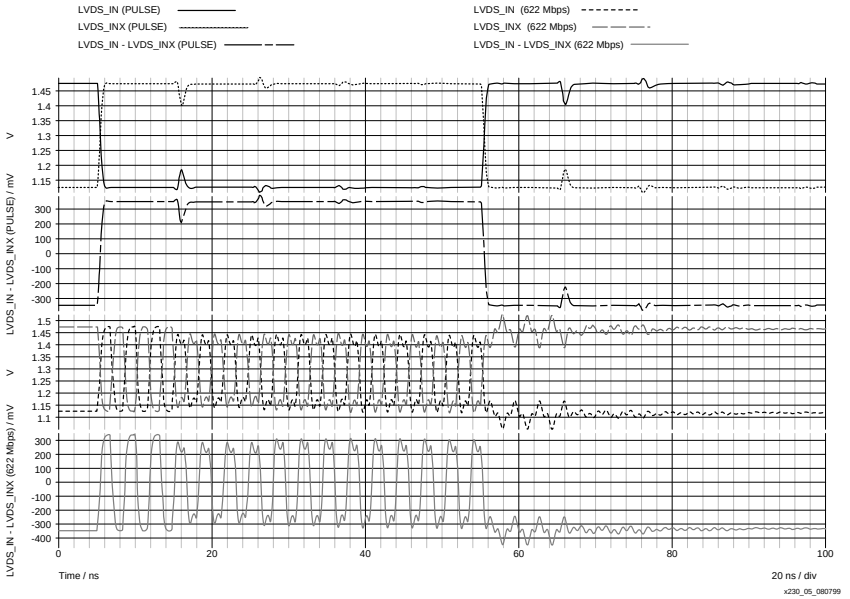

Figure 7: Generic LVDS Driver Performance with a 5 ns (30 inch) transmission line in the circuit shown in Figure 2

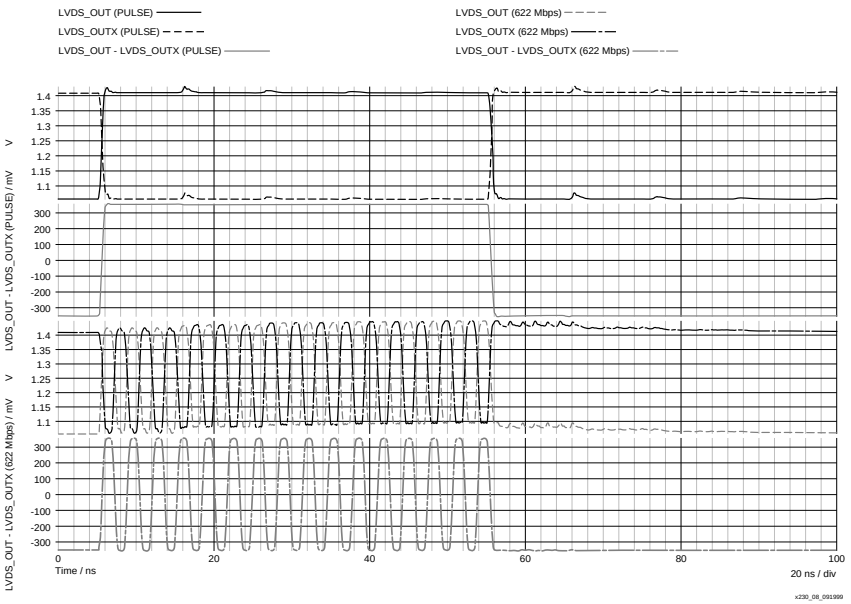

Figure 8: Virtex-E LVDS Driver Performance with a 5 ns (30 inch) transmission line in the circuit shown in Figure 5.

Figure 8 shows the pulse and burst data response of the Virtex-E LVDS line driver circuit in Figure 5 driving a Virtex-E LVDS receiver in the 432-pin BGA package with long (5 ns) transmission lines. Voltages are measured at the on-die differential input. Notice the differential reflections (LVDS_OUT - $\overline{\text{LVDS\_OUT}}$ on second waveform down) are negligible, confirming that the matched source impedance of the Virtex-E LVDS driver absorbs nearly all differential reflections. Comparing Figures 7 and 8, the Virtex driver absorbs spurious reflections much more than the regular LVDS driver.

The astute reader may notice that the Virtex-E LVDS driver of Figure 8 shows none of the undershoot or signal swing reduction evident with the generic LVDS driver of Figure 7.

Data and clocks can be transmitted over longer cables than 5 ns electrical length, limited only by the quality of the cable, namely the cable attenuation caused by skin effect losses at high frequencies. Signal swing is the same or better than the long line (5 ns) example of Figure 7. The excellent signal integrity of the Virtex-E LVDS driver makes it ideal for reliable data transfer at high rates over long distances. For the best LVDS signal quality, use a Virtex-E LVDS driver instead of standard off-the-shelf LVDS drivers.

How to specify LVDS on Virtex-E devices

For LVDS inputs on Virtex-E FPGAs, it is simply necessary to select an LVDS differential pair of pins that drive a single differential receiver. In the pinout tables, these differential pairs are designated with an IO_LXX[N,P]_[<>,Y,YY] type of designation. For example, a BG432 package has the following designation:

B13	PAD61	1	IO_L20N_YY	1
D14	PAD62	1	IO_L20P_YY	1

The IO_L20 indicates that these two pins drive differential receiver L20. The "N" stands for negative polarity, and the "P" stands for the positive polarity input. The YY suffix indicates that these LVDS pairs are available on all sizes of Virtex-E devices that support this package. For more information see XAPP235: Virtex-E Package Compatibility Guide.

For LVDS outputs, LVDS pairs can drive complementary outputs directly from the two LVDS pins using the LVDS drivers available in the Xilinx implementation software.

For PCB layout guidelines, see XAPP230: The LVDS I/O Standard. Resistors R_S and R_{DIV} should lie close to the Virtex-E outputs for the Virtex-E LVDS line driver. The parallel termination resistor R_T needs to be close to the LVDS inputs at the destination. The differential LVDS output should use a pair of adjacent Virtex-E pins, preferably in the same output block of the Virtex-E FPGA (see EPIC plots for block clustering). The LVDS data must have a single clock driving both of the output IOB's to minimize output skew between the two pins.

For additional information on transmission lines in LVDS, see the National Semiconductor LVDS Design Guide, available at
http://www.national.com/appinfo/lvds/lvdstotal.pdf.

Conclusion

The Virtex-E series of devices can transmit and receive LVDS at high speed. Virtex-E LVDS drivers provide significant improvement in signal integrity over standard off-the-shelf LVDS drivers due to their matched output impedance acting to source terminate the transmission lines. Reliable data transmission is possible over electrical lengths exceeding 5 ns (30 inches), limited only by cable attenuation due to skin effect. Virtex-E devices utilizing LVDS eliminate costly TTL-LVDS drivers and LVDS-TTL receivers, reduce board area, and reduce signal delay skew, while reliably transferring high-speed data and clocks over long distances between boards, chassis, and peripherals.

Appendix A:

Component value derivations for the Virtex-E LVDS line driver

Referring to Figure 5, resistors R_S and R_{DIV} attenuate the signals coming out of the Virtex-E LVDS drivers and provide a matched source impedance (series termination) to the transmission lines. Values for R_S and R_{DIV} are determined by these two constraints. The equivalent source impedance R_{EQ}, including the Virtex-E driver impedance R_{DRIVER}, must equal the transmission line impedance, typically 50 Ω. Using the differential half-circuit:

(R_{DIV} -> $R_{DIV}/2$, R_T -> $R_T/2$),

$$R_{EQ} = (R_{DRIVER} + R_S) \,//\, (R_{DIV}/2) = Z_0 \quad (1)$$

R_S and R_{DIV} are chosen to obtain the desired attenuation of the signal path from the Virtex-E driver to the LVDS destination. The desired signal attenuation is defined as α,

$$\alpha = V_{swing}(LVDS) / V_{CCO} = [(R_{DIV}/2) /((R_{DIV}/2) + R_{DRIVER} + R_S)]\,[R_T/2 / (R_T/2 + R_{EQ})]$$

$R_T/2 / (R_T/2 + R_{EQ}) = 1/2$, therefore,

$$\alpha = V_{swing}(LVDS) / V_{CCO} = [\,(R_{DIV}/2) /((R_{DIV}/2) + R_{DRIVER} + R_S)\,]\,/\,2 \quad (2)$$

Using Eqs. 1 and 2 and solving for R_{DIV} and R_S yields

$$R_S = (Z_0 / 2\alpha) - R_{DRIVER} \quad (3)$$

$$R_{DIV} = [\,4\alpha/\,(1 - 2\alpha)]\,[R_{DRIVER} + R_S\,] \quad (4)$$

Substituting Z_0 = 50 Ω, R_{DRIVER} = 12 Ω, V_{CCO} = 2.5 V, and V_{swing}(LVDS) = 350 mV into equations 2 through 4, the values of R_S = 167 Ω and R_{DIV} = 139 Ω are obtained. The values shown in Figure 5 are obtained by rounding to standard 1% values of R_S = 165 Ω and R_{DIV} = 140 Ω.

Revision

Date	Revision	Activity
10/04/99	1.0	Initial Release