# WebFITTER–
# Now *Better* Than *Ever*

**Here are the new features and capabilities for WebFITTER, our Internet-enabled XC9500 fitting and device evaluation tool.**

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Even if you have tried the industry's first on-line CPLD design and evaluation system, it's time to take another look. With the first version of the WebFITTER™ we gave you an easy to use graphical interface (Figure 1) that made it quick and simple to use. We provided you with all the necessary reports to see how Xilinx CPLDs could perform in your design, and all of the essential files (HDL simulation models and JEDEC programming files) to fully verify our solution.

In our latest release, Xilinx has once again raised the bar by providing you with the very best in on-line EDA solutions. By combining ABEL v7.1 (the newly updated version of the popular PLD design language), with our new Xilinx Synthesis Technology (VHDL and Verilog synthesis that augments Synopsys FPGA Express V3.2), Xilinx now offers the best suite of HDL design tools available. This combination of Synopsys synthesis, Xilinx synthesis, and ABEL, allows you to realize the full performance and cost effectiveness of the XC9500 family of ISP CPLDs.

## WebFITTER Design Input Interface

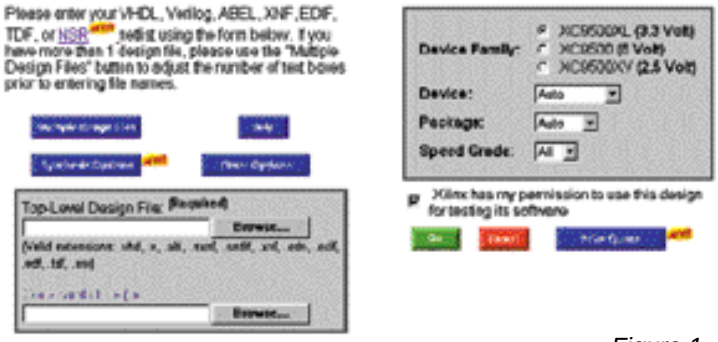


*Figure 1*

## Design Statistics and Price Quote Option

*Figure 2*

In addition to making it easier to implement your design, we have also made your overall device selection much faster through on-line device price quotes. Whether you need to know the price for a specific device/package/speed grade combination or the price for all devices in a specific package, it is just one click away (Figure 2).Σ

Check out the latest version of the WebFITTER at: www.xilinx.com/sxpresso/webfitter.htm.