# 32-Channel (Duplex) ADPCM Transcoder for Virtex FPGAs

**Digital signal processing without the complicated DSP chip—that's the power of Xilinx DSP solutions in Virtex FPGAs.**

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Thanks to the advent of high-density programmable logic device technology, you can now do high-performance ADPCM in off-the-shelf silicon without all the problems associated with a programmable digital signal processor. Xilinx AllianceCORE partner, Integrated Silicon Systems (ISS), offers reusable cores for ITU-compliant ADPCM Transcoders.

## Up to 32 Duplex ADPCM Channels

Xilinx recently released an ISS-designed 8-channel (duplex) ADPCM AllianceCORE for the Virtex family. This solution supports ITU G.721, G. 723, G.726, G.726a, G.727a, or G.727, and has been tested and verified to be fully compliant using the ITU specified test vectors. This same IP core was originally targeted at the XC4000 family, an FPGA architecture with distributed RAM features. However, thanks to the enhanced Block RAM features of the new Virtex FPGA architecture, ISS can realize a complete 32-channel (duplex) ADPCM Transcoder on a single V150BG352-4 Virtex device.

ISS achieved this unusually compact FPGA implementation by mapping all the multiplication calls in the transcoder algorithm into a single multiplier. What's more, ISS can also deliver fully customized variants. For example, the PCM input channel multiplexing and serial-to-parallel conversion circuitry may be added as required to suit your Virtex-based target system.

## Online Configuration

The 8-channel (duplex) version ADPCM AllianceCORE for Virtex is "on-line configurable" in terms of compression rate and PCM companding algorithm: A-law (for Europe), µ-law (for USA). This means that each channel can be individually programmed.

ISS ADPCM AllianceCORE deliverables include netlists, test-bench files, and command scripts, together with technical documentation, on-line, and hot-line technical support for one year. You can get the Xilinx AllianceCORE datasheet (.pdf) for the ISS ADPCM core at: www.iss-dsp.com/adpcm.

## Conclusion

The Virtex architecture is capable of hosting a 32-channel (duplex) ADPCM Transcoder that is on-line configurable for compression rate, µ/A-law, and number of channels. This demonstrates the attractiveness of the Virtex family as a viable platform for high-performance DSP applications using high-quality IP cores. Σ

### Adaptive Differential Pulse Code Modulation

**ADPCM (Adaptive Differential Pulse Code Modulation) is a dynamically adaptive form of Differential PCM. DPCM is a more bandwidth-efficient than PCM because voice data is represented more succinctly as the difference between the present signal value and the previous. ADPCM cuts the bandwidth of straight PCM by around 50 percent through a process called companding.**