New *FPGA* Compiler II– For Million-Gate Designs

Achieve dramatic increases in productivity and perfor mance for your million-gate Xilinx Virtex FPGA designs.

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You now have a revolutionary new synthesis solution crafted to meet your advanced design needs. The Synopsys FPGA Compiler II v3.2 implements ASIC-compatible design flows and methodologies for million-gate FPGAs, while also effortlessly delivering "push-button" synthesis with unprecedented quality of results.

FPGA Compiler II Defined

Since it was introduced, FPGA Express has been extremely well received in the market place for its easy-to-use GUI and its highly efficient synthesis technology. Synopsys now introduces a second distinct FPGA synthesis product: FPGA Compiler II. FPGA Compiler II builds on the success of FPGA Express by encompassing all of the features and functionality of the FPGA Express tool. It also adds many new breakthrough features that allow you to implement a million-gate design within your tight schedule and high performance design requirements.

You can use FPGA Compiler II as a standalone tool in a traditional FPGA design flow or, if you are an existing ASIC designer or plan on implementing an ASIC style flow for additional performance reasons, FPGA Compiler II is designed to plug into your existing or enhanced flow.

Key features supported by FPGA Compiler II v3.2:

- Reads and writes Design Compiler shell scripts.
- Outputs Synopsys .db database files.
- Support for DesignWare Foundation IP library.
- VISTA gate-level and RTL-level schematic viewer.
- Available on Solaris and HPUX as well as Windows 95/98/NT.

Design Flow

The FPGA Compiler II flow (Figures 1 and 2) offers you many key advantages when migrating an ASIC design to an FPGA or when performing ASIC prototyping within a standard ASIC flow.

First is the capability to utilize your industry standard Design Compiler ASIC synthesis shell

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FPGA Compiler II Input Flow

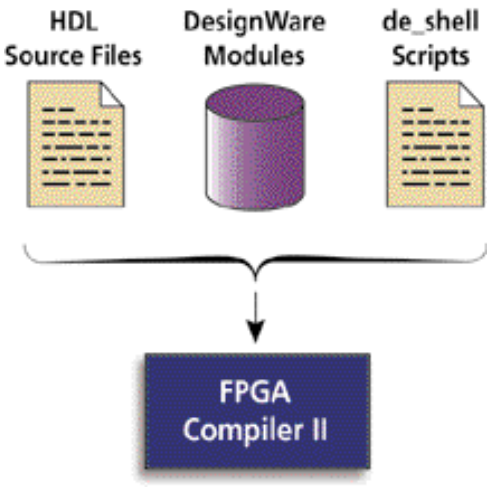

Figure 1

scripts with your FPGA synthesis tool. FPGA Compiler II is unique in that along with its intuitively simple GUI (Figure 3) you can also run a translated Design Compiler shell script in an interactive command shell (Figure 4) or as a transparent batch job.

Second is the capability to output the Synopsys .db database format that is supported by Design Compiler, PrimeTime (Static Timing Analysis), and many other Synopsys tools. ASIC designers have found that using static timing analysis allows for much faster design verification for million-gate designs.

Third, you can now make use of the DesignWare Foundation library. DesignWare Foundation is an off-the-shelf IP library provided by Synopsys that has been available to Design Compiler customers for many years, and now is available to you with FPGA Compiler II to efficiently and predictably implement your Xilinx solutions.

Summary

With the introduction of million-gate FPGAs, the need for you to have ASIC-compatible shell scripting, DesignWare IP libraries, and a proven synthesis product that leverages your existing investment and knowledge, is quickly becoming a reality. In today's market, if you are going to complete your design on schedule and on specification, then now is the time to implement these flows and methodologies. The Virtex Family and FPGA Compiler II v3.2 will make your success a reality.

FPGA Complier II Output Flow

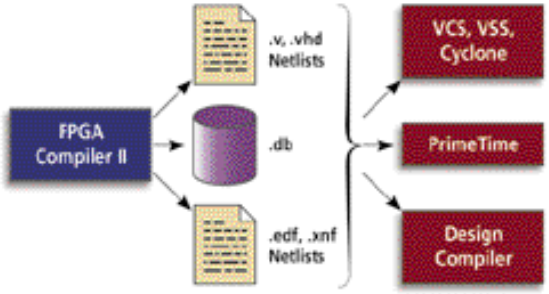

Figure 2

For more information on Synopsys FPGA Compiler II go to: www.synopsys.com/fpga

FPGA Compiler II GUI

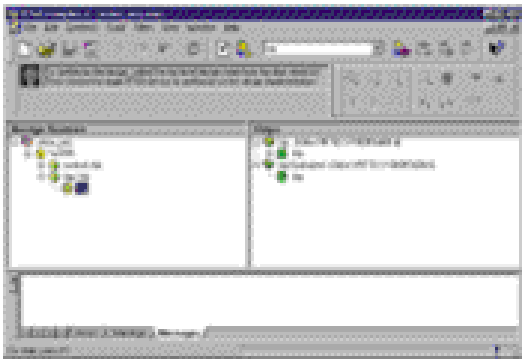

Figure 3

FPGA Compiler II Interractive Command Shell

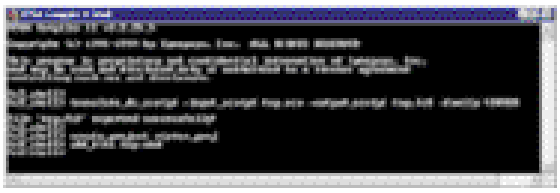

Figure 4