Using SelectI/O Interfaces in Spartan-II FPGAs

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Application Note

Summary

The Spartan™-II FPGA family simplifies high-performance design by offering SelectI/O™ inputs and outputs. The Spartan-II devices can support 16 different I/O standards with different specifications for current, voltage, I/O buffering, and termination techniques. As a result, the Spartan-II FPGA can be used to integrate discrete translators and directly drive the most advanced backplanes, busses, and memories. This application note describes how to take full advantage of the flexibility of the SelectI/O features and the design considerations to improve and simplify system level design.

Introduction

As FPGAs are used in more advanced applications, they must support an increased variety of I/O standards. Directly providing the necessary interface standard not only eliminates the cost of external translators, but also significantly improves the critical chip-to-chip speed and reduces power consumption. The revolutionary SelectI/O input/output standards of Spartan-II devices have met this need by providing a highly configurable, high-performance alternative to the I/O resources of conventional programmable devices. SelectI/O resources are most useful in applications with high-speed memory or programmable backplane interfaces running at over 100 MHz.

This application note covers the following topics:

- Overview of I/O Standards
- Choosing SelectI/O Options
- Board Design Considerations

SelectI/O Overview

Each SelectI/O block can support up to 16 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Spartan-II SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

I/O Standards Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards.

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. An input buffer can be configured as either a simple buffer or as a differential amplifier input. An output buffer can be configured as either a Push-Pull output or as an Open Drain output.

Overview of Supported I/O Standards

Table 1 provides a brief overview of the I/O standards supported by the Spartan-II FPGAs, including the sponsors and common uses for the standard. Detailed information on each specification may be found on the Electronic Industry Association (EIA) JEDEC website at www.jedec.org. The standard numbers are indicated where appropriate.

Table 1: SelectI/O Standards

Standard	Description	Spec	Use/Sponsor	Input Buffer	Output Buffer	5V Tolerant
LVTTL	Low-voltage TTL	JESD8B	General purpose	LVTTL	Push-Pull	Yes
LVCMOS2	Low-voltage CMOS for 2.5V	JESD8B	General purpose 2.5V	CMOS	Push-Pull	Yes
PCI	Peripheral Component Interconnect	PCI SIG	PCI bus	LVTTL	Push-Pull	33 MHz, 5V option
GTL	Gunning Transceiver Logic	JESD8-3	High speed bus, backplane; Xerox	Differential Amplifier	Open Drain	No
GTL+	GTL Plus		Intel Pentium Pro			
HSTL	High-speed Transceiver Logic	JESD8-6	Hitachi SRAM; IBM; three of four classes supported	Differential Amplifier	Push-Pull	No
SSTL3	Stub Series Terminated Logic for 3.3V	JESD8-8	SRAM/ SDRAM bus; Hitachi and IBM; two classes	Differential Amplifier	Push-Pull	No
SSTL2	SSTL for 2.5V	JESD8-9				
CTT	Center Tap Terminated	JESD8-4	Memory bus; Fujitsu	Differential Amplifier	Push-Pull	No
APG-2X	Advanced Graphics Port	AGP Forum	Intel Pentium II, SRAM	Differential Amplifier	Push-Pull	No

As shown in Table 2, each buffer type can support a variety of current and voltage requirements. While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. See www.jedec.org for more details.

Table 2: SelectI/O Supported Standards (Typical Values)

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	0.75
HSTL Class IV	0.9	1.5	0.75
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

Registered I/O

The Spartan-II IOB includes an optional flip-flop or latch on the input path, output path, and 3-state control input. Note, however, that there are no special library components for the I/O registers. To simplify design, especially synthesis, the standard register primitives are automatically absorbed into the IOB when possible. This feature is selected by the user by turning on the Map Option "Pack I/O Registers/Latches into IOBs", which can be set to "Off" (default), "Inputs Only", "Outputs Only", or "Inputs and Outputs". Alternatively, the IOB=TRUE property can be placed on a register to force the mapper to place the register in an IOB.

An optional delay element is associated with the input path in each logic input primitive (IBUF or IOBUF). When the buffer drives an input register within the IOB, the delay element activates by default to ensure a zero hold time requirement. The user can override this default with the NODELAY=TRUE property. The delay element is not used for non-registered inputs, to provide higher performance. If extra delay is desired, use the DELAY=TRUE property.

LVTTL Slew Rate and Drive Strength

The default LVTTL interface standard provides two unique output options, slew rate and drive strength. By default, the slew rate is reduced ("Slow") to minimize power bus transients when switching non-critical signals. This option is indicated as an S following the buffer name. Use the "Fast" slew rate for speed-critical outputs, indicated by an F following the buffer name. The

slew rate can be alternatively specified with the SLEW= property, which can be set to "SLOW" or "FAST".

The drive strength is selected in a similar fashion, with the default being 12 mA. Select a buffer with the appropriate suffix for the desired drive strength, choosing from 2, 4, 6, 8, 12, 16, or 24. The drive strength can be alternatively specified with the DRIVE= property, which can be set to any of the same seven values.

Table 3: SelectI/O Library Symbol

			IBUF	IBUFG	OBUF	OBUFT	IOBUF
LVTTL	**Slew**	**Drive**					
	Slow	**2 mA**	IBUF	IBUFG	OBUF_S_2	OBUFT_S_2	IOBUF_S_2
		4 mA			OBUF_S_4	OBUFT_S_4	IOBUF_S_4
		6 mA			OBUF_S_6	OBUFT_S_6	IOBUF_S_6
		8 mA			OBUF_S_8	OBUFT_S_8	IOBUF_S_8
		12 mA			OBUF_S_12	OBUFT_S_12	IOBUF_S_12
					OBUF	OBUFT	IOBUF
		16 mA			OBUF_S_16	OBUFT_S_16	IOBUF_S_16
		24 mA			OBUF_S_24	OBUFT_S_24	IOBUF_S_24
	Fast	**2 mA**			OBUF_F_2	OBUFT_F_2	IOBUF_F_2
		4 mA			OBUF_F_4	OBUFT_F_4	IOBUF_F_4
		6 mA			OBUF_F_6	OBUFT_F_6	IOBUF_F_6
		8 mA			OBUF_F_8	OBUFT_F_8	IOBUF_F_8
		12 mA			OBUF_F_12	OBUFT_F_12	IOBUF_F_12
		16 mA			OBUF_F_16	OBUFT_F_16	IOBUF_F_16
		24 mA			OBUF_SF_24	OBUFT_F_24	IOBUF_F_24
LVCMOS2			IBUF_LVCMOS2	IBUFG_LVCMOS2	OBUF_LVCMOS2	OBUFT_LVCMOS2	IOBUF_LVCMOS2
PCI	**Speed**	**Voltage**					
	33 MHz	3V	IBUF_PCI33_3	IBUFG_PCI33_3	OBUF_PCI33_3	OBUFT_PCI33_3	IOBUF_PCI33_3
		5V	IBUF_PCI33_5	IBUFG_PCI33_5	OBUF_PCI33_5	OBUFT_PCI33_5	IOBUF_PCI33_5
	66 MHz	3V	IBUF_PCI66_3	IBUFG_PCI66_3	OBUF_PCI66_3	OBUFT_PCI66_3	IOBUF_PCI66_3
GTL			IBUF_GTL	IBUFG_GTL	OBUF_GTL	OBUFT_GTL	IOBUF_GTL
GTL+			IBUF_GTLP	IBUFG_GTLP	OBUF_GTLP	OBUFT_GTLP	IOBUF_GTLP
HSTL	**Class**						
	I		IBUF_HSTL_I	IBUFG_HSTL_I	OBUF_HSTL_I	OBUFT_HSTL_I	IOBUF_HSTL_I
	III		IBUF_HSTL_III	IBUFG_HSTL_III	OBUF_HSTL_III	OBUFT_HSTL_III	IOBUF_HSTL_III
	IV		IBUF_HSTL_IV	IBUFG_HSTL_IV	OBUF_HSTL_IV	OBUFT_HSTL_IV	IOBUF_HSTL_IV
SSTL	**Voltage**	**Class**					
	3V	**I**	IBUF_SSTL3_I	IBUFG_SSTL3_I	OBUF_SSTL3_I	OBUFT_SSTL3_I	IOBUF_SSTL3_I
		II	IBUF_SSTL3_II	IBUFG_SSTL3_II	OBUF_SSTL3_II	OBUFT_SSTL3_II	IOBUF_SSTL3_II
	2.5V	**I**	IBUF_SSTL2_I	IBUFG_SSTL2_I	OBUF_SSTL2_I	OBUFT_SSTL2_I	IOBUF_SSTL2_I
		II	IBUF_SSTL2_II	IBUFG_SSTL2_II	OBUF_SSTL2_II	OBUFT_SSTL2_II	IOBUF_SSTL2_II
CTT			IBUF_CTT	IBUFG_CTT	OBUF_CTT	OBUFT_CTT	IOBUF_CTT
AGP			IBUF_AGP	IBUFG_AGP	OBUF_AGP	OBUFT_AGP	IOBUF_AGP

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic Spartan-II IBUF symbol appears in Figure 1. The extension to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

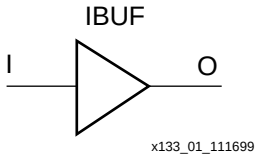

Figure 1: Input Buffer (IBUF) Symbol

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG symbol can only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic Spartan-II IBUFG symbol appears in Figure 2.

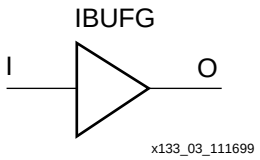

Figure 2: Global Clock Input Buffer (IBUFG) Symbol

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Spartan-II BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 3.

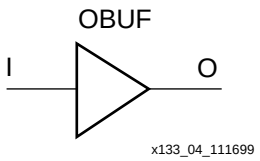

Figure 3: Output Buffer (OBUF) Symbol

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 4, typically implements 3-state outputs or bidirectional I/O. Unused I/O are configured with OBUFT_S_12, which is disabled with a weak pulldown.

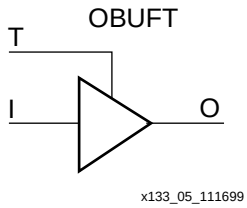

Figure 4: 3-State Output Buffer (OBUFT) Symbol

3-state output buffers and bi-directional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 5.

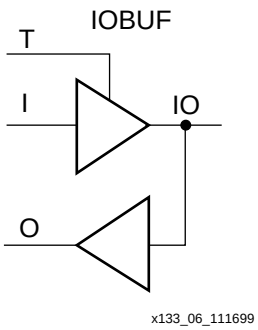

Figure 5: Input/Output Buffer (IOBUF) Symbol

3-state output buffers and bi-directional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

HDL Entry

SelectI/O components can be easily instantiated in VHDL or Verilog code. The Xilinx Foundation development system includes a Language Assistant that provides templates for any of the standard I/O components. Following is an example of the template for the IOBUF input/output buffer component. Note that registers can automatically be merged into the Spartan-II SelectI/O block, simplifying the generation of the HDL code

```
--Replace the XXX with the appropriate I/O standard
-- INOUT_PORT : inout STD_LOGIC;
--**Insert the following between the
--  'architecture' and 'begin' keywords**
   signal IN_SIG, OUT_SIG, T_ENABLE:  std_logic;
component IOBUF_XXX
      port (I, T: in std_logic;
            O: out std_logic;
            IO: inout std_logic);
end component;
   --**Insert the following after the 'begin' keyword**
U1: IOBUF_XXX port map (I => OUT_SIG, T => T_ENABLE,
              O => IN_SIG, IO => INOUT_PORT);
```

5V Tolerance

When the input buffer symbol (IBUF, IBUFG, or IOBUF) used supports an I/O standard that does not require a differential amplifier input (LVTTL, LVCMOS2, or PCI33_5), and the V_{CCO} within the given I/O bank is greater than 2V, the input automatically configures with a 5V-tolerant input buffer. If placing the single-ended input in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V-tolerant.

When the input symbol used supports an I/O standard that requires a differential amplifier input, the input automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

In summary, the following lists the Spartan-II SelectI/O standards for which the input and output buffers are 5V tolerant:

- LVTTL
- LVCMOS2
- PCI33_5

The 3V PCI I/O standards do not include 5V tolerant input and output buffers.

I/O Placement Rules

Each Spartan-II device provides eight banks of I/O, two per edge, for supporting multiple I/O standards on the same device. This allows multiple V_{REF} and V_{CCO} values on the same device. It is important to understand the restrictions on placement based on the availability of these banks.

Note that there is no power-up sequence requirement for the V_{CCO}, V_{REF}, and V_{CCINT} pins. The user can start with either supply first with no effect to the device This makes the Spartan-II device ideal for HotSwap and CompactPCI applications.

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device. A resistor divider can be used to generate the source voltage, since the current required by V_{REF} is typically less than 10 µA.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 6 for a representation of the Spartan-II I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

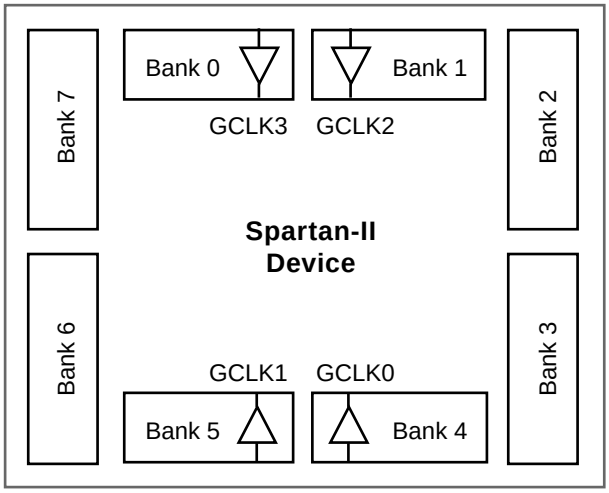

Figure 6: Spartan-II I/O Banks

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank. Table 4 summarizes the Spartan-II input standards compatibility requirements.

Table 4: Xilinx Input Standards Compatibility Requirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The Spartan-II Fine-Pitch Ball Grid Array (FG) packages provide eight V_{CCO} banks. The Spartan-II Chip Scale (CS) and Thin Quad Flat Pack (TQ) packages support four V_{CCO} banks. The Spartan-II Plastic QFP (PQ) and Very Thin QFP (VQ) packages support only one V_{CCO} bank.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers of any type and GTL output buffers can be placed within any V_{CCO} bank. Table 5 summarizes the Spartan-II output standards compatibility requirements.

Table 5: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards which share compatible V_{CCO} may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	PCI, LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design. See the Spartan-II data sheet for pin names and bank locations.

The LOC properties use the following form.

LOC = A12

LOC = P37

Design Considerations

While the SelectI/O features are easy to use, attention to the following design considerations can help avoid pitfalls and improve success.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5 inches for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques.

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 7.

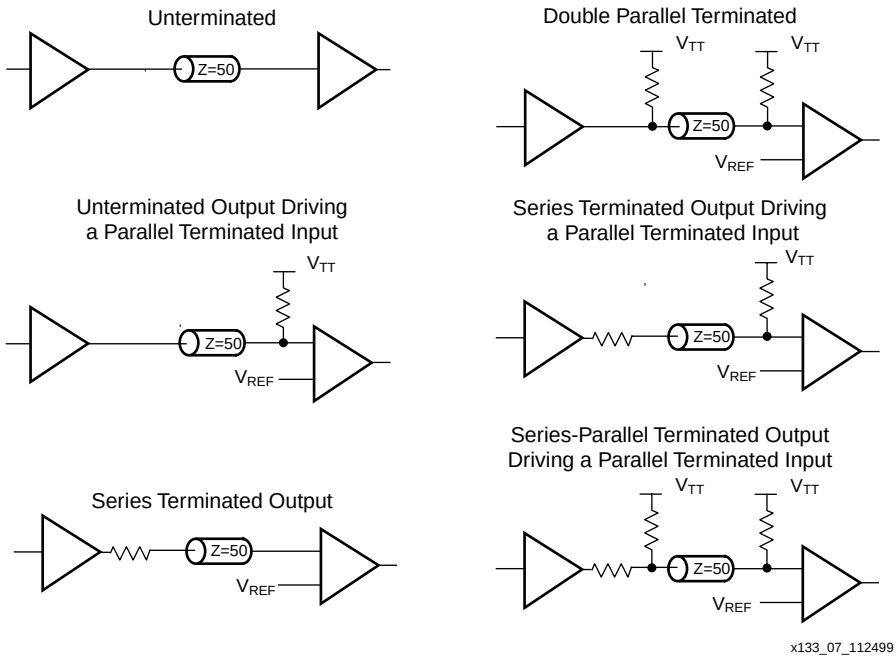

Figure 7: Overview of Standard Input and Output Termination Methods

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 6 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 7 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

Table 6: Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair

Standard	Package	
	CS, FGA	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVCMOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

Note: This analysis assumes a 35 pF load for each output.

Table 7: Effective Output Power/Ground Pairs for Spartan-II Devices

Package	Spartan-II Devices				
	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150
VQ100	8	8	-	-	-
CS144	12	12	-	-	-
TQ144	12	12	12	12	-
PQ208	-	16	16	16	16
FG256	-	-	16	16	16
FG456	-	-	-	48	48

Useful Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 8.

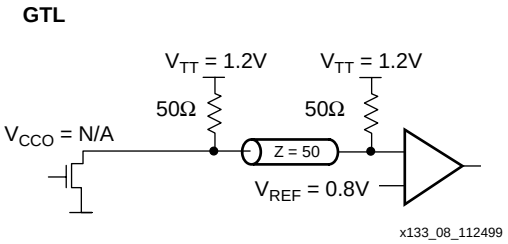

Figure 8: Terminated GTL

Table 8 lists DC voltage specifications.

Table 8: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$ (1)	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} – 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Note:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 9. DC voltage specifications appear in Table 9.

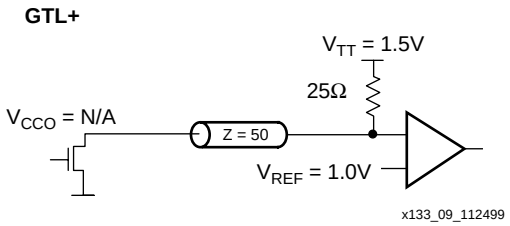

Figure 9: Terminated GTL+

Table 9: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$ 1	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.08	1.2	-
$V_{IL} = V_{REF} – 0.2$	-	0.8	0.92
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Note:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 10. HSTL Class I DC voltage specifications appear in Table 10.

HSTL Class I

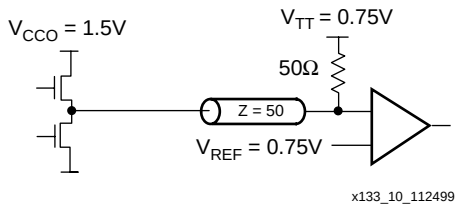

Figure 10: Terminated HSTL Class I

Table 10: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}		-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 11. DC voltage specifications appear in Table 11.

HSTL Class III

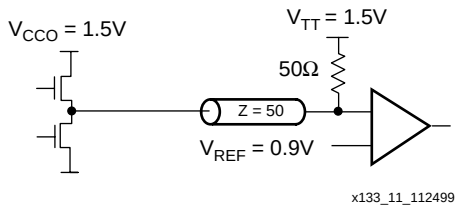

Figure 11: Terminated HSTL Class III

Table 11: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 12. DC voltage specifications appear in Table 12.

HSTL Class IV

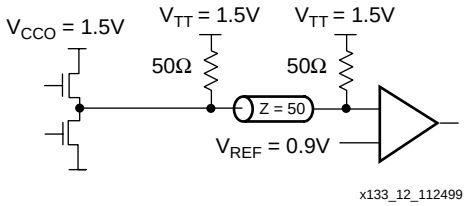

Figure 12: Terminated HSTL Class IV

Table 12: HSTL Class IV Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Note:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 13. DC voltage specifications appear in Table 13.

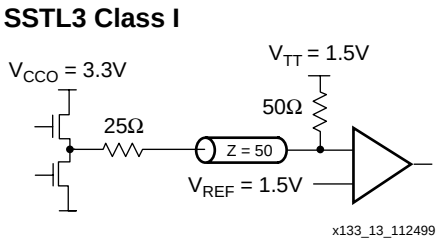

Figure 13: Terminated SSTL3 Class I

Table 13: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	2.1	-
$V_{OL} = V_{REF} – 0.6$	-	0.9	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3.
2. V_{IL} minimum does not conform to the formula.

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 14. DC voltage specifications appear in Table 14.

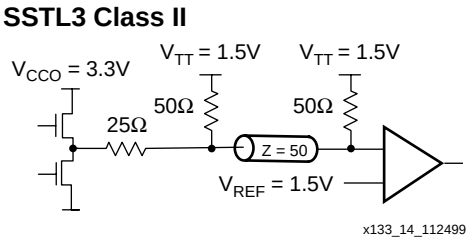

Figure 14: Terminated SSTL3 Class II

Table 14: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	2.3	-
$V_{OL} = V_{REF} – 0.8$	-	0.7	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3.
2. V_{IL} minimum does not conform to the formula.

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 15. DC voltage specifications appear in Table 15.

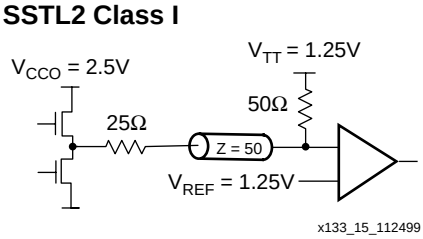

Figure 15: Terminated SSTL2 Class I

Table 15: SSTL2_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.03	1.17
$V_{OH} = V_{REF} + 0.05$	1.76	1.82	1.96
$V_{OL} = V_{REF} – 0.05$	0.54	0.68	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 16. DC voltage specifications appear in Table 16.

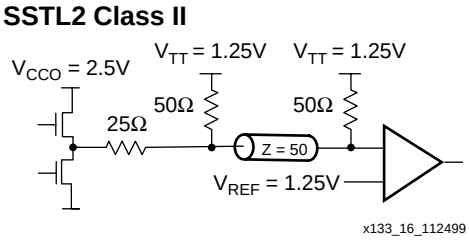

Figure 16: Terminated SSTL2 Class II

Table 16: SSTL2_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.8$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} - 0.8$	–0.3(3)	1.07	1.21
V_{OH}	1.95	2.01	-
V_{OL}	-	0.49	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appears in Figure 17. DC voltage specifications appear in Table 17 .

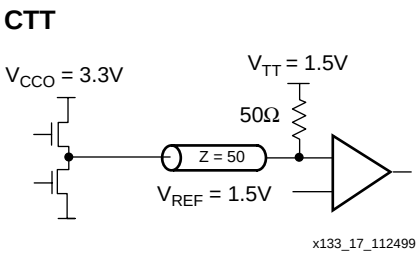

Figure 17: Terminated CTT

Table 17: CTT Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.05[1]	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} – 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} = V_{REF} – 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Note:

1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 18.

Table 18: PCI33_3 and PCI66_3 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.6 \times V_{CCINT}$	1.425	1.5	3.6
$V_{IL} = 0.4 \times V_{CCINT}$	–0.5	1.0	1.05
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Note:

1. Tested according to the relevant specification.

PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 19.

Table 19: PCI33_5 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.425	1.5	5.5
V_{IL}	–0.5	1.0	1.05
V_{OH}	2.4	-	-
V_{OL}	-	-	0.55
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Note:

1. Tested according to the relevant specification.

LVTTL

LVTTL requires no termination. DC voltage specifications appear in Table 20.

Table 20: LVTTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	5.5
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 21.

Table 21: LVCMOS2 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	5.5
V_{IL}	–0.5	-	0.7
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL}at V_{OL} (mA)	12	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 22.

Table 22: AGP-2X Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$(1)	1.17	1.32	1.48
$V_{TT} = V_{REF}$	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} = V_{REF} – 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL} at V_{OL} (mA)	Note 2	-	-

Note:

1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

Revision History

Date	Version	Revision
11/24/99	1.0	Initial release.