XF8250 Asynchronous Communications Core

September 16, 1999 Product Specification

Memec Design Services

7810 South Hardy Drive, Suite 104
Tempe, Arizona 85284 USA
Phone: +1 888-845-5585 (USA)
+1 480-753-5585
Fax: +1 480-753-5899
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Features

- Compatible with Xilinx CORE Generator tool
- Function compatible with Industry Standard 8250
- Combined UART and Baud Rate Generator
- DC to 625K baud (DC to 10 MHz Clock)
- 1 to 65535 divisor generates 16X clock
- Prioritized interrupt mode
- Microprocessor bus oriented interface
- Modem interface Line break generation and detection
- Loopback and Echo modes

Applications

- Serial data communications applications
- Logic consolidation

AllianceCORE™ Fact

Core Specifics		
Device Family	XC4000E/XL	Spartan
CLBs Core Core+Ext logic	 114 114	 114 114
CORE I/O Core [1] Core+Ext logic	 39 36	 39 36
Systems Clock fmax	10+MHz[2]	
Device Features Used	Tbufs, global clock buffers	
Provided with Core		
Documentation	Core schematics, User's guide, Application notes, FAQ, Implementation instructions	
Design File Formats	.ngo netlist Viewlogic, Foundation or Verilog source files available extra	
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim, Testbench for Foundation, VHDL and Verilog.	
Symbols	ViewLogic, Foundation Instantiation templates for VHDL and Verilog	
Constraint Files	.ucf	
Evaluation Model	None	
Reference designs & application notes	Sample designs in Viewlogic, Foundation, VHDL and Verilog	
Additional Items	Warranty by MDS Netlist only version available on enCORE CD-ROM	
Design Tool Requirements		
Xilinx Core Tools	Alliance/Foundation 1.4	
Support		
Support provided by Memec Design Services.		

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed to meet industry standard specification

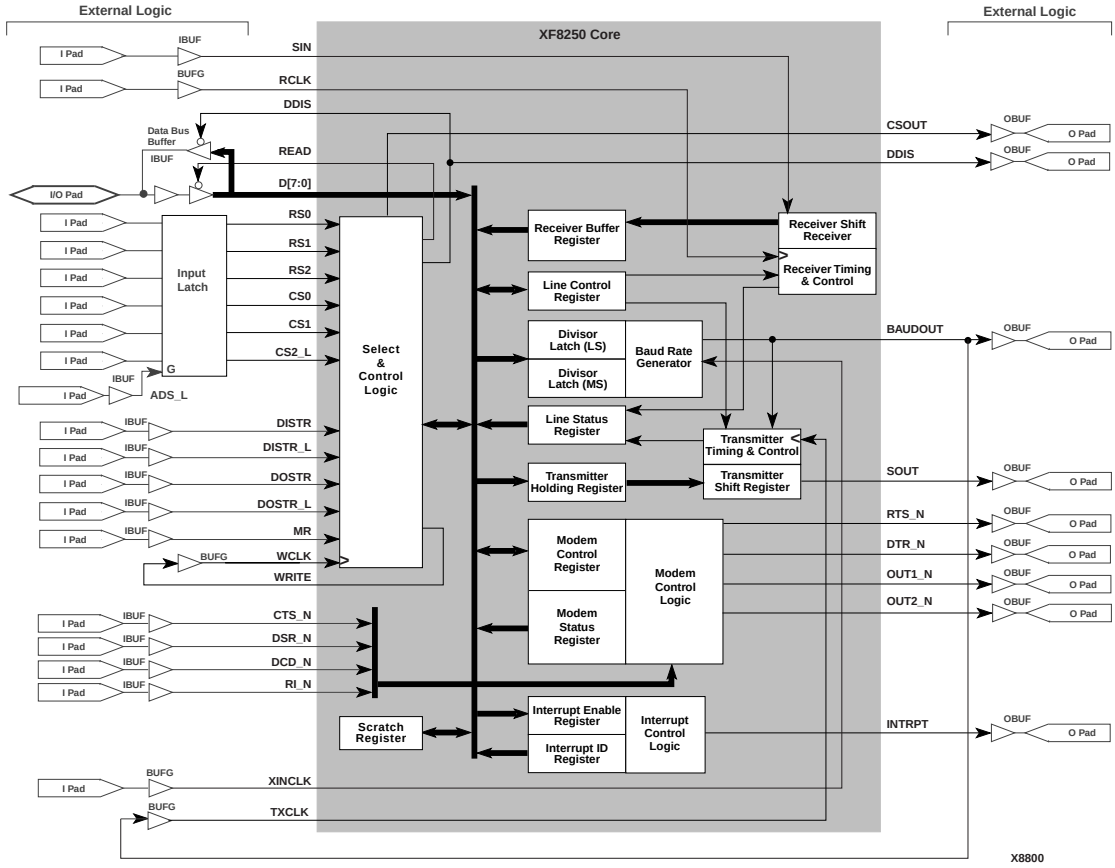

Figure 1: XF8250 Asynchronous Communications Core Block Diagram

General Description

The XF8250 Asynchronous Communications Core is a high-performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, then run through a global buffer, then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core inorder to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

Functional Description

The XF8250 core is partitioned into modules as shown in Figure 1 and described below. Refer to the XF8250 User's Guide for detailed technical information. The User's Guide is available directly for MDS.

Select and Control Logic

This controls and decodes commands for the core and the direction of the data bus buffer.

Scratch Register

This register is an 8-bit Read/Write register which has no effect on the XF8250. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

Line Control Register (LCR)

This register controls the format of the data character. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory.

Line Status Register (LSR)

A single register that provides status indications, the LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the XF8250.

Transmitter Holding Register

This register holds parallel data from the data bus, D[7:0], until the Transmitter Shift Register is empty and ready to accept a new character for transmission.

Modem Control Register (MCR)

This controls the interface to the modem or data set. The MCR is a read/write register.

Modem Status Register (MSR)

This provides the CPU with the status of the modem input lines from the external device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the XF8250.

Interrupt Enable Register

This is a Write register used to independently enable the four XF8250 interrupts that activate the interrupt (INTRPT) output.

Interrupt ID Register

This register provides the XF8250 with interrupt capability for interfacing with microprocessors. In order to minimize software overhead during data character transfers, the XF8250 has four levels of interrupt priorities:

- Priority 1 -Receiver Line Status
- Priority 2 -Received Data Ready
- Priority 3-Transmitter Holding Register Empty
- Priority 4 -Modem Status

Baud Rate Generator

This divides the clock by a 16-bit divisor to generate the 16x baud rate clock (BAUDOUT).

Receiver Shift Register

This register is programmable for 5, 6, 7, or 8 data-bits per character.

Receiver Timing & Control

This block detects the start-bit, controls the sampling of the asynchronous receive data (SIN), and determines when a complete word has been shifted into the receiver shift register.

Contact Memec Design Services for descriptions of other blocks in Figure 1.

Core Modifications

The XF8250 meets or exceeds the AC Specifications of the industry standard 8250. However, in most cases the timespecs can be tightened significantly. Successful operation with 120 ns bus cycles has been achieved. In all cases, a post- route timing analysis should be performed to verify performance. Implementation beyond 10 MHz and other customization is available through Memec Design Services.

Pinout

The XF8250 may be implemented as stand alone logic using the provided pinout or may be implemented internally with the user's design. Both versions are included with the Core deliverables. Signal names are provided in the block diagram shown in Figure 1 and Table 1.

Core Assumptions

Deviations from the industry standard 8250 functional specification are described below.

Stop-Bit Programming

When the UART is programmed for two stop-bits (1.5 in 5-bit mode), the receiver does not check the level of the second stop- bit. If the first stop-bit is high and the second stop-bit is either high or low, the receiver moves the shift register contents into the Receiver Buffer Register without posting a framing error. In the majority of applications, this will not cause a problem. However, in cases where a corrupted second stop-bit must be reported as a framing error, the receiver will need modification.

External Crystal Support

This core does not support connection of a crystal directly to the device.

Baud Rate Generator

The Baud Rate Generator differs from the industry standard in the following ways.

Divide by Zero -A divisor value of 0x0000 acts like divide by 65536, where BAUDOUT is high for one XINCLK period and low for 65535 XINCLK periods.

Other Division - For all divisor values between 0x0001 and 0xffff, the BAUDOUT signal is high for one XINCLK period

and low for N-1 XINCLK periods, where N is the divisor value. For divisors of 0x0001 through 0x0003, the BAUDOUT signal is identical to the industry standard datasheet.

Verification Methods

Complete functional and timing simulation has been performed on the XF8250 using ViewSim. (Simulation vectors used for verification are provided with the core.) This core has also been used successfully in customer designs.

Available Support Products

Memec Design Services supplies a Xilinx-based FPGA Development Module that can be used to hardware test this and other MDS cores. To purchase this, or to obtain more information, contact MDS directly.

Recommended Design Experience

For the source code versions, users should be familiar with ViewLogic Workview Office or Foundation schematic entry, or Verilog HDL and Xilinx design flows. For the netlist version, users should be familiar with Workview office, Xilinx Foundation, Verilog simulation/synthesis or VHDL simulation/synthesis.

Users should also have experience with microprocessor systems.

Ordering Information

The XF8250 Asynchronous Communications Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

Information furnished by Memec Design Services is believed to be accurate and reliable. Memec Design Services reserves the right to change specifications detailed in this data sheet at any time without notice, in order to improve reliability, function or design, and assumes no responsibility for any errors within this document. Memec Design Services does not make any commitment to update this information.

Memec Design Services assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction, if such be made, nor does the company assume responsibility for the functioning of undisturbed features or parameters.

Memec Design Services will not assume any liability for the accuracy or correctness of any support or assistance provided to a user.

Table 1: Core Signal Pinout

READ	Signal Direction	Description
SIN	Input	Serial Data Input
RCLK	Input	16x Baud for Receiver
DDIS	Output	Driver Disable
READ	Output	Read From Data Bus
D[7:0]	In/Out	Data bits 7-0
RS0	Input	Register Selects
RS1	Input	Register Selects
RS2	Input	Register Selects
CS0	Input	Chip Select 0
CS1	Input	Chip Select 1
CS2_L	Input	Chip Select 2
DISTR	Input	Data In Strobe
DISTR_L	Input	Data In Strobe
DOSTR	Input	Data Out Strobe
DOSTR_L	Input	Data Out Strobe
MR	Input	Master Reset
WCLK	Input	Register Write Pulse In
WRITE	Output	Register Write Pulse Out
CTS_N	Input	Clear To Send
DSR_N	Input	Data Set Ready
DCD_N	Input	Data Carrier Detect
RI_N	Input	Ring Indicator
XINCK	Input	Baud Rate Source Clock
TXCLK	Input	Transmit Clock
CSOUT	Output	Chip Select Out
BAUDOUT	Output	BAUDOUT
SOUT	Output	Serial Data Output
RTS_N	Output	Request to Send
DTR_N	Output	Data Terminal Ready
OUT1_N	Output	Output 1
OUT2_N	Output	Output 2
INTRPT	Output	Interrupt Request

Memec Design Services does not represent that products described herein are free from patent infringement or from any other third-party right. No license is granted by implication or otherwise under any patent or patent rights of Memec Design Services.

Memec Design Services products are not intended for use in life support appliances, devices, or systems. Use of a Memec Design Services product in such application without the written consent of the appropriate Memec Design Services officer is prohibited.

All trademarks, registered trademarks, or servicemarks are property of their respective owners

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm