# XF8255 Programmable Peripheral Interface

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Memec Design Services

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## Features

- Compatible with Xilinx CORE Generator tool
- Software and function compatible with Industry Standard 8255
- 24 programmable I/O pins
- Fully compatible with most microprocessor families
- Direct bit set/reset capability easing control application interface

## Applications

- Embedded Microprocessor Control

## General Description

The XF8255 Programmable Peripheral Interface Core is a general purpose programmable I/O device designed for use with most microprocessors. It has 24 I/O pins which may be individually programmed in two groups of 12 and used in three major modes of operation.

The first mode, MODE 0, is basic input/output operation where ports A and B are 8 bits wide and Port C is split into upper and lower halves of 4 bits each. Port A, Port B, Port C upper, and Port C lower can each be independently configured as input or output. This gives a total of 16 direction combinations.In MODE 1 each group may be programmed to have eight lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals. The third mode of operation, MODE 2, is only available on the Group A ports (Port A and Port C upper). It is a bi-directional bus mode that uses eight lines for a bi-directional bus, and five lines (borrowing one from the other group) for handshaking and interrupt control signals.

## AllianceCORE™ Facts

| Core Specifics | | |
|---|---|---|
| Device Family | XC4000E/XL | Spartan |
| CLBs Used<br>Core<br>Core +Ext logic | <br>64<br>64 | <br>64<br>64 |
| Core I/O<br>Core[1]<br>Core +Ext logic | <br>97<br>38 | <br>97<br>38 |
| System Clock $f_{max}$ | No External Clock[2] | |
| Device Features Used | Tbufs, global clock buffers, input latches | |
| **Provided with Core** | | |
| Documentation | Users guide, application notes implementation instructions | |
| Design File Formats | .ngo netlist<br>Viewlogic source files (schematics) available extra | |
| Constraint Files | .ucf | |
| Verification Tool | Machine-readable simulation vectors for ViewLogic ViewSim, Testbenches for VHDL and Verilog | |
| Symbols | ViewLogic, Foundation, VHDL, Verilog | |
| Evaluation Model | None | |
| Reference designs & application notes | Sample designs in Viewlogic, Foundation, VHDL and Verilog | |
| Additional Items | Warranty by MDS, netlist only version available on enCORE CD-ROM | |
| **Design Tool Requirements** | | |
| Xilinx Core Tools | Alliance/Foundation 1.4 | |
| **Support** | | |
| Support provided by Memec Design Services. | | |

Notes:

1. Assuming all core signals are routed off-chip.
2. Function does not have a clock, but will, at a minimum, perform no wait-state operation alongside an 8 MHz 80C86.

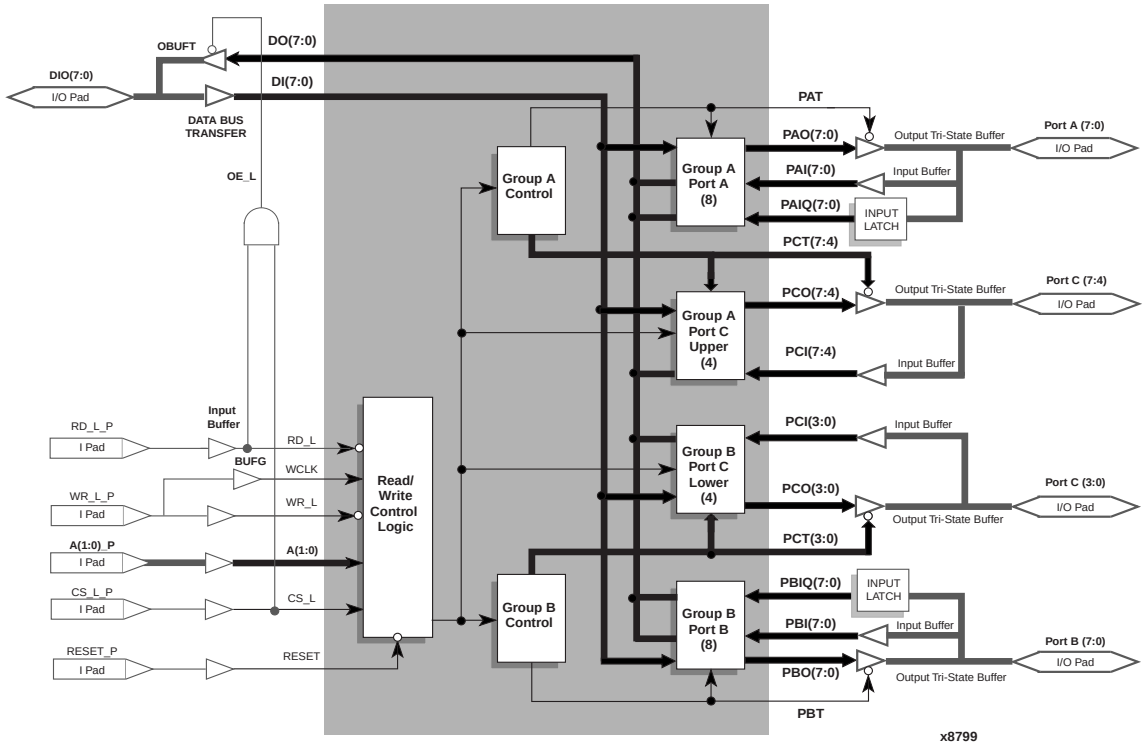


**Figure 1: XF8255 Block Diagram**

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance where one of our cores generates a clock, that signal is brought out of the core, then run through a global buffer, then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this design philosophy is that the cores are not self-contained. External logic must be connected to the core in order to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

# Functional Description

The XF8255 is partitioned into modules as shown in Figure 1 and described below.

## Read/Write Control Logic

This logic manages all of the internal and external transfers of both Data and Control or Status words.

## Group A and Group B Controls

The system software programs the functional configuration of each port. Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control Logic, receives “control words” from the internal data bus, and issues the proper commands to its associated ports.

- Control Group A - Port A and Port C upper (C7 – C4)
- Control Group B - Port B and Port C lower (C3 – C0)

The control word register can be both written and read. When the control word is read, bit D7 will always be logic “1”, as this implies control word mode information.

***Port A:***

One 8-bit data output latch/buffer and one 8-bit data input latch.

***Port B:***

One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

***Port C:***

One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control.

Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

# Pinout

The XF8255 may be implemented as stand-alone logic using the provided sample designs or may be implemented internally with the user’s design. Both versions are included with the Core deliverables. Signal names are provided in the block diagram shown in Figure 1, and Table 1.

# Core Assumptions

## Bus-Hold Capability

Ports A, B, and C do not have Bus-Hold capability. This would require two OBUFTs per port pin. Since Xilinx devices only have one OBUFT per pin, it would take two Xilinx pins connected together externally for each port pin.

Workaround: Most applications don't require Bus-Hold capability, but for those that do, a customized version of the XF8255 core can be developed.

**Table 1: Core Signal Pinout**

| Signal | Signal Direction | Description | |
|---|---|---|---|
| DI[7:0] | Input | Data bus input. | |
| DO[7:0] | Output | Data bus output. | |
| RESET | Input | RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode. | |
| CS_L | Input | CHIP SELECT: An active low input used to enable the XF8255 onto the data bus for CPU communications. | |
| RD_L | Input | READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus. | |
| WR_L | Input | WRITE: Write does the CPU to load control words and data into the XF8255 use an active low input control signal. | |
| WCLK | Input | Write clock. This is the clock input to all clock registers. It is usually sourced from a global clock buffer (BUFG). | |
| A[1:0] | Input | PORT ADDRESS: These input signals, in conjunction with the RD_L and WR_L inputs, control the selection of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the address bus A0, A1. | |
| PAI[7:0] | Input | Port A 8-bit input buffer. | These four signals comprise Port A |
| PAO[7:0] | Output | Port A output register | |
| PAIQ[7:0] | Input | Port A 8-bit input latch. | |
| PAT | Output | Port A output enable. | |
| PBI[7:0] | Input | Port B 8-bit input buffer. | These four signals comprise Port B |
| PBO[7:0] | Output | Port B output register. | |
| PBIQ[7:0] | Input | Port B 8-bit input latch. | |
| PBT | Output | Port B output enable. | |
| PCI[7:0] | Input | Port C 8-bit input. | These three signals comprise Port C |
| PCO[7:0] | Output | Port C 8-bit Output register. | |
| PCT[7:0] | Output | Port C 8-bit output enables. | |

## Core Modifications

The XF8255 is designed to meet or exceed the AC Specifications of the industry standard 8255. However, in most cases the Timespecs can be tightened significantly. In all cases, a post-route timing analysis should be performed to verify performance. Implementation and other customizing is available through Memec Design Services.

## Verification Methods

Complete functional and timing simulation has been performed on the XF8255 using ViewSim ModelSim – VHDL, Silos3 - Verilog. (Simulation vectors used for verification are provided with the core.)

## Recommended Design Experience

For the source version, users should be familiar with View-Logic Workview Office schematic entry and Xilinx design flows. For the netlist version, users should be familiar with Workview office, Xilinx Foundation, Verilog simulation/synthesis or VHDL simulation/synthesis.

Users should also have experience with microprocessor systems.

## Additional Support

Memec Design Services supplies a Xilinx-based FPGA Development Module that can be used to hardware test this and other MDS cores. To purchase this, or obtain more information, contact MDS directly.

## Ordering Information

The XF8255 Programmable Peripheral Interface Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact MDS for pricing and more information.

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## Related Information

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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