Fast Ethernet MAC Core Evaluation Board

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Product Specification

CoreEl MicroSystems

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Features

- Fully compliant with IEEE 802.3 10 Mbps and 100Mbps standards.
- Fully compatible with industry standard Network Interface Cards (NIC) for PC-AT.
- Implemented using two Xilinx XC4028EX FPGAs.
  - One for the CoreEl Ethernet MAC transmitter and receiver cores.
  - Other for ISA bus interface and glue logic.
- SEEQ 80221 chip provides physical line interface.
- Included are Both transmitter and receiver cores plus reference design for a complete NIC card.
- Industry standard 16-bit ISA interface.
- The card is supplied with a Windows NT 4.0 (NDIS) driver.
- Supports on board buffer of 8Kbytes.
- Jumper programmable address space and interrupt number.

General Description

The Fast Ethernet MAC Core Evaluation Board is a Xilinx-based hardware platform that is ideal for testing the functioning of the CoreEl Fast Ethernet Media Access Controller Transmitter and Receiver Cores. It has a standard 16 bit ISA bus interface for host PC.

Functional Description

The entire peripheral circuitry is designed to check the feature list of MAC. The PHY device as shown in Figure 2, provides the connection between the MAC and physical medium using the standard MII interface. The host configures the card by writing into the configuration registers. The status of current TX / RX process can be read from the status register.

Packet Reception

Data from the PHY device is accepted by the MAC receiver. The Rx Controller takes this data from the MAC and stores it in the memory. At the end of a successful packet reception, a bit in the Rx status register is set for generating an interrupt to the host. The host then reads the packet data from the memory through the Host controller.

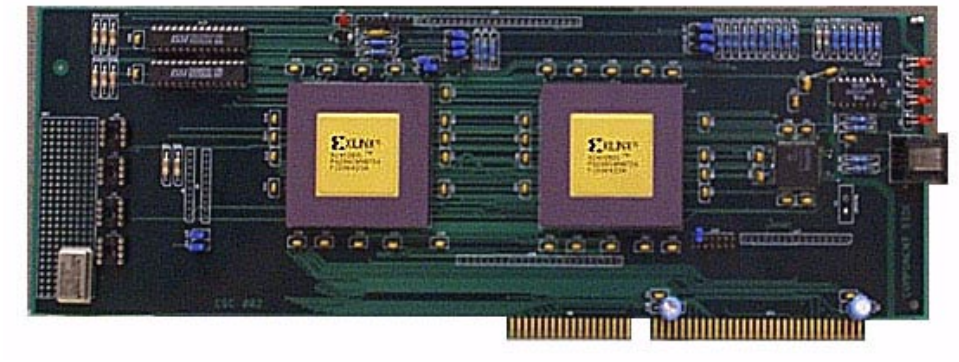

Figure 1: 10/1000 Ethernet NIC Board

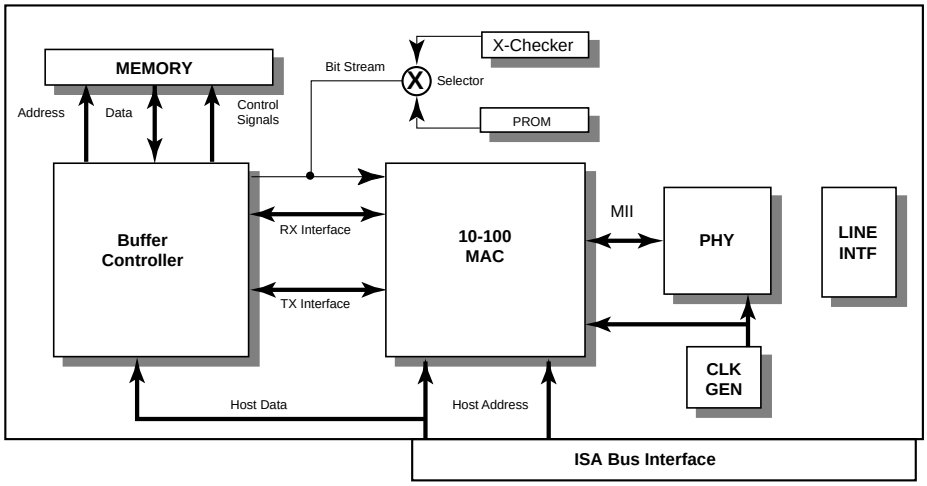

Figure 2: Fast Ethernet MAC Core Evaluation Board Block Diagram

Packet Transmission

The host controller takes the data to be transmitted from the host and stores it in the memory. Once the full packet is received from the Host, host controller generates request to the Tx controller to do the packet transfer. The TX controller in turn reads this data from the memory and gives it to the MAC TX for transmission on to the PHY.

Available Support Products

CoreEl provides a complete line of support products to help you develop your Fast Ethernet MAC design. These products are listed below and must be purchased separately.

- Fast Ethernet Media Access Controller Transmitter and Receiver Cores
- FEM Test Bench

Ordering Information

To order or obtain more information on this or other products mentioned in this datasheet, contact CoreEl MicroSystems directly.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
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For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
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For AllianceCORE™ specific information, contact:

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