UTOPIA Master (CC140f)

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CoreEl MicroSystems

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Features

- Conforms to ATM Forum's UTOPIA Level 2 specifications, Version1.0
- 8/16 bit UTOPIA operation
- SPHY operation supports Octet Level and Cell Level handshake
- MPHY operation with Single or Double Clav
- 32 bit Data transfer on ATM interface
- Statistics Feature on Transmitter and Receiver
- Round Robin Polling of ports on logical port basis
- Logical to Physical Address translation for port polling and selection
- Parity check and error reporting in Receive direction
- Parity generation in Transmit direction
- Insertion of Dummy HEC in transmit direction
- Removes HEC byte in receive direction
- Operates at 50/33/25MHz on XC4000XL-1 Device

AllianceCORE™ Facts

Core Specifics[1]	
Device Family	XC4000XL
CLBs - Transmitter CLBs - Receiver	254 204
IOBs - Transmitter IOBs - Receiver	123[1] 126[1]
CLKIOBs - Tx CLKIOBs - Rx	1 1
System Clock f_{max}	50MHz
Device Features Used	SelectRAM™

Supported Devices/Resources Remaining[1]		
	I/O	CLBs
XC4013XL-1-BG256 (Tx)	69	322
XC4013XL-1-BG256 (Rx)	66	388

Provided with Core	
Documentation	Product Brief Datasheet Design Document Testbench Design Document
Design File Formats	VHDL Compiled EDIF netlist
Constraint Files	Transmitter: Txtop.ucf Receiver: Rxtop.ucf
Verification Tool	Script based behavioral VHDL test bench
Schematic Symbols	None
Evaluation Model	Behavioral VHDL
Reference designs & application notes	UTOPIA Level 2 Specification V1.0
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.3
Entry/Verification Tool	Model Tech V-System

Support
Support provided by CoreEl Microsystems

Note:
1. Assuming all core signals are routed off-chip.

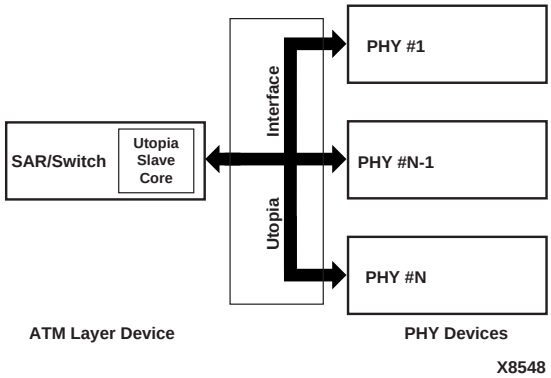

Figure 1: Data transfer between ATM layer device and UTOPIA compatible PHY devices

Applications

The Master UTOPIA core (MUC) can be used in any Asynchronous Transfer Mode (ATM) Layer Device that manages data transfer with PHY devices, including Switch, SAR and NIC circuits. The MUC facilitates data transfer between the UNI (User Network Interface device) in ATM networks and a UTOPIA compatible ATM layer device as shown in Figure 1. In SPHY operation, it supports octet level handshake and cell level handshake. In MPHY operation, it supports up to 31 PHY devices.

General Description

The UTOPIA Master core consists of separate transmitter and receiver modules. The transmitter provides an industry standard interface between the ATM layer and PHY devices through a shift register. It supports both SPHY and MPHY modes of operation.

In MPHY mode it supports 31 PHY devices. It accepts cells of sizes 54 or 53 bytes from the ATM layer, reads them

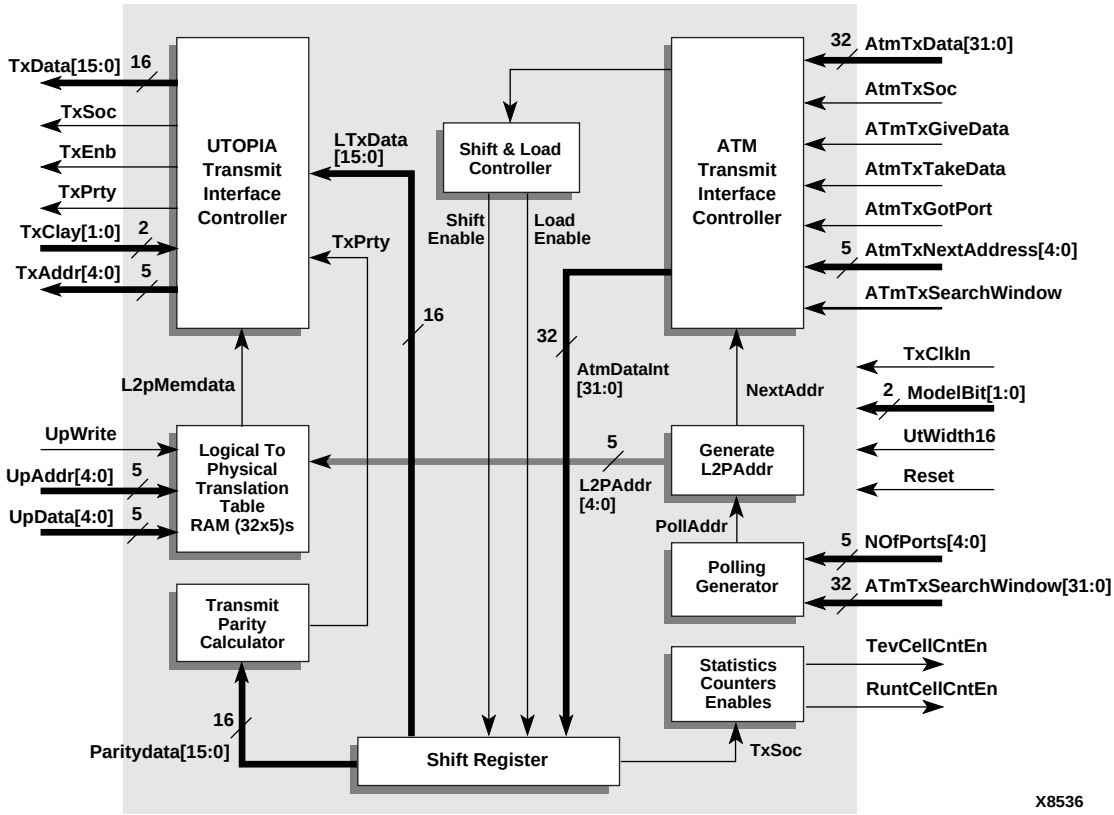

Figure 2: Master UTOPIA Transmitter Block Diagram

using TxClkIn, inserts a dummy HEC byte and sends them to a PHY device using TxClkIn. It computes parity on received bytes and outputs this to the PHY device using TxPrty. It generates count enables for counting number of cells or runt cells transmitted.

The receiver supports both SPHY (Cell-Level handshake or octet level handshake) and MPHY (supports up to 31 PHY devices) modes of operation. In MPHY mode it polls 31 PHY devices on a logical address basis and outputs poll status to the ATM layer. It accepts cells of sizes 54 or 53 bytes from the PHY device, runs these through a shift register and outputs 32-bit data on the ATM side using RxClkIn.

The receiver removes the HEC byte from cells received from the PHY. It also performs parity check and gives the user the option of discarding cells on the occurrence of a parity error. It generates enables for counting number of cells, runt cells, excess cells and cells with parity error received.

Transmitter Functional Description

The MUC Transmitter is architecturally divided into blocks as shown in Figure 2, and described below.

Transmit Interface Controller-UTOPIA

This module generates TxEnb signal for various handshake modes. It asserts TxEnb if 32 bit data is available, and deactivates TxEnb if no data is available in the bank. Other functions of this block includes:

- Generating poll addresses on TxAddr bus
- Generating parity with Txdata
- Detecting status of PHY device through TxClav port
- Validation of TxData.

Transmit Parity Calculator

This module calculates parity one clock before it is sent on TxData bus. The word is divided in two bytes in the 16 bit

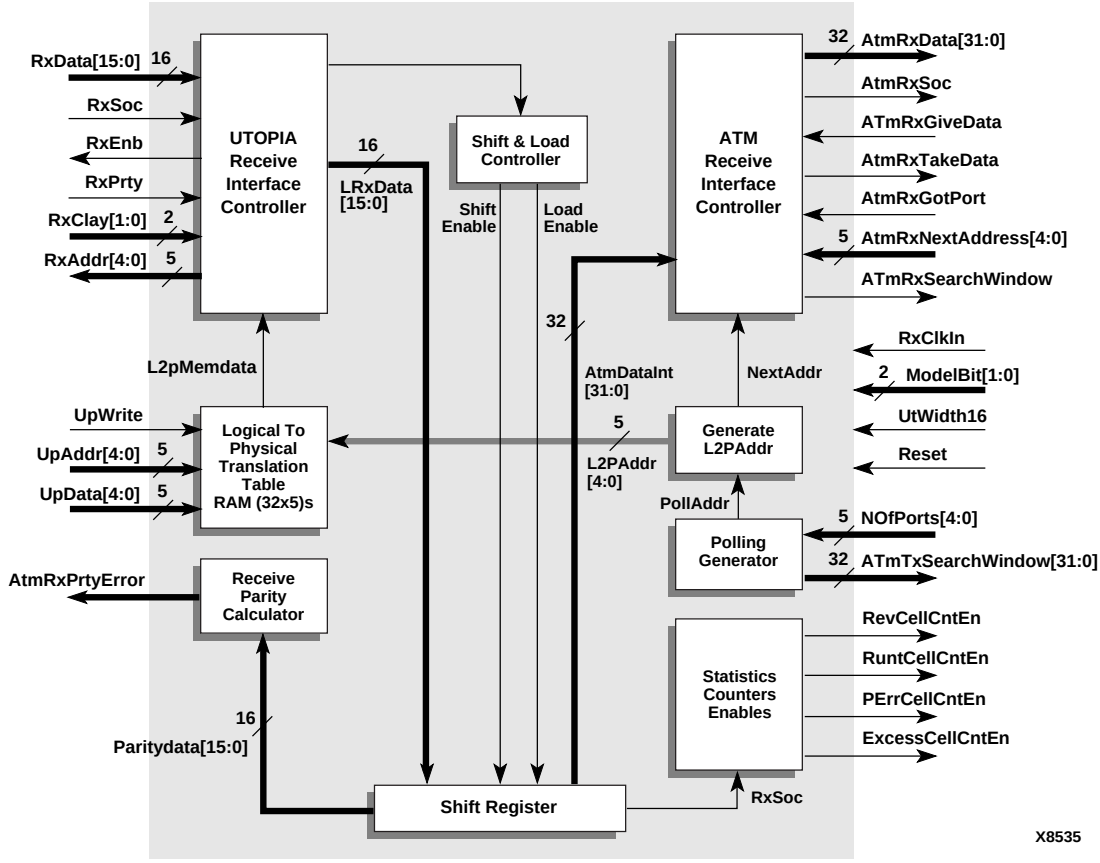

Figure 3: Master UTOPIA Receiver Block Diagram

case. Parity is generated separately on each byte and combined to give TxPrty. Data is given out with odd parity.

Logical To Physical Translation Table-RAM (32x5s)

This module stores the physical addresses of the active PHY devices to be polled. It converts the logical address into Physical address which is seen on the TxAddr bus. The user can write to this table using UpData, UpAddr and UpWrite signals.

Polling Generator

This module generates the polling address. It also reports PHY device status on 32 bit bus to ATM side. The Clav status is reported after one clock cycle once Clav is detected.

Statistics Counters Enables

This module generates enables for statistics counters. It generates Count Enables for total cells and runt cells transmitted.

Shift Register

This is used for data on the UTOPIA side. It takes input from the Shift and Load Controller and outputs to the Parity Calculator and Transmit Interface Controller UTOPIA blocks.

Transmit Interface Controllership

This module uses data and control signals from the ATM layer to generate new control signals. This block also responds to the UTOPIA side and informs the ATM side through appropriate control signals.

Generate L2PAdder

This module generates addresses for the Logical To Physical Translation Table. During polling phase the Polladdr is given as L2pAddr. In port selection phase, Port Selection address is given as L2pAddr. L2pAddr is the logical address for the Logical To Physical Address Translation Table.

Shift and Load Controller

This module latches data on the ATM Bus when validated by AtmTxSoc and loads in the shift register. Shifting data on the UTOPIA Interface is controlled by the Shift Controller. Once 32 bit Data is received it continues to shift data on a byte-by-byte basis, validated by TxEnb.

Receiver Functional Description

The MUC Receiver is architecturally divided into blocks as shown in Figure 3, and described below.

Receive Interface Controller-UTOPIA

This module generates RxEnb signal for various handshake modes. It can assert RxEnb if ATM device is ready to receive data. Other functions of this block include:

- Generating poll addresses on RxAddr bus
- Detecting status of PHY device through RxClav port
- Removing HEC byte from the cell.

Receive Parity Verifier

This module receives data from the Receive Interface Controller, generates parity and compares it with parity received from the PHY device. It reports parity errors to the ATM layer using AtmRxPrtyError signal.

Logical To Physical Translation Table-RAM (32x5s)

This module stores the physical addresses of the active PHY devices to be polled. It converts the logical address into physical address seen on the RxAddr bus. The user can write to this Table using UpData, UpAddr and UpWrite signals.

Polling Generator

This module generates the polling address. It also reports PHY device status over a 32-bit bus to the ATM side. Clav status is reported after one clock cycle once Clav is detected.

Statistics Counter Enable

This module generates enables for the statistics counters. It generates Count Enables for total cells, runt cells, excess byte cells and cells with parity error received.

Shift Register

This module maintains a shift register for shifting data on the ATM side. It takes input from the Shift and Load Controller and gives output to Receive Interface Controller ATM.

Receive Interface Controller-ATM

This module uses data and control signals from the ATM layer to generate new control signals. This block also responds to the UTOPIA side and informs the ATM side through appropriate control signals.

Generate L2PAdder

This module generates addresses for the Logical To Physical Translation Table. During polling phase the Polladdr is given as L2pAddr. In port selection phase, Port Selection address is given as L2pAddr. L2pAddr is the logical address for the Logical To Physical Address Translation Table.

Shift and Load Controller

This module latches data on the UTOPIA Bus when validated by Clav and loads it into the shift register. Data shifted on the ATM Interface is controlled by the Shift Controller. It counts the number of bytes received. Once four bytes are received, Data is shifted on ATM Interface.

Table 1: UTOPIA Transmit Interface

Signal	Signal Direction	Description
UTOPIA Transmit Interface Signals		
TxData[7:0]	Output	Least significant octet of transmit data. Bit 7 is MSB, Bit 0 is LSB in 8-bit data path.
TxData[15:8]	Output	Most significant octet of transmit data. Bit 15 is MSB, TxData 0 is LSB in 16-bit data path.
TxSOC	Output	Start of cell indication.
TxEnb	Output	Enable validates data on TxData Bus.
TxPrty	Output	Odd parity over 8/16 bit TxData.
TxClav[1:0]	Input	Transmit Cell Available - used in SPHY mode and one-Clav operation in MPHY mode. Bit 1 is used only in MPHY two Clav operation. In two-Clav operation, Bit 0 is for even ports and Bit 1 for odd ports for Clav status; active high.
TxAddr[4:0]	Output	Address of PHY device in MPHY configuration. Bit 4 is MSB.
TxClkin	Input	Transmit clock; uses 1 FPGA CLKIOB pin.
ATM Layer Transmit Interface Signals		
AtmTxData[31:0]	Input	Data input from ATM layer
AtmTxSoc	Input	Start of cell indication from ATM layer to MUC.
AtmTxGiveData	Output	Asseted by MUC to indicate it is ready to take data from ATM layer; active high.
AtmTxTakeData	Input	Asserted by ATM layer to indicate that valid data is present on data bus; active high.
AtmTxGotPort	Input	Validates address on ATM side address bus; active high.
AtmTxNextAddress[4:0]	Input	Address bus from ATM layer to MUC; generates port address for next cell transfer.
AtmTxSearchWindow	Output	Tells ATM layer to give next port address for cell transfer; active high.
AtmTxPortPollingStatus[31:0]	Output	Clav status of polled ports on 32 bit bus.
Configuration Interface Signals		
UpWrite	Input	Write Enable for Logical To Physical Translation Table.
UpAddr [4:0]	Input	Address for Logical To Physical Translation Table, starting from (00h to 1fh).
UpData [4:0]	Input	Data for Logical To Physical Translation Table.
TxClkIn	Input	Transmit Clock input.
ModeBit[1:0]	Input	Bit 0: 1 = SPHY, 0 = MPHY. Bit 1 SPHY operation: 0 = octet level handshake, 1 = cell level handshake. Bit 1 MHPY operation: 0 = 1 Clav operation, 1 = 2-Clav operation.
UtWidth16	Input	0 = 8 bit UTOPIA Bus Width, 1 = 16 bit UTOPIA Bus Width.
Reset	Input	System Reset.
NOfPorts[4:0]	Input	Number of ports polled in MPHY operation.
TcvCellCntEn	Output	Enable to count total number of cells.
RuntCellCntEn	Output	Enable to count total runt cells transmitted.

Table 2: UTOPIA Receive Interface

Signal	Signal Direction	Description
UTOPIA Receive Interface Signals		
RxData[7:0]	Input	Least significant octet of receive data, driven from PHY to MUC. Bit 7 is MSB, Bit 0 is LSB in 8-bit data path.
RxData[15:8]	Input	Most significant octet of receive data, driven from PHY to MUC. Bit 15 is MSB, Bit 0 is LSB in 16-bit data path.
RxSOC	Input	Start of cell indication.
RxEnb	Output	Tells PHY device to drive data, after sampling this signal low.
RxPrty	Input	Odd parity over 8/16 bit RxData.
RxClav[1:0]	Input	Receive Cell Available - used in SPHY mode and one-Clav operation in MPHY mode. Bit 1 is used only in MPHY two Clav operation. In two-Clav operation, Bit 0 is for even ports and Bit 1 for odd ports for Clav status; active high.
RxAddr[4:0]	Output	Address of MPHY device, driven from MUC to PHY to poll and select appropriate PHY device. Bit 4 is MSB.
RxClkin	Input	Receiver clock; uses 1 FPGA CLKIOB pin.
ATM Layer Receive Interface Signals		
AtmRxData[31:0]	Output	Data output from MUC to ATM layer.
AtmRxSOC	Output	Start Of Cell indication to ATM layer from MUC; active high.
AtmRxGiveData	Input	Indicates ATM layer is ready to take data from MUC; active high.
AtmRxTakeData	Output	Indicates presence of valid data on data bus; active high.
AtmRxGotPort	Input	Validates ATM side address; active high.
AtmRxNextAddress[4:0]	Input	ATM layer generates next port address for cell transfer.
AtmRxSearchWindow	Output	Tells ATM layer to give next port address for cell transfer; active high.
AtmRxPortPolling Status[31:0]	Output	Status output from MUC to ATM layer; status indicates readiness of various ports to give cells to ATM layer.
AtmRxPrtyError	Output	Data Path Parity Error; MUC computes odd parity over data path and compares with received parity.
Configuration Interface Signals		
UpWrite	Input	Write Enable for Logical To Physical Translation Table.
UpAddr[4:0]	Input	Address for Logical To Physical Translation Table, starting from (00h to 1fh).
UpData[4:0]	Input	Data for Logical To Physical Translation Table.
RxClkIn	Input	Receive Clock Input.
ModeBit[1:0]	Input	Bit 0: 1 = SPHY, 0 = MPHY. Bit 1 SPHY operation: 0 = octet level handshake, 1 = cell level handshake. Bit 1 MHPY operation: 0 = 1 Clav operation, 1 = 2-Clav operation.
UtWidth16	Input	0 = 8 bit UTOPIA Bus Width, 1 = 16 bit UTOPIA Bus Width.
Reset	Input	System Reset.
NOfPorts[4:0]	Input	Number of ports polled in MPHY operation
RcvCellCntEn	Output	Enable to count total number of cells.
RuntCellCntEn	Output	Enable to count total runt cells transmitted.
PErrCellCntEn	Output	Enable to count cells with parity error.
ExcessCellCntEn	Output	Enable to count total excess cells received.

Core Modifications

Normally, modifications are not possible by the user since the core is provided in a Xilinx netlist format. CoreEl can perform special modifications for additional charge. However source code is available for additional cost where the customer can make modifications. Contact CoreEl Microsystems for more information.

Pinout

The pinout is not fixed to any specific device I/O. Signal names for the transmit and receive UTOPIA blocks are provided in the block diagrams shown in Figures 2 and 3, and described in Tables 1 and 2, respectively.

Verifications Methods

This core has been used in larger ASICs and is silicon proven. The FPGA verification was done by back annotating the implementation and simulating in a Model technology V-System environment.

The test bench was written in VHDL with very powerful scripting capabilities and several scripts have been written for verifying the implementation. Additional tests can be added to the testbench by writing new scripts.

Recommended Design Experience

To implement a complete design using the Master UTOPIA Core, the user should have:

- Complete understanding of the UTOPIA Level-2 Specifications
- Knowledge of ATM and B-ISDN (Broadband ISDN)
- Familiarity with Xilinx FPGA architecture
- Familiarity with the simulation, synthesis and Xilinx tools

Available Support Products

Additional support tools and related products are available to help users to integrate this product into a system. These are available separately from CoreEl Microsystems and can be purchased separately.

UTOPIA Master Test Bench

The UTOPIA Master Test Bench facilitates simple, flexible and thorough testing of UTOPIA Master models conforming to UTOPIA Level-2, Version 1.0 Specifications. This script-based test bench tests all possible fault conditions of the master using simple commands. It generates a report file of the handshaking that occurs between the UTOPIA Master model and the test bench.

UTOPIA Slave Core Cell (CC141)

The UTOPIA Slave Core (SUC) can be used in any ATM layer device. It facilitates data transfer between ATM layer and UTOPIA compatible PHY devices. This core has been implemented in Xilinx FPGAs.

UTOPIA Slave Test Bench

The UTOPIA Slave Test Bench provides simple, flexible and thorough testing of UTOPIA Slave models, conforming to UTOPIA Level 2 Ver. 1.0 specifications. The UTOPIA slave test bench is actually a UTOPIA master model. This script-based test bench tests all possible fault conditions of the slave using simple commands. It generates a report file of the handshaking that occurs between the UTOPIA Master model and the test bench.

Ordering Information

For information on this or other products mentioned in this datasheet, contact CoreEl Microsystems directly from the information provided on the front page.

Related Information

The ATM Forum

The ATM Forum publishes specifications regarding ATM. For more information, contact them as follows:

ATM Forum
Worldwide Headquarters
2570 West El Camino Real, Suite 304
Mountain View, CA 94040-1313
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Fax: +1 650-949-6705
E-mail: info@atmforum.com
URL: www.atmforum.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
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URL: www.xilinx.com/products/logicore/alliance/tblpart.htm