XC4000EX Routing: A Comparison with XC4000E and ORCA

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Summary

The new XC4000EX family includes large amounts of new routing resources, necessary to support today's larger designs. These resources are detailed and compared with the XC4000E, and with ORCA devices from Lucent Technologies (formerly AT&T).

Xilinx Family

XC4000EX, XC4000XL

Demonstrates

CLB routing resources
IOB routing resources (VersaRing™)
Global clocking

XC4000EX Routing Philosophy

Xilinx XC4000EX devices were designed for applications over 25,000 gates. As the number of gates in a design grows, the amount of routing required to service these gates grows even faster. FPGAs consist of arrays of programmable logic blocks; as the array size increases, more routing is required to service each logic block. Additional routing can be included in the logic block, which is then replicated throughout the array, or it can be added as one or more localized wide buses, or tracks. Xilinx decided against using localized routing tracks, because they are less versatile than routing distributed throughout the logic cell array. Distributed routing is available wherever needed, while to use the routing track often requires routing the signal over to the track, then back again to the destination, resulting in additional unnecessary delay.

Xilinx addressed the routability needs of today's high-density designs by greatly increasing the routing available in their XC4000E series Configurable Logic Block (CLB), then increasing the size of the array to up to 62,000 usable gates. The new family thus formed is called the XC4000EX.

The XC4000EX family also includes many other new features, but they are not addressed here. See the *XC4000 Series Field Programmable Gate Arrays* product specification and the application note *"*System Design with New XC4000EX I/O Feature*s"* for details.

Comparison of Routing Resources

Logic array routing in XC4000-Series devices can be divided into three broad categories:

- General interconnect
- Global nets
- Carry logic.

The routing resources available in one CLB are shown in Table 1.

Input/Output areas have their own routing, which can be categorized as:

- General interconnect
- Global nets
- Edge decoders.

ORCA routing can be divided into similar categories, except that ORCA devices also offer localized "track" routing. This track routing is taken into account in all of the discussions below, and factored into all calculations as if it were distributed throughout the logic array.

Routing in Logic Array

General Interconnect

XC4000EX general interconnect includes the same single- and double-length lines as the XC4000E. (Single- and double-length lines span one and two CLBs, respectively.) The number of longlines, which span the whole array, has been increased from twelve to sixteen by adding four new vertical longlines. Because of the larger array size, these longlines can also be split into four independent segments, rather than two segments as in the XC4000E.

Table 1: Routing per CLB in XC4000E/EX Devices

	XC4000E		XC4000EX	
	Vertical	Horizontal	Vertical	Horizontal
Singles	8	8	8	8
Doubles	4	4	4	4
Quads			12	12
Longlines	6	6	10	6
Direct Connects			2	2
Globals	4		8	
Carry Logic	2	0	1	0
Total	24	18	45	32

Two new types of general interconnect have been added. Direct connect lines provide two fast paths between adjacent blocks, from left to right and top to bottom. The direct connect lines also provide a feedback path that reduces the delay on the feedback loop to approximately one-third of its previous value. The new quad lines were designed for the fastest possible signal distribution over long distances. Each quad line is optionally buffered at every fourth CLB, with the timing-driven software automatically buffering wherever desirable.

ORCA device routing can be divided into similar categories. The amount of available ORCA routing per row and column is shown in Table 2. Interquad routing is a localized routing track, a group of 20 lines through the center of the chip, both vertically and horizontally. Some users reported serious routing difficulties in the ORCA 2C26, which may have led to the addition of the subquad routing in the 2C40. Subquad routing is somewhat more dispersed, being grouped in a track every four PLC rows or columns.

Table 1 and Table 2 show 77 lines per XC4000EX CLB, 68 per 2C26 PLC, and 74 per 2C40 PLC. However, a direct comparison between the numbers of routing channels in ORCA and the XC4000EX family is not meaningful, because the ORCA basic logic block, the Programmable Logic Cell (PLC), is twice as large as the XC4000EX CLB. Additionally, an ORCA PLC has 23 pins, while an XC4000EX CLB has only 16 pins. Therefore, the PLC clearly requires more routing channels to service the logic. For a meaningful comparison, the number of routing channels per logic block pin is compared in Table 3.

Clearly, while the ORCA devices have marginally more routing than XC4000E devices, they do not stack up well against the XC4000EX routing.

Table 2: Routing per PLC in ORCA Devices

	ORCA 2C26		ORCA 2C40	
	Vertical	Horizontal	Vertical	Horizontal
Singles	8	8	8	8
Quads	8	8	8	8
Half Longlines	4	4	4	4
Longlines	4	4	4	4
Direct Connects	5	5	5	5
Globals	2	2	2	2
Carry Logic	2	2	2	2
Interquad Routing[1]	0.83	0.83	0.7	0.7
Subquad Routing[2]			3.1	3.1
Total	33.83	33.83	36.8	36.8

1. 20 horizontal and 20 vertical lines, once in each device. Number displayed is 20 divided by the number of PLC rows and columns in the device.
2. 12 horizontal and 12 vertical lines, every 4 PLC rows or columns, plus 4 extra lines twice per device. Number displayed is 3 + (4 divided by 30 PLCs). Only supported in 2C40 devices.

Table 3: Routing per CLB/PLC Pin for XC4000E, XC4000EX and ORCA Devices

	XC4000E		XC4000EX		ORCA 2C26		ORCA 2C40	
	Vertical	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	Horizontal
Singles	0.5	0.5	0.5	0.5	0.35	0.35	0.35	0.35
Doubles	0.25	0.25	0.25	0.25				
Quads			0.75	0.75	0.35	0.35	0.35	0.35
Half Longlines					0.17	0.17	0.17	0.17
Longlines	0.375	0.375	0.625	0.375	0.17	0.17	0.17	0.17
Direct Connects			0.125	0.125	0.22	0.22	0.22	0.22
Globals	0.25		0.5		0.09	0.09	0.09	0.09
Carry Logic	0.125		0.06		0.09	0.09	0.09	0.09
Interquad Routing					0.04	0.04	0.03	0.03
Subquad Routing							0.13	0.13
Total	1.5	1.125	2.81	2.00	1.48	1.48	1.6	1.6
Overall	2.625		4.81		2.96		3.2	

Global Nets

In the XC4000EX, several buffered long lines are added for the use of global nets. These nets are designed for fast, low-skew distribution of global signals, usually clocks or control signals. The number of these lines is increased from four per CLB column in the XC4000E to eight per column in the XC4000EX. They can be driven from any of the Global Low-Skew or Global Early clock buffers in the device. They are also accessible from local routing; consequently, a virtually unlimited number of signals can be used as clocks throughout the array.

ORCA devices have only two vertical and two horizontal global nets per PLC. The *AT&T Field-Programmable Gate Arrays Data Book* warns against using these lines to drive the clocks, however. Instead, they are to be used as clock spines, while perpendicular longlines are used to distribute the clock signals. (Strictly speaking, therefore, these lines should not have been included as "Globals" in Table 2 and Table 3, and the routing totals for ORCA devices are slightly lower than reported in these tables.)

The "clock spine" method of distributing clocks has the advantage of allowing clocks to be placed on any pad. However, this advantage must be weighed against the potential skew when pads not in the center of a pad edge are used for clocks. Another, potentially very serious, problem occurs when clock pads are locked down to adjacent sides of the chip. The longlines used to distribute the clocks are the same lines driven by the 3-state buffers and used for bidirectional buses. They are constrained to be at right angles to the clock spine. Therefore, if clocks are placed on adjacent edges, both vertical and horizontal longlines are needed by the clocks. If a number of 3-state buses are also used in the design, a conflict occurs. The only reasonable solution in this case is to route one of the clocks from one edge to another, to place the two clocks on the same or opposite edges, before placing it on a clock spine. The result is a sometimes unacceptable delay on the clock net.

Table 4: Global Routing in XC4000E, XC4000EX, and ORCA Devices

	XC4000E	XC4000EX	ORCA
Global Nets per Column/Row	4/0	8/0	2/2
Direct Access to Logic Clock Pins?	Yes	Yes	No
Accessible from Local Routing?	No*	Yes	No
Free From Contention with 3-State Buffers?	Yes	Yes	No
Special Fast and Early Clock Buffers	No	Yes	No

* Local signals must be routed through Global Secondary buffers

Xilinx has traditionally taken the conservative approach of using designated clock pads, with dedicated clock networks and buffers, to guarantee both a minimum skew for all clocks, and no longline contention. Doubling the number of dedicated clock lines in each XC4000EX CLB column, and allowing access to the drivers from local interconnect, adds considerable flexibility to the clocking scheme. The addition of two new types of clock buffers, Global Early and FastCLK™ buffers, adds even more flexibility and performance. For more information, see the *XC4000 Series Field Programmable Gate Arrays* product specification and the application note "System Design with New XC4000EX I/O Features."

Carry Logic

Carry logic in the XC4000 Series consists of dedicated nets that deliver the carry out signal to adjacent CLBs. In the XC4000E, the carry chain runs either up or down. In the XC4000EX, in order to gain speed for potentially very long carry chains, the carry chain is limited to the upward direction. However, general interconnect can be used to continue a carry chain from the top of one column to any point in an adjacent column.

Studies show that limiting the direction of a dedicated carry chain has less effect on placement flexibility than might be expected, since data flow is usually perpendicular to the direction of a carry chain, and in a data path the least significant bit is usually at the same end. Limiting the carry chain to one direction, on the other hand, significantly increased carry chain speed by eliminating a multiplexer from the path through each CLB. The advantage of the faster speed was felt to overcome the disadvantage of a unidirectional carry chain, as long as the general-interconnect option was available.

ORCA designers chose to add flexibility to their carry chain direction, rather than speed. The method giving the best result for a particular design will probably vary.

Routing in Input/Output Ring

XC4000EX devices include a VersaRing™, a ring of versatile routing by the pads that facilitates changing a design after the pins have been locked down. The routing within the VersaRing is summarized in Table 5.

Much of the routing in the VersaRing is comparable to the routing in the logic array. However, the octal lines are new in the XC4000EX. They are very flexible, in that they have excellent connections to other routing in the VersaRing. They are also buffered every eighth CLB (every sixteenth pad), to facilitate faster bussing of signals where the pad must be placed away from the source or destination logic.

As shown in Table 5, both XC4000E and XC4000EX devices have excellent I/O routing compared to ORCA. The eight octal lines, in particular, give the XC4000EX a decided advantage.

Table 5: I/O Routing in XC4000E, XC4000EX, and ORCA Devices (edge decoders omitted)

	XC4000E	XC4000EX	ORCA
Singles			4
Doubles	8	8	4
Octals		8	
Half Longlines			4
Longlines	4	4	2
Direct Connects	2	2	
Globals	2[1]	3.5[2]	
Total	16	25.5	14

1. Average of 4 at left and right edges, none at top and bottom
2. Average of 8 at right edge, 4 at left edge, 1 at top and bottom

Wide Edge Decoders

Four extra lines are included in the VersaRing, but omitted from Table 5 because they cannot be used for general interconnect. These lines can be used to implement wide edge decoders along each edge of the XC4000-Series FPGA. The maximum number of inputs is one for each I/O pad along the edge, plus one for each row or column of CLBs. The wide edge decoder lines can be broken at the center to permit a total of eight decoders per edge, or 32 per device.

ORCA devices do not include edge decoders.

Summary

The XC4000EX has significantly more routing than the ORCA devices. For some designs, this difference may not be important, but for larger, denser designs, it may prove crucial.

It is reasonable to expect that designs implemented in the XC4000EX family of devices will not be routing-limited. Achievable gate counts for XC4000EX devices will certainly be higher than would be expected for XC4000E CLB arrays of the same size.

Two more subtle benefits derive from the additional routing resources.

Firstly, even when the additional routing is not required to implement the design, it will definitely help to make the routing process more of a push-button solution. Complicated designs that would otherwise require manual intervention may route automatically.

Secondly, abundant routing reduce the need for complicated routing paths and feed-throughs, resulting in faster implementations.

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