Synchronous RAM Timing in the

The XC4000E FPGA's synchronous memory mode simplifies the timing of the memory interface and contrbutes to increased utilization and performance (as compared to asynchronous timing schemes). With proper attention to address routing delays, synchronous RAMs constructed from the CLBs of an XC4000E FPGA can be operated at, or close to, the maximum clock frequency, as determined by the minimum write cycle time. This is 70 MHz for XC4000E-3 devices. (All calculations below are for the -3 speed grade).

Write Operations

Most applications generate the RAM address in a synchronous register or counter, clocked by the same Global Clock edge as the synchronous RAM *(Figure 1)*. The address output is guaranteed to be available T_{CKO} after the active clock edge, and this address must arrive at the CLB-RAM one T_{ASS} set-up time before the next active clock edge. At 70 MHz, this leaves 9.2 ns for routing the address to all the CLBs that make up the RAM block. With appropriate CLB placement, this should not be difficult. Of course, set up times on the write data input also must be met.

WRITE TIMING, FIGURE 1

Clock Pulse Width	T_{WPS}	7.2 ns
Write Cycle Time	T_{WCS}	14.4 ns minimum (70 MHz maximum)
Address Register clock-to-out delay	T_{CKO}	2.8 ns maximum
Address Set-up Time	T_{ASS}	2.4 ns minimum
Maximum allowed address routing delay @ 70 MHz		14.4–2.8–2.4 = 9.2 ns

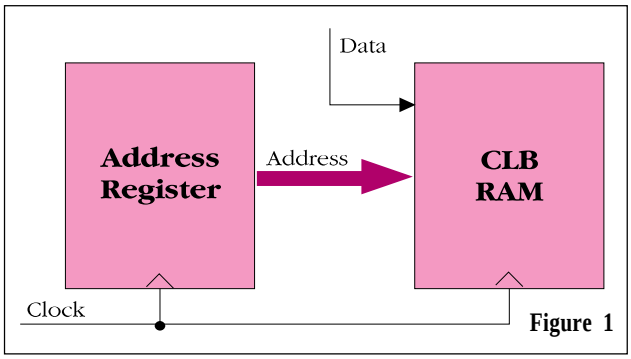

Figure 1

Read Operations

The output from a CLB function generator being used as RAM can be either combinatorial or synchronized using the CLB flip-flop. The combinatorial output from the CLB-RAM is guaranteed to be valid one T_{ILO} (for the 16x2 memory mode) or T_{IHO} (for the 32x1 memory mode) after the arrival of the address at the CLB. Again assuming that the address is held in a register, the total time from the active clock edge at that register to valid data out is

T_{CKO} + address routing delay + (T_{ILO} or T_{IHO}).

If a CLB-internal flip-flop is used to register data read from the RAM *(Figure 2)*, read timing is simple. Of the whole clock period, only T_{CKO} and T_{ICK} are consumed as logic delays; the remainder of the clock period is available for address routing.

READ TIMING, FIGURE 2

Address Register clock-to-out delay	T_{CKO}	2.8 ns maximum
CLB register set-up time (16x2)	T_{ICK}	3.0 ns
CLB register set-up time (32x1)	T_{IHCK}	4.6 ns
Maximum allowed address routing delay @ 70 MHz (16x2)		14.4–2.8–3.0 = 8.6 ns
Maximum allowed address routing delay @ 70 MHz (32x1)		14.4–2.8–4.6 = 7.0 ns

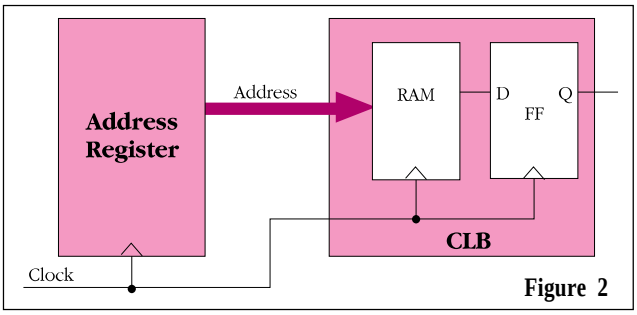

Figure 2

Read Operations *(continued)*

If the pipelined output drives the data input to another CLB-RAM *(Figure 3)*, only T_{CKO} and T_{DSS} are consumed as logic delays on the data path, the remainder of the clock period is available for data routing. The routing delay to the nearest neighbor is already included in T_{CKO}; that is, there is no additional routing delay to take into account if the RAM data is being propagated to the neighboring CLB. Otherwise, the maximum allowable delay for routing the data is calculated as follows (assuming that the second RAM's address is available T_{ASS} before the clock edge):

READ TIMING, FIGURE 3

Registered Data valid after clock	T_{CKO}	2.8 ns
Data input set-up time (16x2)	T_{DSS}	3.2 ns
Data input set-up time (32x1)	T_{DSTS}	1.9 ns
Maximum allowed registered data routing delay (16x2)		14.4–2.8–3.2 = 8.4 ns
Maximum allowed registered data routing delay (32x1)		14.4–2.8–1.9 = 9.7 ns

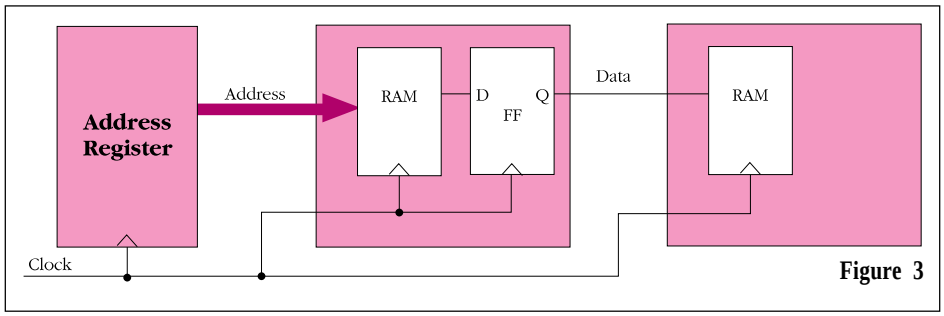

Figure 3

Suppose that the RAM data output bypasses the register in its CLB, but is an input to a function in another CLB, and the output of that function generator is registered with the same clock that is used to register the RAM address *(Figure 4)*. Valid data must be available at that register T_{ICK} before the next active clock edge. Thus, T_{CKO} + (T_{ILO} or T_{IHO}) + T_{ICK} + data routing delay is the minimum time needed to read the CLB-RAM and gets its output to the destination CLB, through its function generator and to the register.

READ TIMING, FIGURE 4

Address Register clock-to-out delay	T_{CKO}	2.8 ns maximum
Data Valid After Address (16 x 2)	T_{ILO}	2.0 ns maximum
Data Valid After Address (32 x 1)	T_{IHO}	4.3 ns maximum
Register Set-up Time	T_{ICK}	3.0 ns minimum
Maximum allowed data routing delay @ 70 MHz		14.4–2.8–2.0–3.0 = 6.6 ns

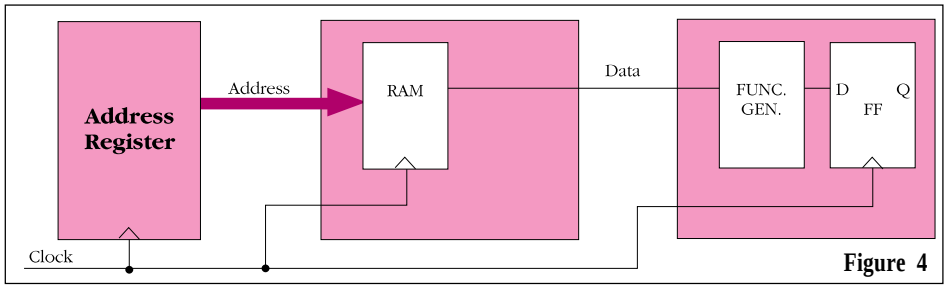

Figure 4

Conclusion

Controlling the timing of synchronous RAM operation is fairly straightforward. For most applications, synchronous RAMs constructed from the CLBs of an XC4000E FPGA can be operated at, or close to, the maximum clock frequency as determined by the minimum write cycle time. ◆